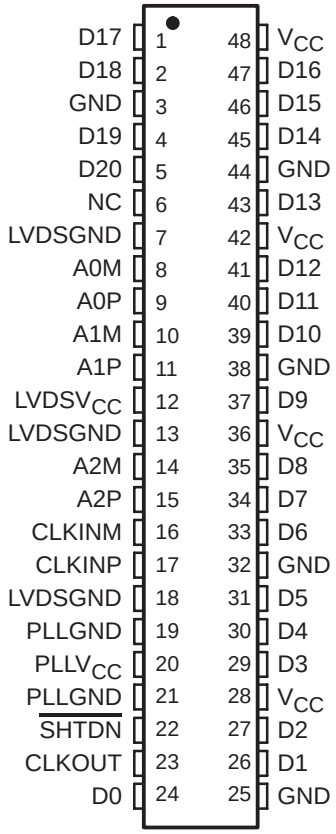
- **3:21 Data Channel Expansion at up to 178.5 Mbytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **Three Data Channels and Clock Low-Voltage Differential Channels In and 21 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant $\overline{\text{SHTDN}}$ Input**
- **ESD Protection Exceeds 4 kV on Bus Pins**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Open-Circuit Receiver Fail-Safe Design**
- **Inputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the National™ DS90C562**

DGG PACKAGE
(TOP VIEW)



NC − Not Connected

description

The SN75LVDS86 FlatLink receiver contains three serial-in 7-bit parallel-out shift registers, a 7× clock synthesizer, and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, ’83, ’84, or ’85, over four balanced-pair conductors, and expansion to 21 bits of single-ended low-voltage TTL (LVTTL) synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at seven times (7×) the LVDS input clock (CLKIN) rate. The data is then unloaded to a 21-bit-wide LVTTL parallel bus at the CLKIN rate. A phase-locked loop (PLL) clock synthesizer circuit generates a 7× clock for internal clocking and an output clock for the expanded data. The SN75LVDS86 presents valid data on the falling edge of the output clock (CLKOUT).

The SN75LVDS86 requires only four line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user. The only possible user intervention is the use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FlatLink is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

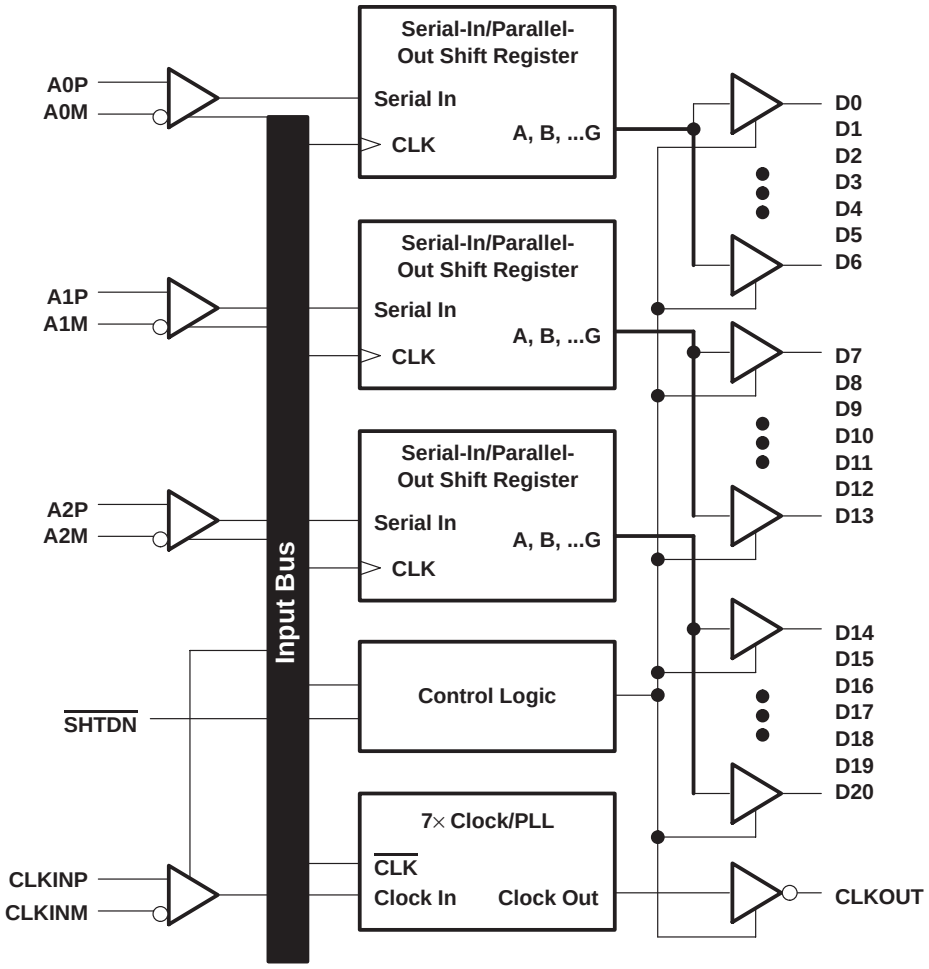
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2006, Texas Instruments Incorporated

The LVDS receivers of the SN75LVDS86 include an open-circuit fail-safe design, such that when the inputs are not connected to an LVDS driver, the receiver outputs go to a low level. This occurs even when the line is differentially terminated at the receiver inputs.

The SN75LVDS86 is characterized for operation over ambient free-air temperatures of 0°C to 70°C.

functional block diagram



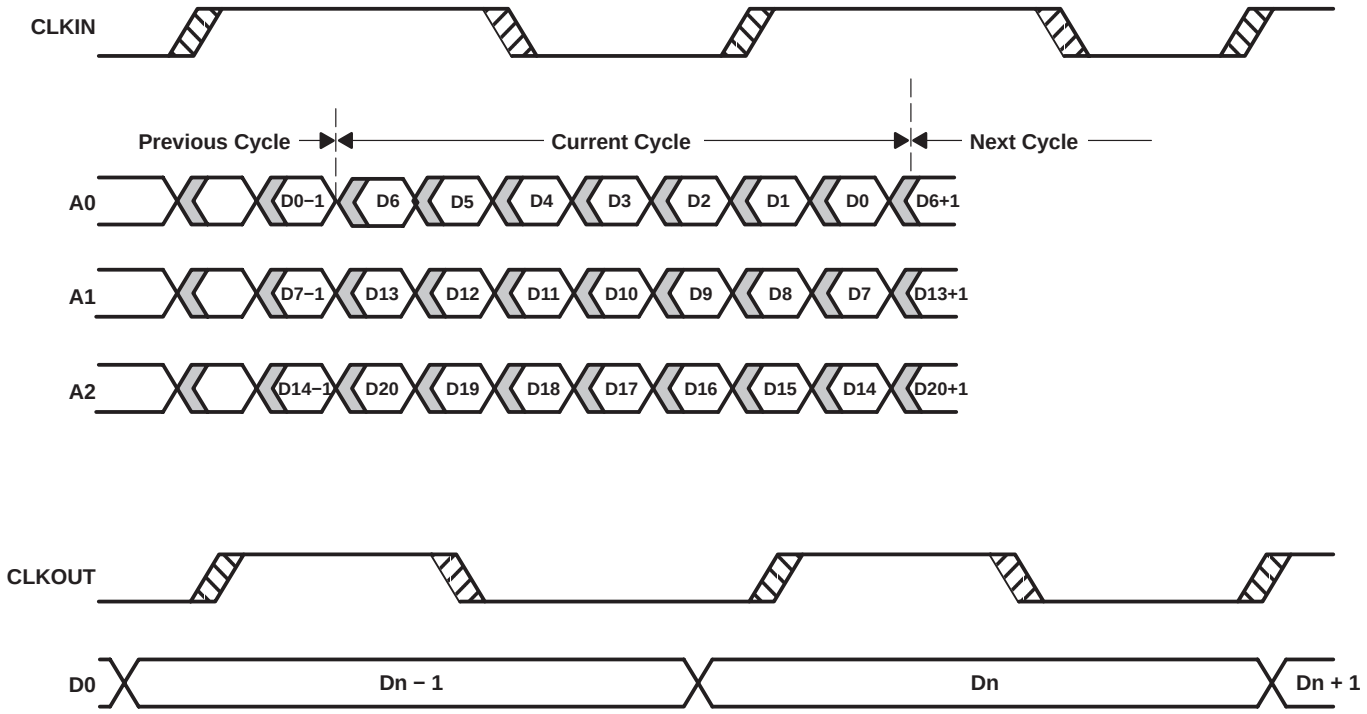
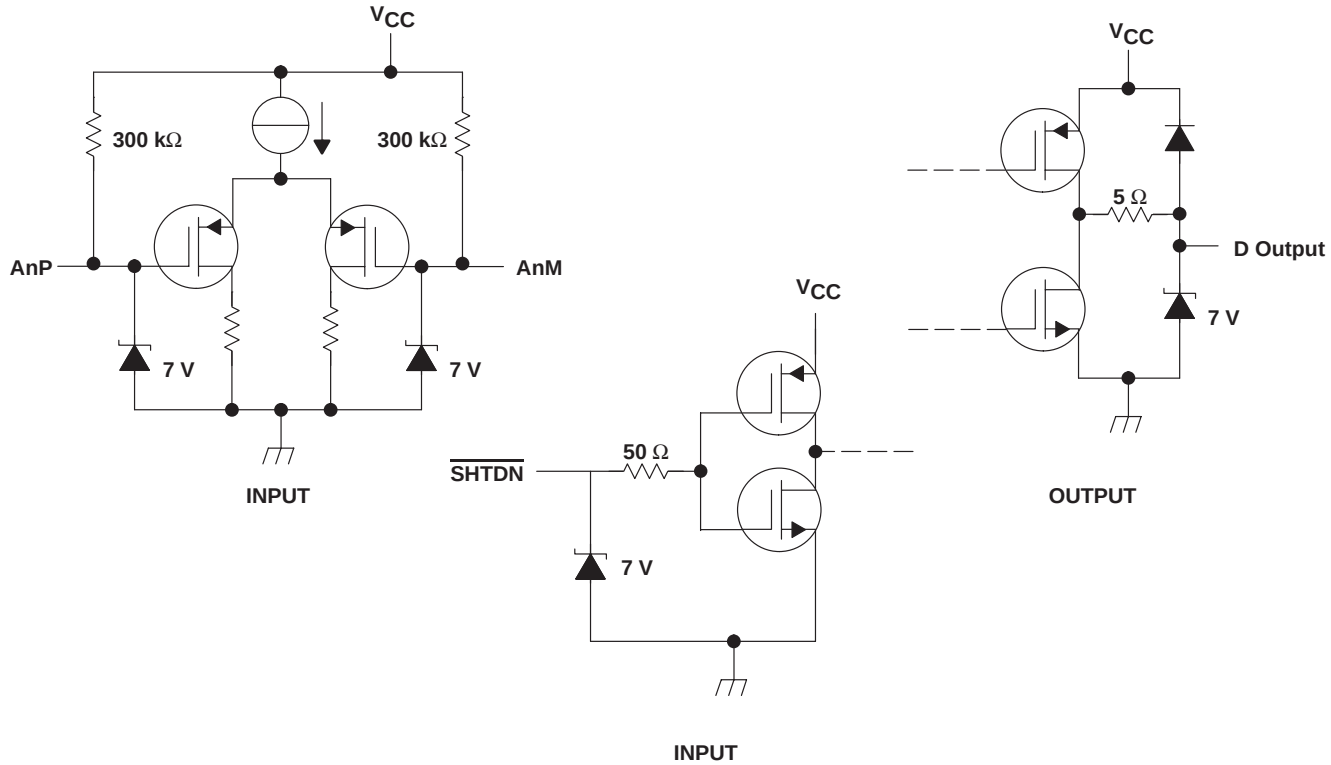


Figure 1. SN75LVDS86 Load and Shift Timing Sequences

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 4 V
Output voltage range, V_O (Dxx terminals) . . . . . −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I: Any terminal except $\overline{SHTDN}$ . . . . . −0.5 V to V_{CC} + 0.5 V
$\overline{SHTDN}$ . . . . . −0.5 V to 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DGG	1316 mW	13.1 mW/°C	726 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

recommended operating conditions (see Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH} ($\overline{SHTDN}$)	2			V
Low-level input voltage, V_{IL} ($\overline{SHTDN}$)			0.8	V
Differential input voltage, $\lvert V_{ID}\rvert$	0.1		0.6	V
Common-mode input voltage, V_{IC} (see Figure 2 and Figure 3)	$\frac{\lvert V_{ID}\rvert}{2}$		$2.4 - \frac{\lvert V_{ID}\rvert}{2}$	V
			$V_{CC} - 0.8$	
Operating free-air temperature, T_A	0		70	°C

timing requirements

		MIN	NOM	MAX	UNIT
t_c	Cycle time, input clock§	14.7	t_c	32.4	ns
t_{su1}	Setup time, input (see Figure 7)	600			ps
t_{h1}	Hold time, input (see Figure 7)	600			ps

§ Parameter t_c is defined as the mean duration of a minimum of 32 000 clock cycles.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage				100	mV
V_{IT-}	Negative-going differential input threshold voltage‡		−100			mV
V_{OH}	High-level output voltage	I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_{CC}	Quiescent current (average)	Disabled, All inputs open			280	µA
		Enabled, AnP = 1 V, AnM = 1.4 V, t_c = 15.38 ns		58	72	mA
		Enabled, C_L = 8 pF, Grayscale pattern (see Figure 4), t_c = 15.38 ns		69		
		Enabled, C_L = 8 pF, Worst-case pattern (see Figure 5), t_c = 15.38 ns		94		
I_{IH}	High-level input current ($\overline{SHTDN}$)	$V_{IH} = V_{CC}$			±20	µA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	V_{IL} = 0 V			±20	µA
I_I	Input current (LVDS input terminals A and CLKIN)	0 ≤ V_I ≤ 2.4 V			±20	µA
I_{OZ}	High-impedance output current	V_O = 0 or V_{CC}			±10	µA

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{su2}	Set up time, D0−D20 valid to CLKOUT↓	C_L = 8 pF, See Figure 6	5			ns
t_{h2}	Hold time, CLKOUT↓ to D0−D20 valid	C_L = 8 pF, See Figure 6	5			ns
t_{RSKM}	Receiver input skew margin§ (see Figure 7)	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps¶	490			ps
t_d	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	t_c = 15.38 ns (±0.2%), C_L = 8 pF		3.7		ns
$\Delta t_{c(o)}$	Cycle time, change in output clock period#	t_c = 15.38 + 0.75 sin (2π500E3t) ± 0.05 ns, See Figure 8		±80		ps
		t_c = 15.38 + 0.75 sin (2π3E6t) ± 0.05 ns, See Figure 8		±300		
t_{en}	Enable time, $\overline{SHTDN}$↑ to Dn valid	See Figure 9		1		ms
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off state	See Figure 10		400		ns
t_t	Transition time, output (10% to 90% t_r or t_f)	C_L = 8 pF		3		ns
t_w	Pulse duration, output clock			0.43 t_c		ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

§ The parameter $t_{(RSKM)}$ is the timing margin available to the transmitter and interconnection skews and clock jitter. It is defined by $\frac{t_c}{14} - t_{su1}/t_{h1}$.
¶ |Input clock jitter| is the magnitude of the change in input clock period.
# $\Delta t_{c(o)}$ is the change in the output clock period from one cycle to the next cycle observed over 15 000 cycles.

PARAMETER MEASUREMENT INFORMATION

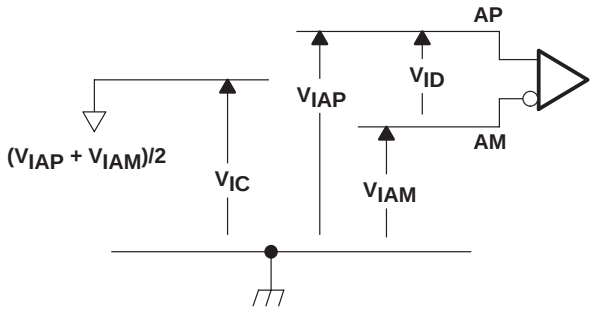


Figure 2. Voltage Definitions

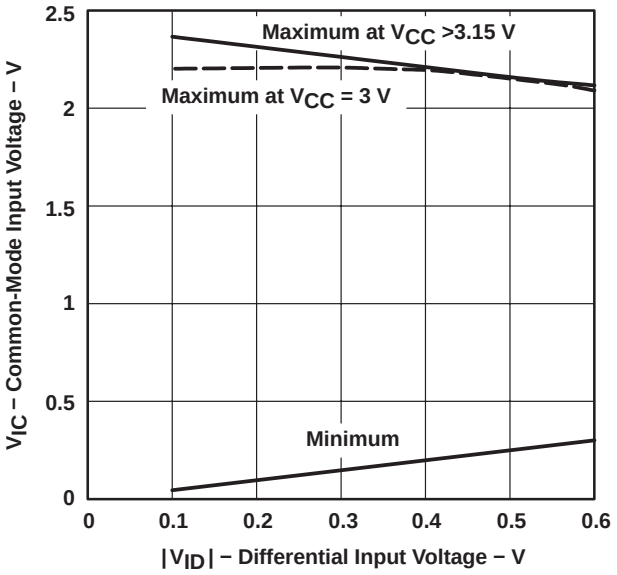
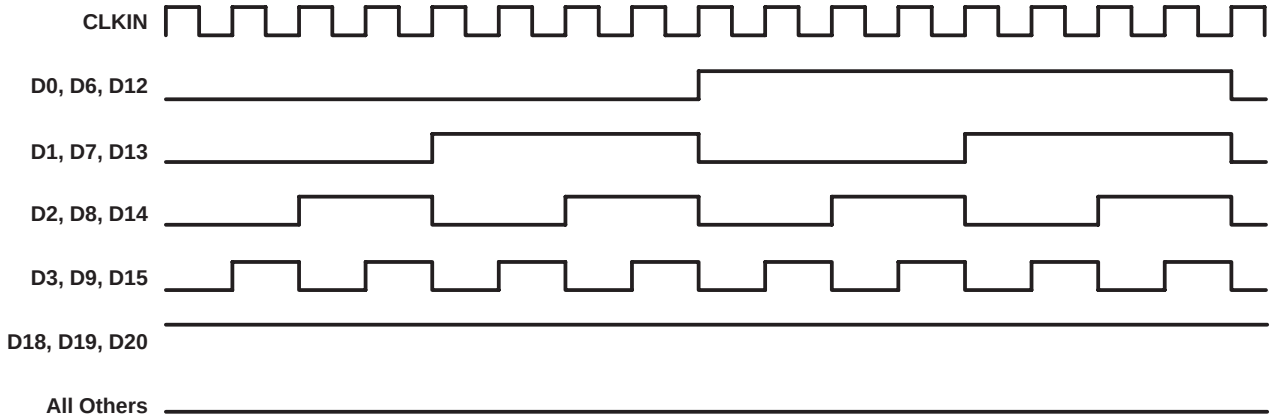


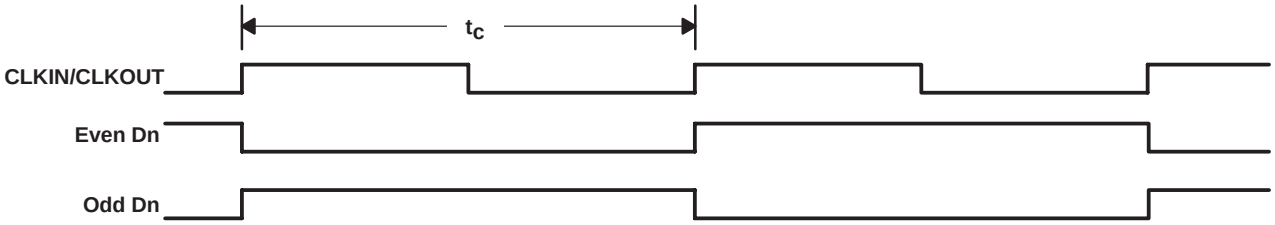
Figure 3. Common-Mode Input Voltage Vs Differential Input Voltage and V_{CC}

PARAMETER MEASUREMENT INFORMATION



NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern

Figure 4. 16-Grayscale Test Pattern



NOTE B: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVTTL outputs.

Figure 5. Worst-Case Test Pattern

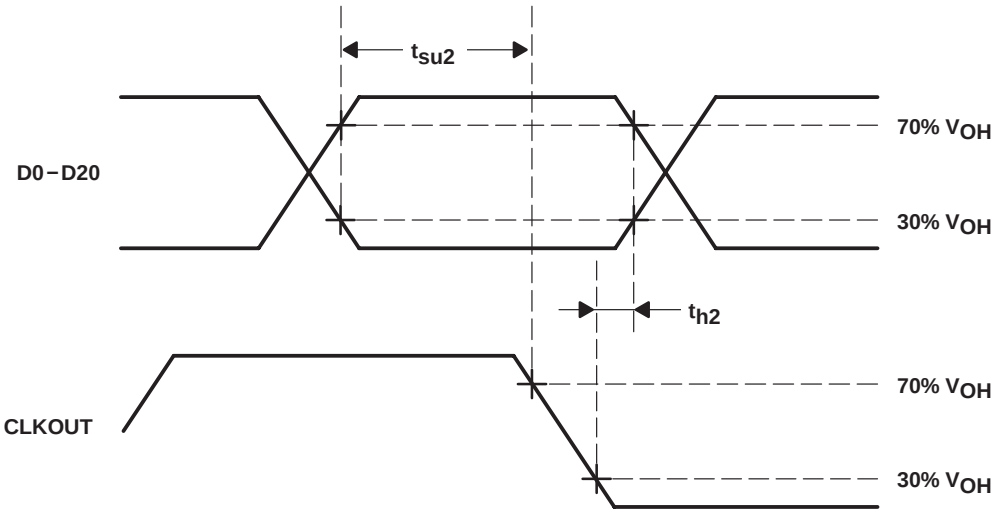
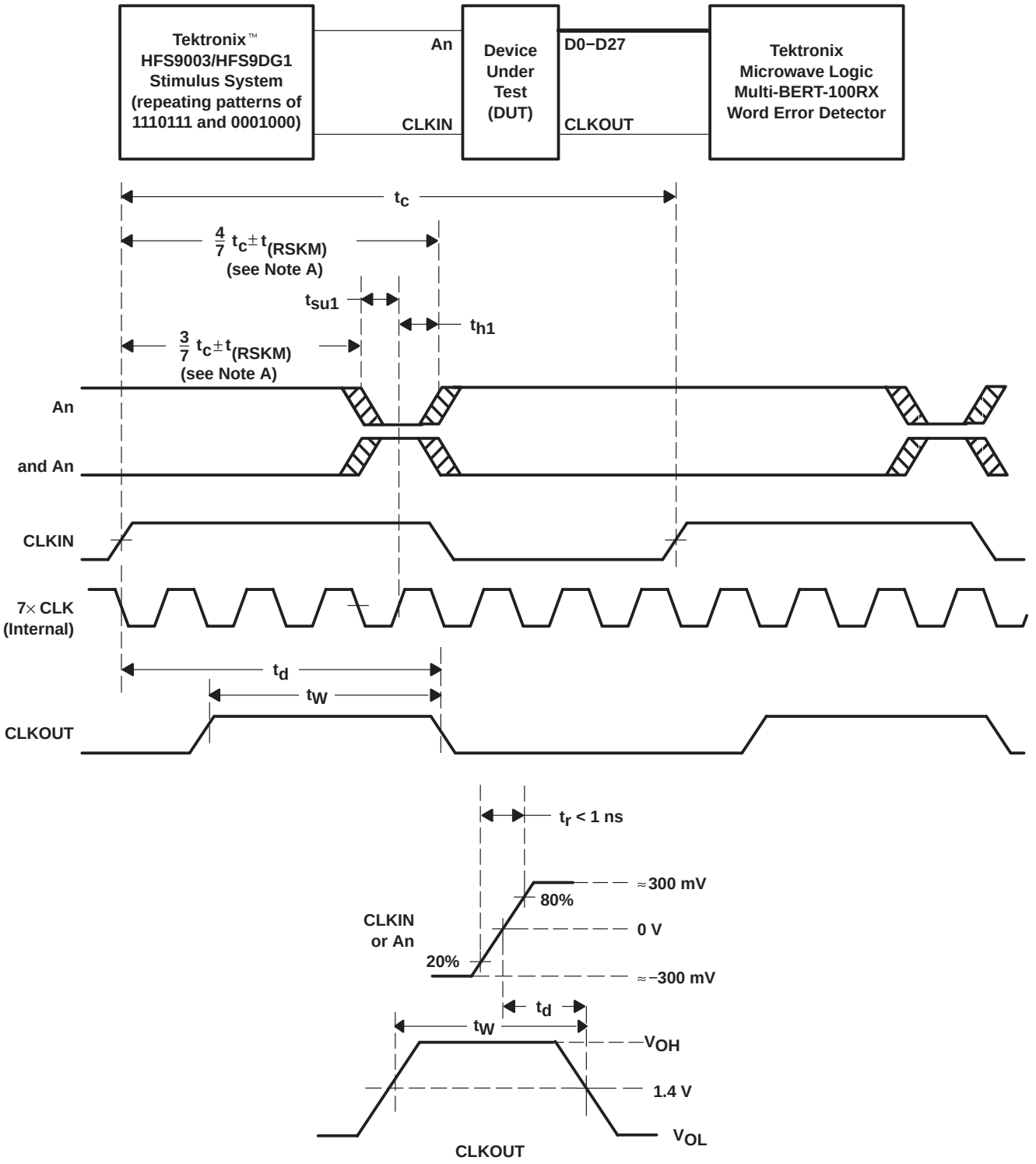


Figure 6. Setup and Hold Time

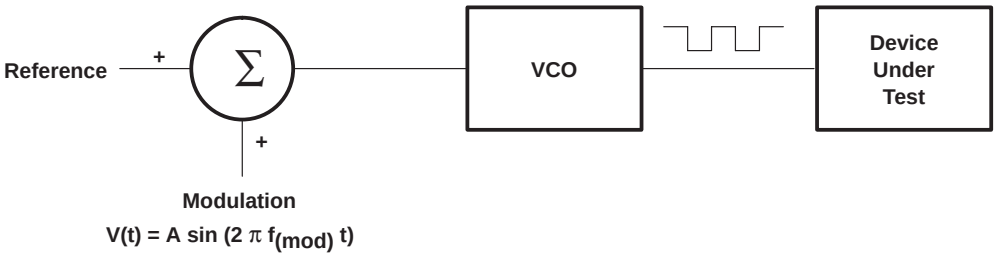
PARAMETER MEASUREMENT INFORMATION



NOTE A: CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is $t_{(RSKM)}$.

Figure 7. Receiver Input Skew Margin, Setup/Hold Time, and Delay Timing

PARAMETER MEASUREMENT INFORMATION



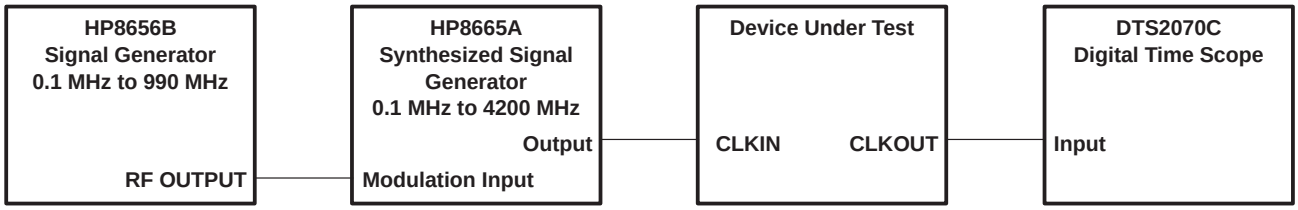


Figure 8. Output Clock Jitter Test Setup

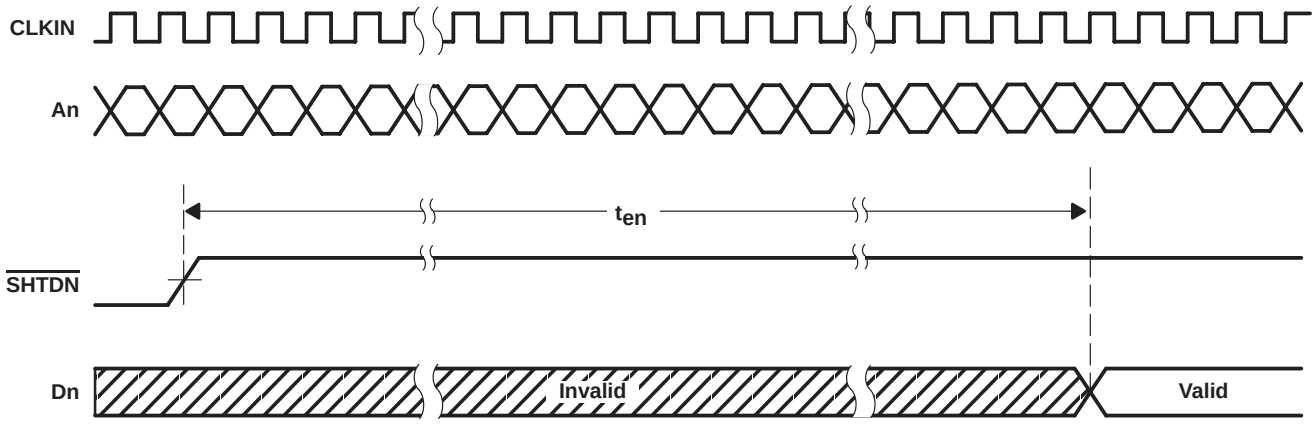


Figure 9. Enable Time

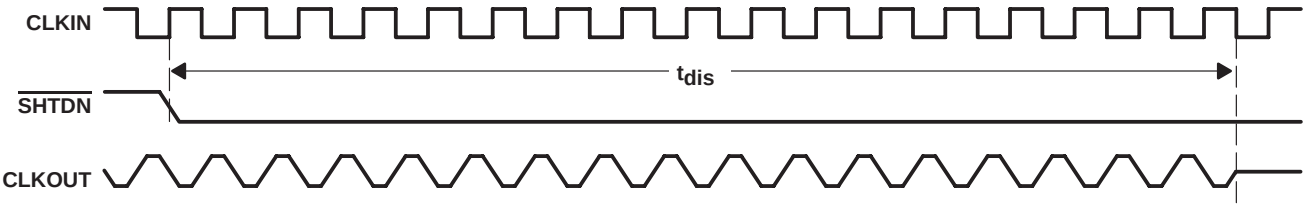


Figure 10. Disable Time

TYPICAL CHARACTERISTICS

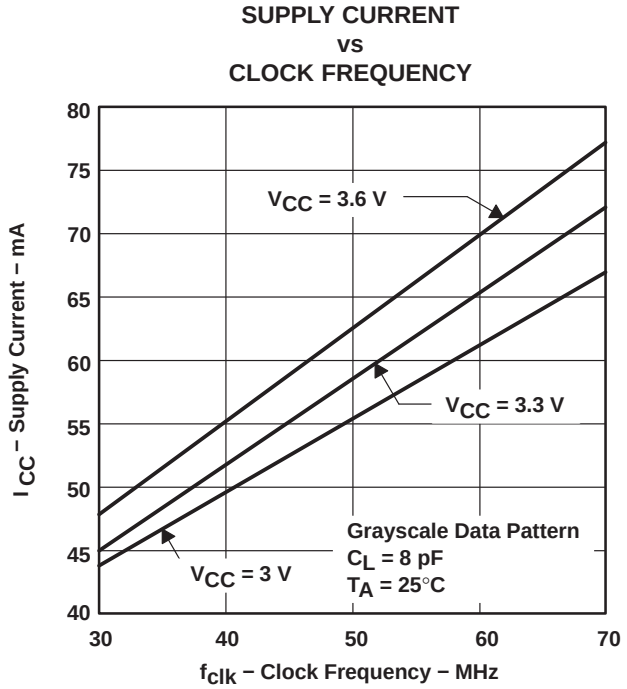


Figure 11. RMS Grayscale I_{CC} vs Clock Frequency

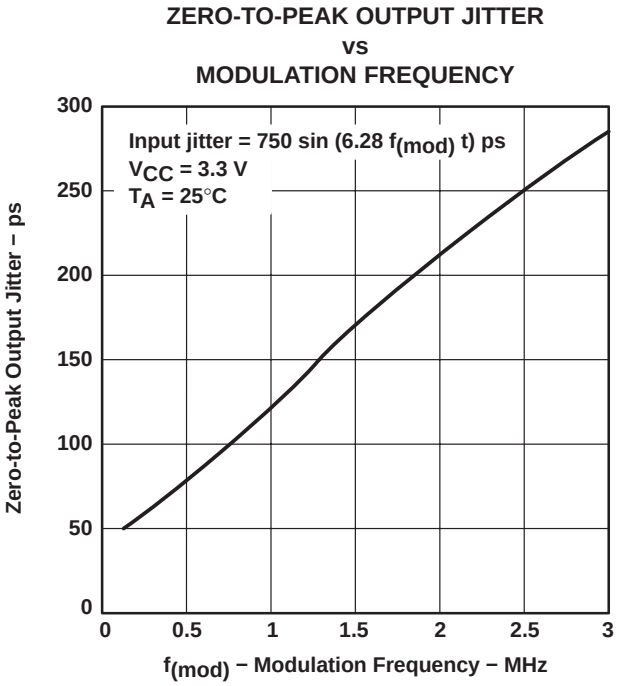
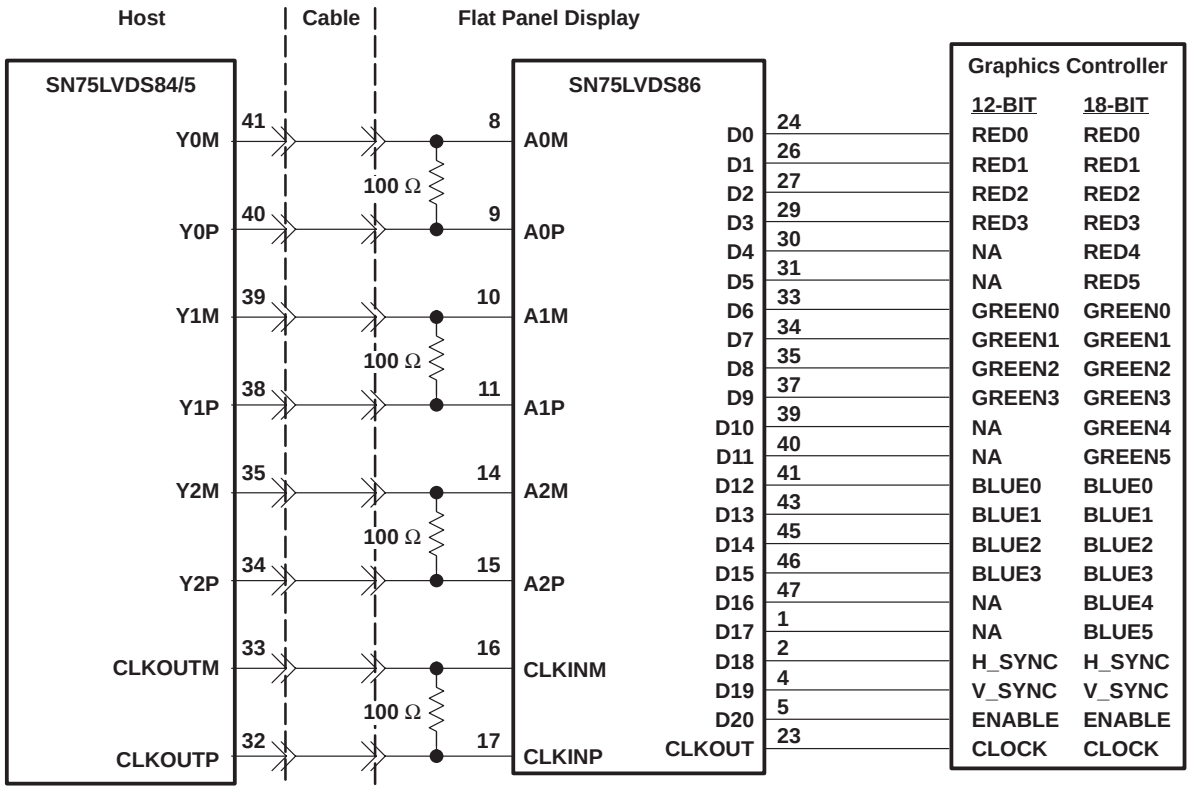


Figure 12. Typical FlatLink™ PLL Characteristics

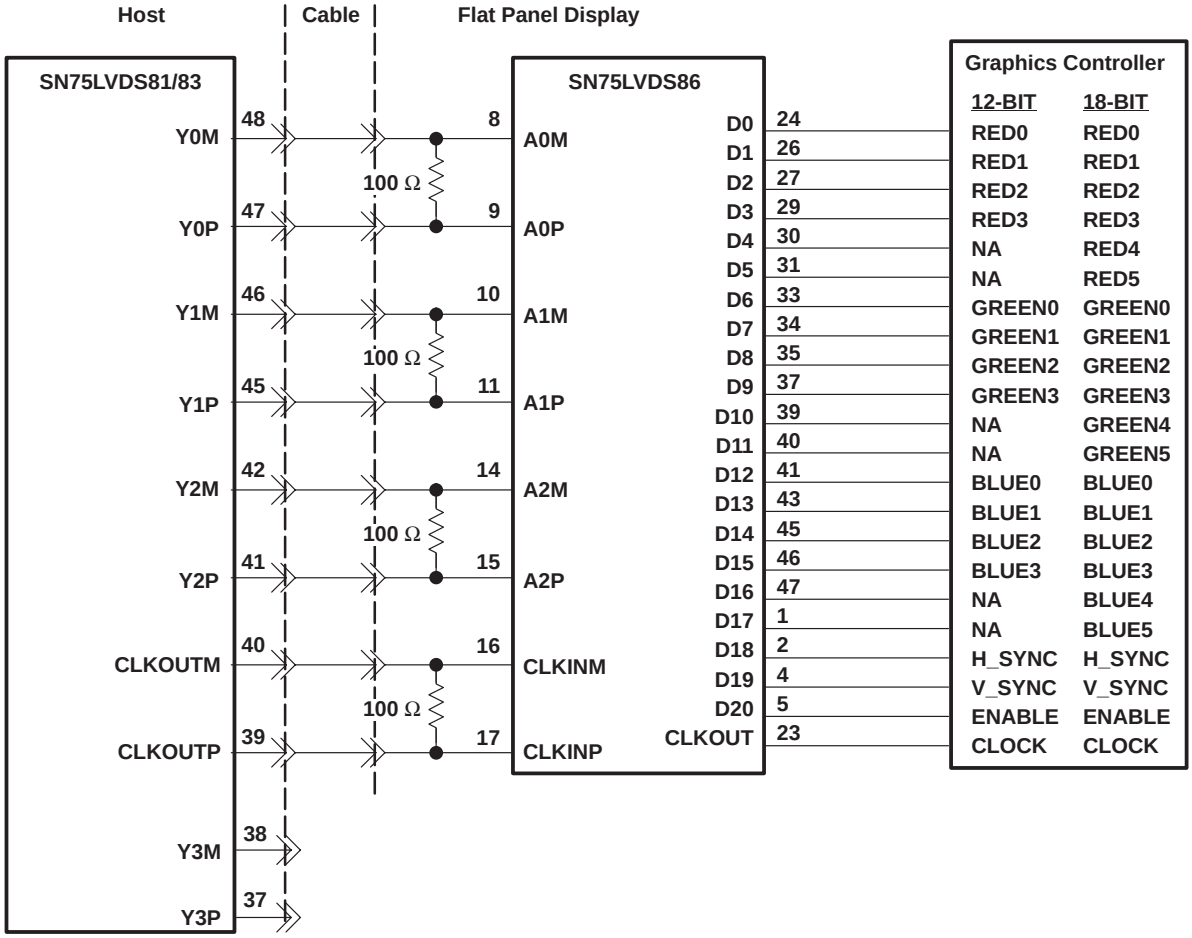
APPLICATION INFORMATION



NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
B. NA − not applicable, these unused inputs should be left open.

Figure 13. 18-Bit Color Host to Flat Panel Display Application

APPLICATION INFORMATION



NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
B. NA − not applicable, these unused inputs should be left open.

Figure 14. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application†

† See the *FlatLink ™ Designer's Guide* (SLLA012) for more application information.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVDS86DGG	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS86	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

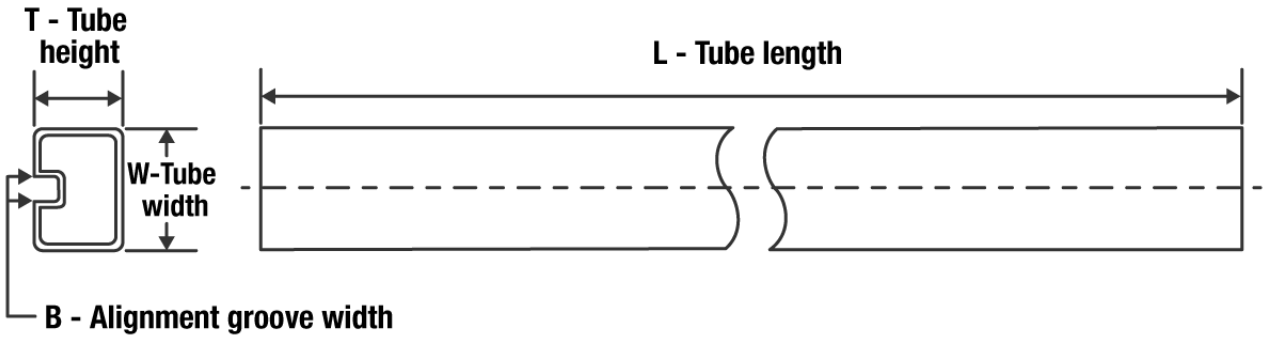
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

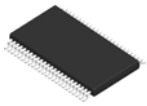
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75LVDS86DGG	DGG	TSSOP	48	40	530	11.89	3600	4.9

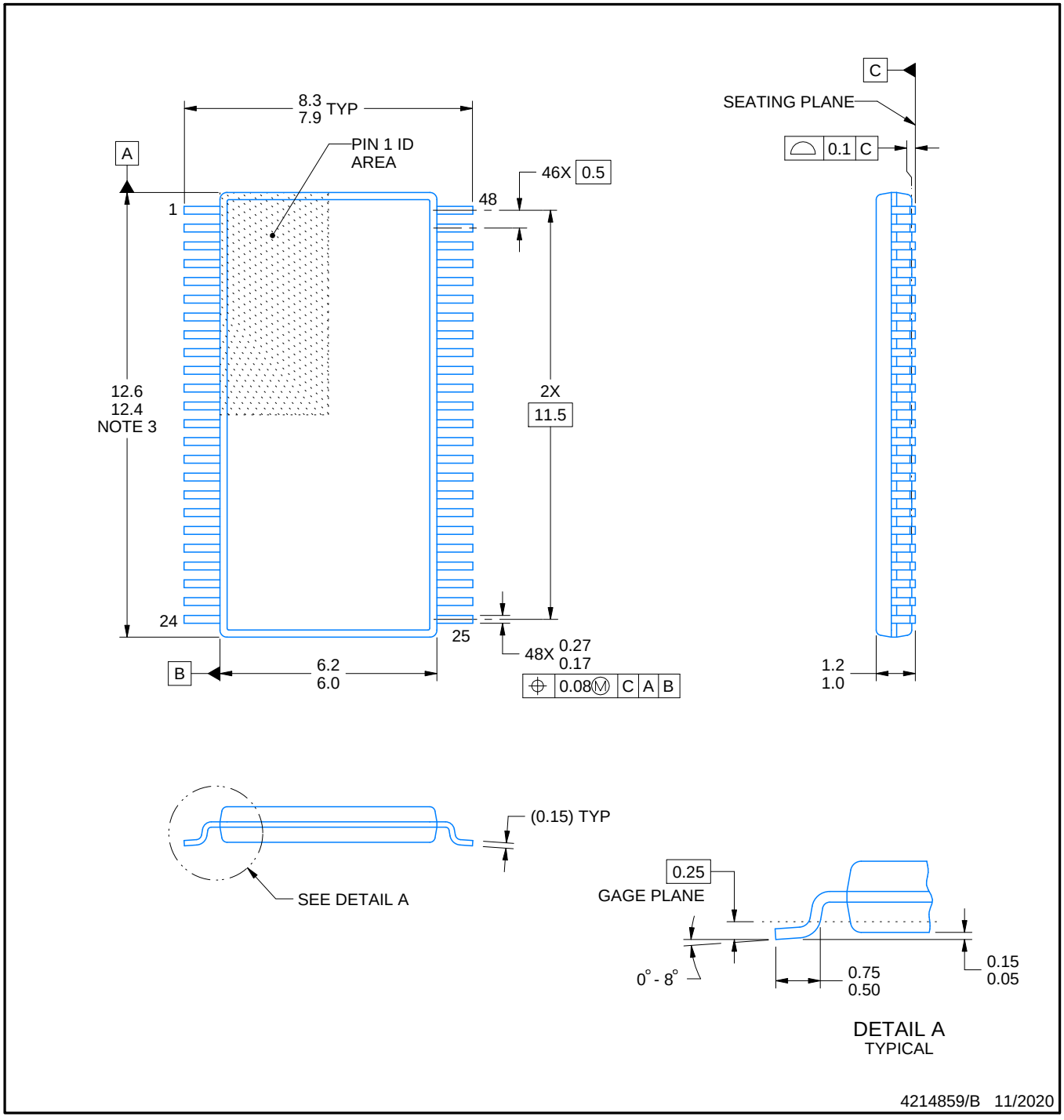


PACKAGE OUTLINE

DGG0048A

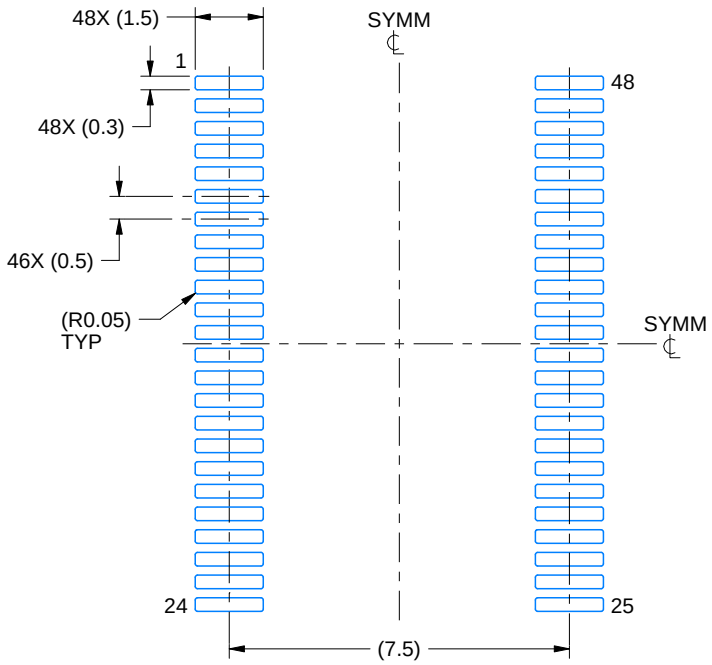
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

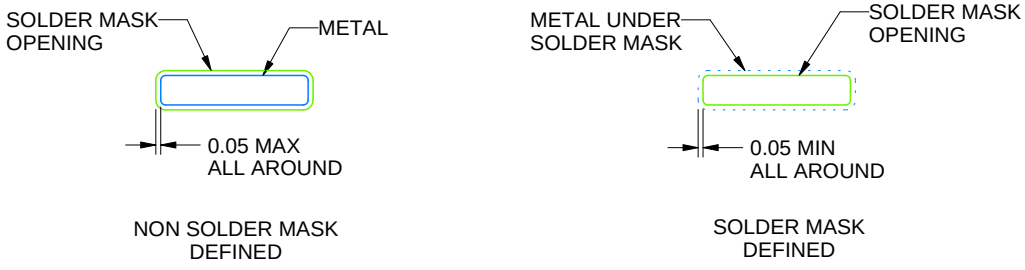


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

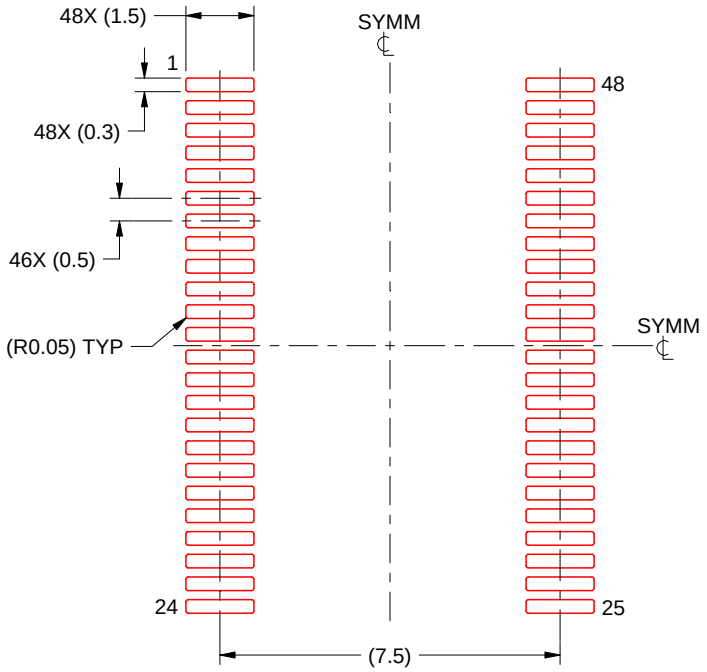


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

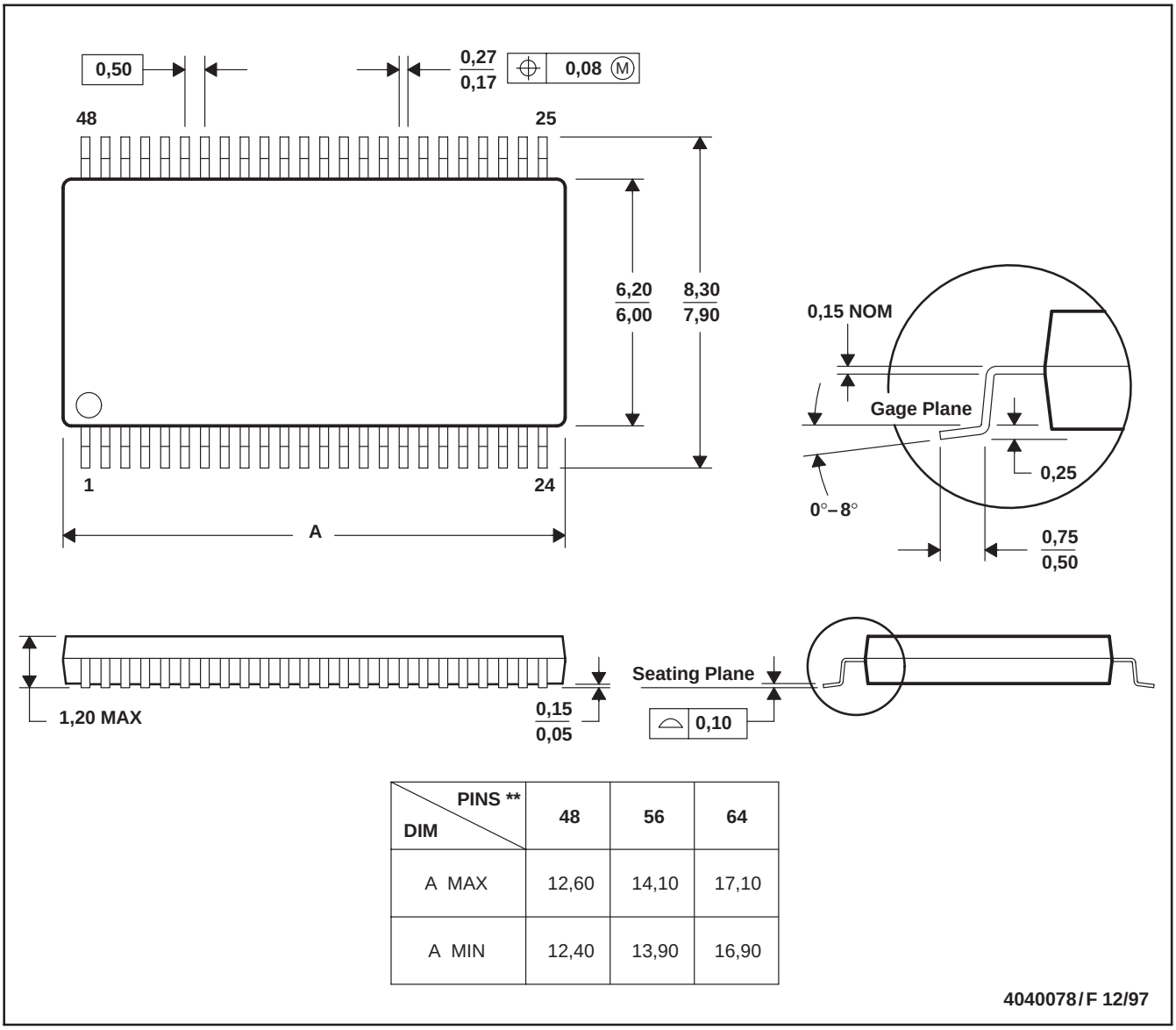
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated