PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/13/8165
Dated 14 Oct 2013

M95010, M95020, M95040, M95080, M95160 1-Kbit, 2-Kbit, 4-Kbit, 8-Kbit, 16-Kbit SPI bus EEPROM / Industrial grade Redesign and upgrade to the CMOSF8H

Table 1. Change Implementation Schedule

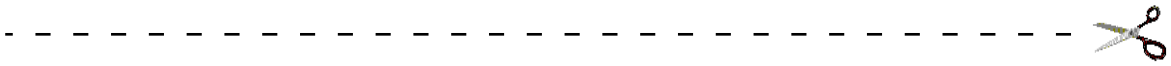
Forecasted implementation date for change	07-Oct-2013
Forecasted availability date of samples for customer	07-Oct-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	07-Oct-2013
Estimated date of changed product first shipment	13-Jan-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	1, 2, 4, 8, 16-Kbit SPI bus EEPROM indus. grade
Type of change	Waferfab technology change
Reason for change	Line up to state-of-the-art of process
Description of the change	Redesign and upgrade to the new CMOSF8H Process technology.
Change Product Identification	Proc. techno identifier "K" for SO8N
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/13/8165**
Please sign and return to STMicroelectronics Sales Office	**Dated 14 Oct 2013**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Leduc, Hubert	Marketing Manager
Rodrigues, Benoit	Product Manager
Pavano, Rita	Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

M95010, M95020, M95040, M95080, M95160
1-Kbit, 2-Kbit, 4-Kbit, 8-Kbit, 16-Kbit
SPI bus EEPROM / Industrial grade
Redesign and upgrade to the CMOSF8H process technology

What is the change?

The **M95010, M95020, M95040**, **M95080** and **M95160**, 1-Kbit, 2-Kbit, 4-Kbit, 8-Kbit and 16-Kbit SPI bus EEPROM product families for Industrial grade, currently produced using the CMOSF6SP 36% process technology at ST Ang Mo Kio (Singapore) 6" or at GLOBALFOUNDRIES (Singapore) 8" wafer diffusion plants, have been **redesigned** and will be **upgraded** to the **CMOSF8H** process technology at **ST Rousset** (France) 8" wafer diffusion plant.

This upgraded version in CMOSF8H allows offering:

- **1.7 V** / 5.5 V ("-**F**") Vcc range over industrial temperature range -40 / +85°C
- **Enhanced cycling** and **data retention** performances:
  - 4 million cycles
  - 200 years data retention

The new M95010, M95020 and M95040 in CMOSF8H version are functionally compatible with the current CMOSF6SP 36% version as per common datasheet rev. 11 – May 2013, attached.
The new M95080 in CMOSF8H version is functionally compatible with the current CMOSF6SP 36% version as per datasheet rev. 1 – March 2012 attached.
The new M95160 in CMOSF8H version is functionally compatible with the current CMOSF6SP 36% version as per datasheet rev. 3 – January 2013 attached.

Differences from current datasheets:

DC characteristic: I_{CC1} standby supply current:

- Max 2 µA at V_{CC} = 2.5 V
- Max 3 µA at V_{CC} = 5.5 V

Concurrent to this change, the new M95010, M95020, M95040, M95080 and M95160 in CMOSF8H will be assembled with 0.8 mil Copper wire when packaged in SO8N or in UFDFPN8 (MLP8).

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M95010, M95020, M95040, M95080 and M95160 in the new CMOSF8H process technology will increase the production capacity throughput and consequently improve the service to our customers.

When?

The production of the upgraded new M95010, M95020, M95040, M95080 and M95160 with the new CMOSF8H will ramp up from December 2013 and shipments can start from January 2014 onward (or earlier upon customer approval).

How will the change be qualified?

The new version of the new M95010, M95020, M95040, M95080 and M95160 in CMOSF8H will be qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.

The **Qualification Reports are** available and included inside this document:

- **QRMMY1316** for **M95020**
- **QRMMY1315** for **M95040**
- **QRMMY1314** for **M95080**
- **QRMMY1205** for **M95160**

The **Qualification report QRMMY1324** for **M95010** will be available Week 50.

What is the impact of the change?

- Form: Marking change (see **Device marking** paragraph)

- Fit: No change

- Function: DC characteristic: I_{CC1} standby supply current:

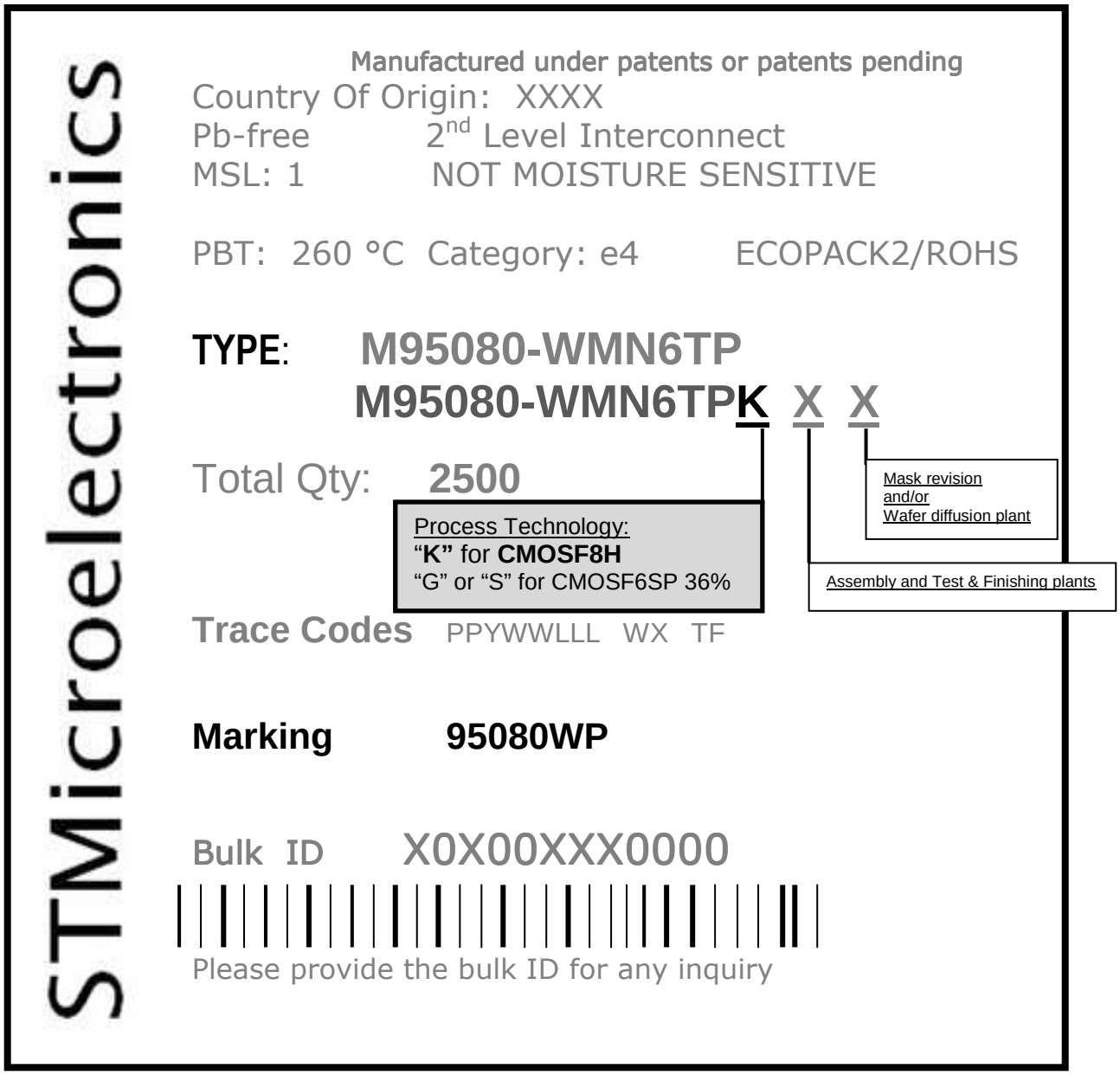
- Max 2 µA at V_{CC} = 2.5 V
- Max 3 µA at V_{CC} = 5.5 V

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **process technology** identifier is "K" for the **upgraded version** in **CMOSF8H**, this identifier being "G" or "S" for the current version in CMOSF6SP 36%.

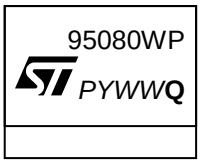
➔ *Example for M95080-WMN6TP*



How can the change be seen?

- DEVICE MARKING

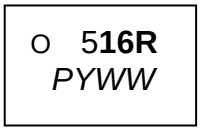
For the **SO8N** package, the difference is visible inside the trace code (*PYWWT*) where the last digit *T* for process technology is "**K**" for the **upgraded version** in **CMOSF8H**, this digit being "Q" for current version.

	Upgraded CMOSF8H (ST Rousset)	Current CMOSF6SP 36% **(ST Ang Mo Kio or GLOBALFOUNDRIES)**
SO8N Example: M95080-WMN6TP		

For the **TSSOP8** package, the difference is visible inside the product name where the last digit is "K" for the **upgraded version** in **CMOSF8H,** this digit being "P" for current version.

	Upgraded CMOSF8H (ST Rousset)	Current CMOSF6SP 36% **(ST Ang Mo Kio or GLOBALFOUNDRIES)**
TSSOP8 Example: M95080-WDW6TP		

For the **UFDFPN8** package, the difference is visible inside the product name: **upgraded version** in **CMOSF8H** is **5DRK**, current version is 516R.

	Upgraded CMOSF8H (ST Rousset)	Current CMOSF6SP 36% **(ST Ang Mo Kio or GLOBALFOUNDRIES)**
UFDFPN8 Example: M95160-RMC6TG		

Appendix A- Product Change Information

Product family / Commercial products:	1-Kbit, 2-Kbit, 4-Kbit, 8-Kbit, 16-Kbit SPI bus EEPROM / Industrial grade
Customer(s):	All
Type of change:	Wafer fab process technology change
Reason for the change:	Line up to state-of-the-art of process
Description of the change:	Redesign and upgrade to the new CMOSF8H Process technology.
Forecast date of the change: (Notification to customer)	Week 41 / 2013
Forecast date of Qualification samples availability for customer(s):	See details in APPENDIX B
Forecast date for the internal STMicroelectronics change, Qualification Report availability:	The **Qualification Reports** are available and included inside this document. The **Qualification report QRMMY1324** for **M95010** will be available Week 50.)
Marking to identify the changed product:	Process Technology identifier "K**"** for CMOSF8H for SO8N.
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See Appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 02 / 2014

Appendix B: Concerned Commercial Part Numbers:

Commercial Part Numbers	Package	Samples availability
M95010-RDW6TP	TSSOP8	December 2013
M95010-RMN6TP	SO8N	December 2013
M95010-WDW6TP	TSSOP8	December 2013
M95010-WMN6P	SO8N	December 2013
M95010-WMN6TP	SO8N	December 2013
M95020-RDW6TP	TSSOP8	November 2013
M95020-RMN6TP	SO8N	November 2013
M95020-WDW6TP	TSSOP8	November 2013
M95020-WMN6P	SO8N	November 2013
M95020-WMN6TP	SO8N	November 2013
5C.P2A02.013	SO8N	October 2013
M95040-RDW6TP	TSSOP8	October 2013
M95040-RMC6TG	UFDFPN8	October 2013
M95040-RMN6TP	SO8N	October 2013
M95040-WDW6TP	TSSOP8	October 2013
M95040-WMN6P	SO8N	October 2013
M95040-WMN6TP	SO8N	October 2013
M95080-RDW6TP	TSSOP8	October 2013
M95080-RMC6TG	UFDFPN8	October 2013
M95080-WDW6TP	TSSOP8	October 2013
M95080-WMN6P	SO8N	October 2013
M95080-WMN6TP	SO8N	October 2013
M95160-RDW6TP	TSSOP8	October 2013
M95160-RMC6TG	UFDFPN8	October 2013
M95160-RMN6TP	SO8N	October 2013
M95160-WDW6TP	TSSOP8	October 2013
M95160-WMN6P	SO8N	October 2013
M95160-WMN6TP	SO8N	October 2013

Appendix C: Qualification Reports:

See following pages

QRMMY1316
Qualification report

New design / M95020-R M95020-W M95020-A125 M95020-A145 using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M95020-RMN6TP M95020-RDW6TP M95020-WDW6TP M95020-WMN6P M95020-WMN6TP
Product description	2 Kbit serial SPI bus EEPROMs with high-speed clock
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8”, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore Subcontractor Ardentec, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M95020-W, M95020-R, M95020-A125 and M95020-A145 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The CMOSF8H is a new advanced silicon process technology that is already qualified in the ST Rousset 8” fab, and in production for M24M02/M95M02, M24M01/M95M01, M24512/M95512, M24256/M95256, M24128/M95128, M24C64/M95640, M24C32/M95320, M95160, M95080 and M95040 EEPROM general purpose products.

The CMOSF8H technology is also qualified for automotive grade using M95640-A125 and M95640-A145 as driver products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for M95020-W devices
- 1.8 to 5.5 V at –40 to 85 °C for M95020-R devices
- 1.8 to 5.5 V at –40 to 125 °C for M95020-A125 devices (automotive grade 1)
- 2.5 to 5.5 V at –40 to 145 °C for M95020-A145 devices (automotive grade 0)

1.2 Conclusion

The new design M95020-W, M95020-R using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab have passed all the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details.

The reliability test results apply also to M95020-A125 and M95020-A145 devices which are forecasted to be fully qualified at completion of 2000 hours stress (Week 47’2013).

2 Device characteristics

The new design M95020-W, M95020-R, M95020-A125 and M95020-A145 are electrically erasable programmable memory (EEPROM) devices based on advanced true EEPROM technology.

The M95020-W, M95020-R, M95020-A125 and M95020-A145 are byte-alterable memories (256 × 8 bits) organized as 16 pages of 16 bytes in which the data integrity is significantly improved with an embedded Error Correction Code logic.

The devices are accessed by a simple serial SPI compatible interface.

The M95020 devices can operate with a supply range from 1.8 V up to 5.5 V, and are guaranteed over the -40 °C/+85 °C temperature range.

The M95020-A125 and M95020-A145 are 2-Kbit serial EEPROM Automotive grade devices operating up to 125 °C and 145 °C respectively. They are compliant with the very high level of reliability defined by the Automotive standard AEC-Q100 grade 0.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The CMOSF8H process technology and EEPROM new design core have been qualified for Automotive products on 3 lots using the driver product M95640 (refer to qualification report QREE0921).

The M95020 is designed with the same technology and similar architecture as the driver product M95640/M95160.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95020 / M95160	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.

The product vehicles used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95020 / M95160 (1)(2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
			TSSOP8	ST Shenzhen
M95640 (2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
			TSSOP8	ST Shenzhen
M24C64 (2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen / subcon Amkor
			TSSOP8	ST Shenzhen / subcon Amkor
			UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / subcon Amkor

1. Qualification on 3 lots using the product driver M95640 - Qualification of M95160/M95020 benefits of the family approach (1 lot).
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M95640/M24C64/M95160 are applicable to M95020.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M95020		
						Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	400K E/W cycles at 150 °C then: HTOL 150 °C, 6 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	0/80	Results W47
	Data retention after endurance							
	AEC-Q100-005	400K E/W cycles at 150 °C then: HTSL at 150 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	Results W39	Results W47
LTOL	Low temperature operating life							
	JESD22-A108	–40 °C, 6 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	Results W39	Results W47

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1) (continued)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M95020		
						Lot 1	Lot 2	Lot 3
HTSL	High temperature storage life							
	AEC-Q100-005 JESD22-A103	Retention bake at 200 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	Results W39	Results W41
					2008 hrs	0/80	Results W46	Results W47
WEB	Program/erase endurance cycling + bake							
	Internal spec.	5 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	5 Million cycles / 48 hrs	0/80 (2)	0/80 (2)	0/80 (2)
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω	27	3	N/A	Pass 4000 V	Pass 4000 V	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	12	3	N/A	Pass 400 V	Pass 400 V	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	3	N/A	Class II - Level A	Class II - Level A	Class II - Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. First rejects after 10 million E/W cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95640			M95160 (2)(3)
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1280	1	N/A	0/1280	0/1280	0/1280	0/1280
THB (4)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
TC (4)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80	0/80	0/80	0/80
TMSK (4)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	1	200 shocks	0/80	0/80	0/80	0/80
AC (4)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	240 hrs	0/80	0/80	0/80	0/80
HTSL (4)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
HTOL (4)	High temperature operating life								
	AEC-Q100-JESD22-A108	HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W41
ELFR (4)	Early life failure rate								
	AEC-Q100-008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the product driver M95640 - Qualification of M95160 benefits of the family approach (1 lot).
3. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M95160 are applicable to M95020.
4. THB-, TC-, TMSK-, AC-, HTSL-, HTOL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95640			M95160 (2)(3)
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1280	1	N/A	0/1280	0/1280	0/1280	0/1280
THB (4)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W39
TC (4)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80	0/80	0/80	0/80
TMSK (4)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	1	200 shocks	0/80	0/80	0/80	0/80
AC (4)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	240 hrs	0/80	0/80	0/80	0/80
HTSL (4)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W39
HTOL (4)	High temperature operating life								
	AEC-Q100-JESD22-A108	HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W41
ELFR (4)	Early life failure rate								
	AEC-Q100-008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the product driver M95640 - Qualification of M95160 benefits of the family approach (1 lot).
3. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M95160 are applicable to M95020.
4. THB-, TC-, TMSK-, AC-, HTSL-, HTOL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 (MLP8) 2 x 3 mm / ST Calamba) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C64 (2)			M95020
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1200	3	N/A	0/1200	0/1200	0/1200	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	-
					1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	100 cycles	0/80	0/80	0/80	-
					500 cycles	0/80	0/80	0/80	-
					1000 cycles	0/80	0/80	0/80	-
			800	3	200 cycles	0/800	0/800	0/800	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	-
					1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Results W45

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24C64 are applicable to M95020.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
17-Sep-2013	1	Initial release.

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QRMMY1315
Qualification report

New design / M95040-R M95040-W M95040-DF M95040-A125 M95040-A145 using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M95040-DFDW6TP M95040-DFMN6TP M95040-RMN6TP M95040-RDW6TP M95040-WDW6TP M95040-WMN6P M95040-WMN6TP
Product description	4 Kbit serial SPI bus EEPROMs with high-speed clock
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8”, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore Subcontractor Ardentec, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M95040-W, M95040-R, M95040-DF, M95040-A125 and M95040-A145 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The CMOSF8H is a new advanced silicon process technology that is already qualified in the ST Rousset 8” fab, and in production for M24M02/M95M02, M24M01/M95M01, M24512/M95512, M24256/M95256, M24128/M95128, M24C64/M95640, M24C32/M95320, M95160 and M95080 EEPROM general purpose products.

The CMOSF8H technology is also qualified for automotive grade using M95640-A125 and M95640-A145 as driver products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for M95040-W devices
- 1.8 to 5.5 V at –40 to 85 °C for M95040-R devices
- 1.7 to 5.5 V at –40 to 85 °C for M95040-DF devices
- 1.8 to 5.5 V at –40 to 125 °C for M95040-A125 devices (automotive grade 1)
- 2.5 to 5.5 V at –40 to 145 °C for M95040-A145 devices (automotive grade 0)

1.2 Conclusion

The new design M95040-W, M95040-R, M95040-DF using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab have passed all the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details.

The reliability test results apply also to M95040-A125 and M95040-A145 devices which are forecasted to be fully qualified at completion of 2000 hours stress (Week 47’2013).

2 Device characteristics

The new design M95040-W, M95040-R, M95040-DF, M95040-A125 and M95040-A145 are electrically erasable programmable memory (EEPROM) devices based on advanced true EEPROM technology.

The M95040-W, M95040-R, M95040-DF, M95040-A125 and M95040-A145 are byte-alterable memories (512 × 8 bits) organized as 32 pages of 16 bytes in which the data integrity is significantly improved with an embedded Error Correction Code logic.

The devices are accessed by a simple serial SPI compatible interface.

The M95040 devices can operate with a supply range from 1.7 V up to 5.5 V, and are guaranteed over the -40 °C/+85 °C temperature range.

The M95040-DF offers an additional page, named the identification page (16 bytes). The identification page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

The M95040-A125 and M95040-A145 are 4-Kbit serial EEPROM Automotive grade devices operating up to 125 °C and 145 °C respectively. They are compliant with the very high level of reliability defined by the Automotive standard AEC-Q100 grade 0.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The CMOSF8H process technology and EEPROM new design core have been qualified for Automotive products on 3 lots using the driver product M95640 (refer to qualification report QREE0921).

The M95040 is designed with the same technology and similar architecture as the driver product M95640/M95160.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95040 / M95160	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.

The product vehicles used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95040 / M95160 (1)(2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
			TSSOP8	ST Shenzhen
M95640 (2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
			TSSOP8	ST Shenzhen
M24C64 (2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen / subcon Amkor
			TSSOP8	ST Shenzhen / subcon Amkor
			UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / subcon Amkor

1. Qualification on 3 lots using the product driver M95640 - Qualification of M95160/M95040 benefits of the family approach (1 lot).
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M95640/M24C64/M95160 are applicable to M95040.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M95040		
						Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	400K E/W cycles at 150 °C then: HTOL 150 °C, 6 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	0/80	Results W47
	Data retention after endurance							
	AEC-Q100-005	400K E/W cycles at 150 °C then: HTSL at 150 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	Results W39	Results W47
LTOL	Low temperature operating life							
	JESD22-A108	–40 °C, 6 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	Results W39	Results W47

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1) (continued)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M95040		
						Lot 1	Lot 2	Lot 3
HTSL	High temperature storage life							
	AEC-Q100-005 JESD22-A103	Retention bake at 200 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	Results W39	Results W41
					2008 hrs	0/80	Results W46	Results W47
WEB	Program/erase endurance cycling + bake							
	Internal spec.	5 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	5 Million cycles / 48 hrs	0/80 (2)	0/80 (2)	0/80 (2)
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω	27	3	N/A	Pass 4000 V	Pass 4000 V	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	12	3	N/A	Pass 400 V	Pass 400 V	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	3	N/A	Class II - Level A	Class II - Level A	Class II - Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. First rejects after 10 million E/W cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95640			M95160 (2)(3)
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1280	1	N/A	0/1280	0/1280	0/1280	0/1280
THB (4)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
TC (4)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80	0/80	0/80	0/80
TMSK (4)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	1	200 shocks	0/80	0/80	0/80	0/80
AC (4)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	240 hrs	0/80	0/80	0/80	0/80
HTSL (4)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
HTOL (4)	High temperature operating life								
	AEC-Q100-JESD22-A108	HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W41
ELFR (4)	Early life failure rate								
	AEC-Q100-008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the product driver M95640 - Qualification of M95160 benefits of the family approach (1 lot).
3. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M95160 are applicable to M95040.
4. THB-, TC-, TMSK-, AC-, HTSL-, HTOL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95640			M95160 (2)(3)
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1280	1	N/A	0/1280	0/1280	0/1280	0/1280
THB (4)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W39
TC (4)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80	0/80	0/80	0/80
TMSK (4)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	1	200 shocks	0/80	0/80	0/80	0/80
AC (4)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	240 hrs	0/80	0/80	0/80	0/80
HTSL (4)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W39
HTOL (4)	High temperature operating life								
	AEC-Q100-JESD22-A108	HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W41
ELFR (4)	Early life failure rate								
	AEC-Q100-008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the product driver M95640 - Qualification of M95160 benefits of the family approach (1 lot).
3. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M95160 are applicable to M95040.
4. THB-, TC-, TMSK-, AC-, HTSL-, HTOL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 (MLP8) 2 x 3 mm / ST Calamba) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C64 (2)			M95040
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1200	3	N/A	0/1200	0/1200	0/1200	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	-
					1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	100 cycles	0/80	0/80	0/80	-
					500 cycles	0/80	0/80	0/80	-
					1000 cycles	0/80	0/80	0/80	-
			800	3	200 cycles	0/800	0/800	0/800	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	-
					1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Results W45

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24C64 are applicable to M95040.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
19-Sep-2013	1	Initial release.

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QRMMY1314
Qualification report

New design / M95080-R M95080-W M95080-DF M95080-A125 M95080-A145 using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M95080-DFDW6TP M95080-DFMN6TP M95080-RMN6TP M95080-RDW6TP M95080-WDW6TP M95080-WMN6P M95080-WMN6TP
Product description	8 Kbit serial SPI bus EEPROMs with high-speed clock
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8”, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore Subcontractor Ardentec, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M95080-W, M95080-R, M95080-DF, M95080-A125 and M95080-A145 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The CMOSF8H is a new advanced silicon process technology that is already qualified in the ST Rousset 8” fab, and in production for M24M02/M95M02, M24M01/M95M01, M24512/M95512, M24256/M95256, M24128/M95128, M24C64/M95640, M24C32/M95320 and M95160 EEPROM general purpose products.

The CMOSF8H technology is also qualified for automotive grade using M95640-A125 and M95640-A145 as driver products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for M95080-W devices
- 1.8 to 5.5 V at –40 to 85 °C for M95080-R devices
- 1.7 to 5.5 V at –40 to 85 °C for M95080-DF devices
- 1.8 to 5.5 V at –40 to 125 °C for M95080-A125 devices (automotive grade 1)
- 2.5 to 5.5 V at –40 to 145 °C for M95080-A145 devices (automotive grade 0)

1.2 Conclusion

The new design M95080-W, M95080-R, M95080-DF using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab have passed all the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details.

The reliability test results apply also to M95080-A125 and M95080-A145 devices which are forecasted to be fully qualified at completion of 2000 hours stress (Week 47’2013).

2 Device characteristics

The new design M95080-W, M95080-R, M95080-DF, M95080-A125 and M95080-A145 are electrically erasable programmable memory (EEPROM) devices based on advanced true EEPROM technology.

The M95080-W, M95080-R, M95080-DF, M95080-A125 and M95080-A145 are byte-alterable memories (1024 × 8 bits) organized as 32 pages of 32 bytes in which the data integrity is significantly improved with an embedded Error Correction Code logic.

The devices are accessed by a simple serial SPI compatible interface.

The M95080 devices can operate with a supply range from 1.7 V up to 5.5 V, and are guaranteed over the -40 °C/+85 °C temperature range.

The M95080-DF offers an additional page, named the identification page (32 bytes). The identification page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

The M95080-A125 and M95080-A145 are 8-Kbit serial EEPROM Automotive grade devices operating up to 125 °C and 145 °C respectively. They are compliant with the very high level of reliability defined by the Automotive standard AEC-Q100 grade 0.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The CMOSF8H process technology and EEPROM new design core have been qualified for Automotive products on 3 lots using the driver product M95640 (refer to qualification report QREE0921).

The M95080 is designed with the same technology and similar architecture as the driver product M95640/M95160.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95080 / M95160	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.

The product vehicles used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95080 / M95160 (1)(2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
			TSSOP8	ST Shenzhen
M95640 (2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
			TSSOP8	ST Shenzhen
M24C64 (2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen / subcon Amkor
			TSSOP8	ST Shenzhen / subcon Amkor
			UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / subcon Amkor

1. Qualification on 3 lots using the product driver M95640 - Qualification of M95160/M95080 benefits of the family approach (1 lot).
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M95640/M24C64/M95160 are applicable to M95080.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M95080		
						Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	400K E/W cycles at 150 °C then: HTOL 150 °C, 6 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	0/80	Results W47
	Data retention after endurance							
	AEC-Q100-005	400K E/W cycles at 150 °C then: HTSL at 150 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	Results W39	Results W47
LTOL	Low temperature operating life							
	JESD22-A108	–40 °C, 6 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	Results W39	Results W47

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1) (continued)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M95080		
						Lot 1	Lot 2	Lot 3
HTSL	High temperature storage life							
	AEC-Q100-005 JESD22-A103	Retention bake at 200 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	Results W39	Results W41
					2008 hrs	0/80	Results W46	Results W47
WEB	Program/erase endurance cycling + bake							
	Internal spec.	5 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	5 Million cycles / 48 hrs	0/80 (2)	0/80 (2)	0/80 (2)
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω	27	3	N/A	Pass 4000 V	Pass 4000 V	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	12	3	N/A	Pass 400 V	Pass 400 V	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	3	N/A	Class II - Level A	Class II - Level A	Class II - Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. First rejects after 10 million E/W cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95640			M95160 (2)(3)
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1280	1	N/A	0/1280	0/1280	0/1280	0/1280
THB (4)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
TC (4)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80	0/80	0/80	0/80
TMSK (4)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	1	200 shocks	0/80	0/80	0/80	0/80
AC (4)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	240 hrs	0/80	0/80	0/80	0/80
HTSL (4)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
HTOL (4)	High temperature operating life								
	AEC-Q100-JESD22-A108	HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W41
ELFR (4)	Early life failure rate								
	AEC-Q100-008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the product driver M95640 - Qualification of M95160 benefits of the family approach (1 lot).
3. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M95160 are applicable to M95080.
4. THB-, TC-, TMSK-, AC-, HTSL-, HTOL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95640			M95160 (2)(3)
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1280	1	N/A	0/1280	0/1280	0/1280	0/1280
THB (4)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W39
TC (4)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80	0/80	0/80	0/80
TMSK (4)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	1	200 shocks	0/80	0/80	0/80	0/80
AC (4)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	240 hrs	0/80	0/80	0/80	0/80
HTSL (4)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W39
HTOL (4)	High temperature operating life								
	AEC-Q100-JESD22-A108	HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W41
ELFR (4)	Early life failure rate								
	AEC-Q100-008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the product driver M95640 - Qualification of M95160 benefits of the family approach (1 lot).
3. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M95160 are applicable to M95080.
4. THB-, TC-, TMSK-, AC-, HTSL-, HTOL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 (MLP8) 2 x 3 mm / ST Calamba) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C64 (2)			M95080
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1200	3	N/A	0/1200	0/1200	0/1200	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	-
					1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	100 cycles	0/80	0/80	0/80	-
					500 cycles	0/80	0/80	0/80	-
					1000 cycles	0/80	0/80	0/80	-
			800	3	200 cycles	0/800	0/800	0/800	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	-
					1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Results W45

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24C64 are applicable to M95080.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
17-Sep-2013	1	Initial release.

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QRMMY1205
Qualification report

New design / M95160-R M95160-W M95160-DF M95160-A125 M95160-A145 using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M95160-DFDW6TP M95160-DFMN6TP M95160-RMN6TP M95160-RDW6TP M95160-WDW6TP M95160-WMN6P M95160-WMN6TP
Product description	16 Kbit serial SPI bus EEPROMs with high-speed clock
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8”, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore Subcontractor Ardentec, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M95160-W, M95160-R, M95160-DF, M95160-A125 and M95160-A145 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The CMOSF8H is a new advanced silicon process technology that is already qualified in the ST Rousset 8” fab, and in production for M24M02/M95M02, M24M01/M95M01, M24512/M95512, M24256/M95256, M24128/M95128, M24C64/M95640 and M24C32/M95320 EEPROM general purpose products.

The CMOSF8H technology is also qualified for automotive grade using M95640-A125 and M95640-A145 as driver products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for M95160-W devices
- 1.8 to 5.5 V at –40 to 85 °C for M95160-R devices
- 1.7 to 5.5 V at –40 to 85 °C for M95160-DF devices
- 1.8 to 5.5 V at –40 to 125 °C for M95160-A125 devices (automotive grade 1)
- 2.5 to 5.5 V at –40 to 145 °C for M95160-A145 devices (automotive grade 0)

1.2 Conclusion

The new design M95160-W, M95160-R, M95160-DF using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab have passed all the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details.

The reliability test results apply also to M95160-A125 and M95160-A145 devices which are forecasted to be fully qualified at completion of 2000 hours stress (Week 47’2013).

2 Device characteristics

The new design M95160-W, M95160-R, M95160-DF, M95160-A125 and M95160-A145 are electrically erasable programmable memory (EEPROM) devices based on advanced true EEPROM technology.

The M95160-W, M95160-R, M95160-DF, M95160-A125 and M95160-A145 are byte-alterable memories (2048 × 8 bits) organized as 64 pages of 32 bytes in which the data integrity is significantly improved with an embedded Error Correction Code logic.

The devices are accessed by a simple serial SPI compatible interface.

The M95160 devices can operate with a supply range from 1.7 V up to 5.5 V, and are guaranteed over the -40 °C/+85 °C temperature range.

The M95160-DF offers an additional page, named the identification page (32 bytes). The identification page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

The M95160-A125 and M95160-A145 are 16-Kbit serial EEPROM Automotive grade devices operating up to 125 °C and 145 °C respectively. They are compliant with the very high level of reliability defined by the Automotive standard AEC-Q100 grade 0.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The CMOSF8H process technology and EEPROM new design core have been qualified for Automotive products on 3 lots using the driver product M95640 (refer to qualification report QREE0921).

The M95160, driver product for SPI low densities EEPROM, is designed with the same technology and similar architecture as the driver product M95640.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95160	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.

The product vehicles used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95160 (1)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
			TSSOP8	ST Shenzhen
M95640 (2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
			TSSOP8	ST Shenzhen
M24C64 (2)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen / subcon Amkor
			TSSOP8	ST Shenzhen / subcon Amkor
			UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / subcon Amkor

1. Qualification on 3 lots using the driver product M95640 - Qualification of M95160 benefits of the family approach (1 lot).
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M95640/M24C64 are applicable to M95160.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M95160		
						Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	400K E/W cycles at 150 °C then: HTOL 150 °C, 6 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	0/80	Results W47
	Data retention after endurance							
	AEC-Q100-005	400K E/W cycles at 150 °C then: HTSL at 150 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	Results W39	Results W47
LTOL	Low temperature operating life							
	JESD22-A108	–40 °C, 6 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	Results W41
					2008 hrs	0/80	Results W39	Results W47

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1) (continued)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M95160		
						Lot 1	Lot 2	Lot 3
HTSL	High temperature storage life							
	AEC-Q100-005 JESD22-A103	Retention bake at 200 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	Results W39	Results W41
					2008 hrs	0/80	Results W46	Results W47
WEB	Program/erase endurance cycling + bake							
	Internal spec.	5 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	5 Million cycles / 48 hrs	0/80 (2)	0/80 (2)	0/80 (2)
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω	27	3	N/A	Pass 4000 V	Pass 4000 V	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	12	3	N/A	Pass 400 V	Pass 400 V	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	3	N/A	Class II - Level A	Class II - Level A	Class II - Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. First rejects after 10 million E/W cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95640			M95160 (2)
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1280	1	N/A	0/1280	0/1280	0/1280	0/1280
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80	0/80	0/80	0/80
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	1	200 shocks	0/80	0/80	0/80	0/80
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	240 hrs	0/80	0/80	0/80	0/80
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
HTOL (3)	High temperature operating life								
	AEC-Q100-JESD22-A108	HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W41
ELFR (3)	Early life failure rate								
	AEC-Q100-008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the driver product M95640 - Qualification of M95160 benefits of the family approach (1 lot).
3. THB-, TC-, TMSK-, AC-, HTSL-, HTOL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95640			M95160 (2)
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1280	1	N/A	0/1280	0/1280	0/1280	0/1280
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W39
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80	0/80	0/80	0/80
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	1	200 shocks	0/80	0/80	0/80	0/80
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	240 hrs	0/80	0/80	0/80	0/80
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W39
HTOL (3)	High temperature operating life								
	AEC-Q100-JESD22-A108	HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	Results W41
ELFR (3)	Early life failure rate								
	AEC-Q100-008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the driver product M95640 - Qualification of M95160 benefits of the family approach (1 lot).
3. THB-, TC-, TMSK-, AC-, HTSL-, HTOL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 (MLP8) 2 x 3 mm / ST Calamba) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C64 (2)			M95160
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1200	3	N/A	0/1200	0/1200	0/1200	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	-
					1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	100 cycles	0/80	0/80	0/80	-
					500 cycles	0/80	0/80	0/80	-
					1000 cycles	0/80	0/80	0/80	-
			800	3	200 cycles	0/800	0/800	0/800	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	-
					1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Results W45

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24C64 are applicable to M95160.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
13-Sep-2013	1	Initial release.

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Document Revision History

Date	Rev.	Description of the Revision
September 17, 2013	1.00	First draft creation

Source Documents & Reference Documents

Source document Title	**Rev.:**	**Date:**

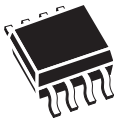
M95160 M95160-W
M95160-R M95160-F

16-Kbit serial SPI bus EEPROM with high-speed clock

Datasheet – production data

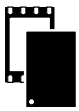
Features

- Compatible with the Serial Peripheral Interface (SPI) bus
- Memory array
  - 16 Kb (2 Kbytes) of EEPROM
  - Page size: 32 bytes
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Write Protect: quarter, half or whole memory array
- High-speed clock: 10 MHz
- Single supply voltage:
  - 4.5 V to 5.5 V for M95160
  - 2.5 V to 5.5 V for M95160-W
  - 1.8 V to 5.5 V for M95160-R
  - 1.7 V to 5.5 V for M95160-F
- Operating temperature range: from -40°C up to +85°C
- Enhanced ESD protection
- More than 1 million Write cycles
- More than 40-year data retention
- Packages
  - RoHS compliant and halogen-free (ECOPACK®)



SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width



UFDFPN8 (MC)
2 x 3 mm (MLP)

WLCSP (CS)
(preliminary data)

Contents

List of tables

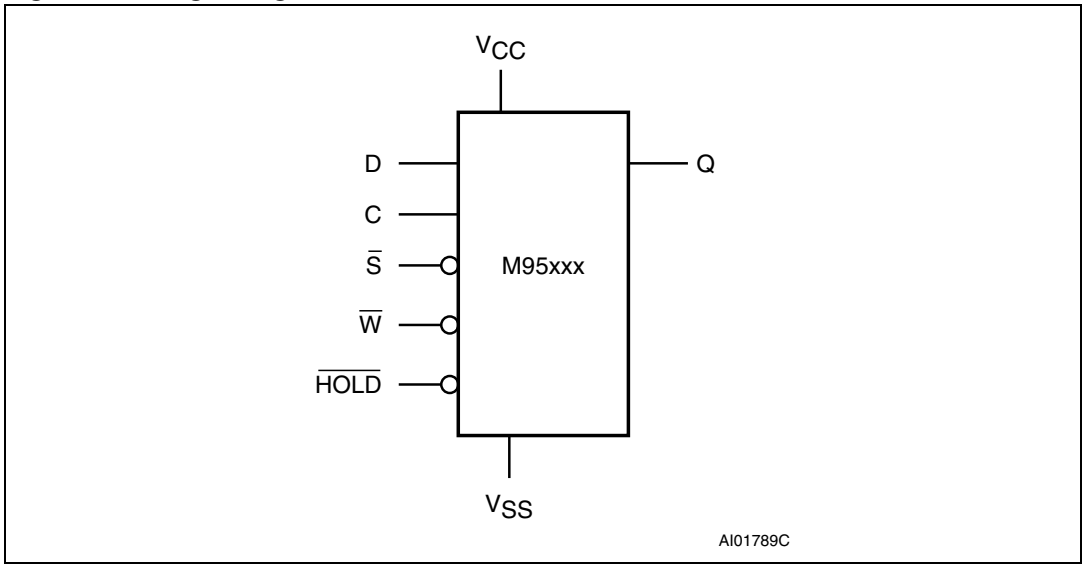
List of figures

1 Description

The M95160 devices are Electrically Erasable PROgrammable Memories (EEPROMs) organized as 2048 x 8 bits, accessed through the SPI bus.

The M95160 can operate with a supply voltage from 4.5 V to 5.5 V, the M95160-W can operate with a supply voltage from 2.5 V to 5.5 V, the M95160-R can operate with a supply voltage from 1.8 V to 5.5 V, and the M95160-F can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C / +85 °C.

Figure 1. Logic diagram

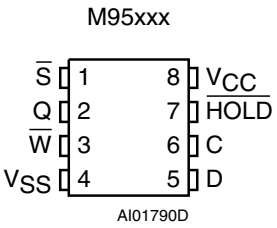


The SPI bus signals are C, D and Q, as shown in *Figure 1* and *Table 1*. The device is selected when Chip Select ($\overline{S}$) is driven low. Communications with the device can be interrupted when the $\overline{HOLD}$ is driven low.

Table 1. Signal names

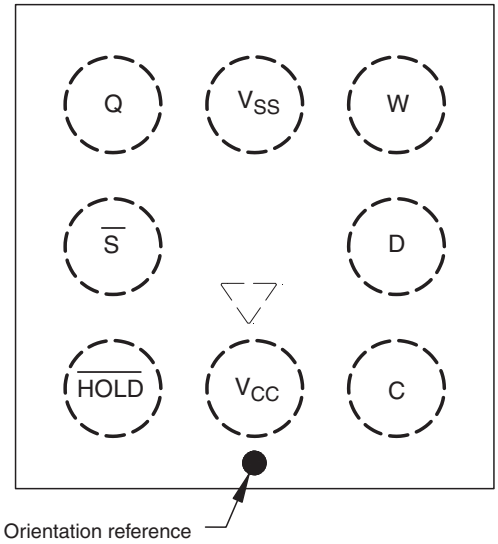
Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data Input	Input
Q	Serial Data Output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. 8-pin package connections (top view)



1. See *Section 10: Package mechanical data* section for package dimensions, and how to identify pin 1.

Figure 3. WLCSP connections (top view, marking side, with balls on the underside)

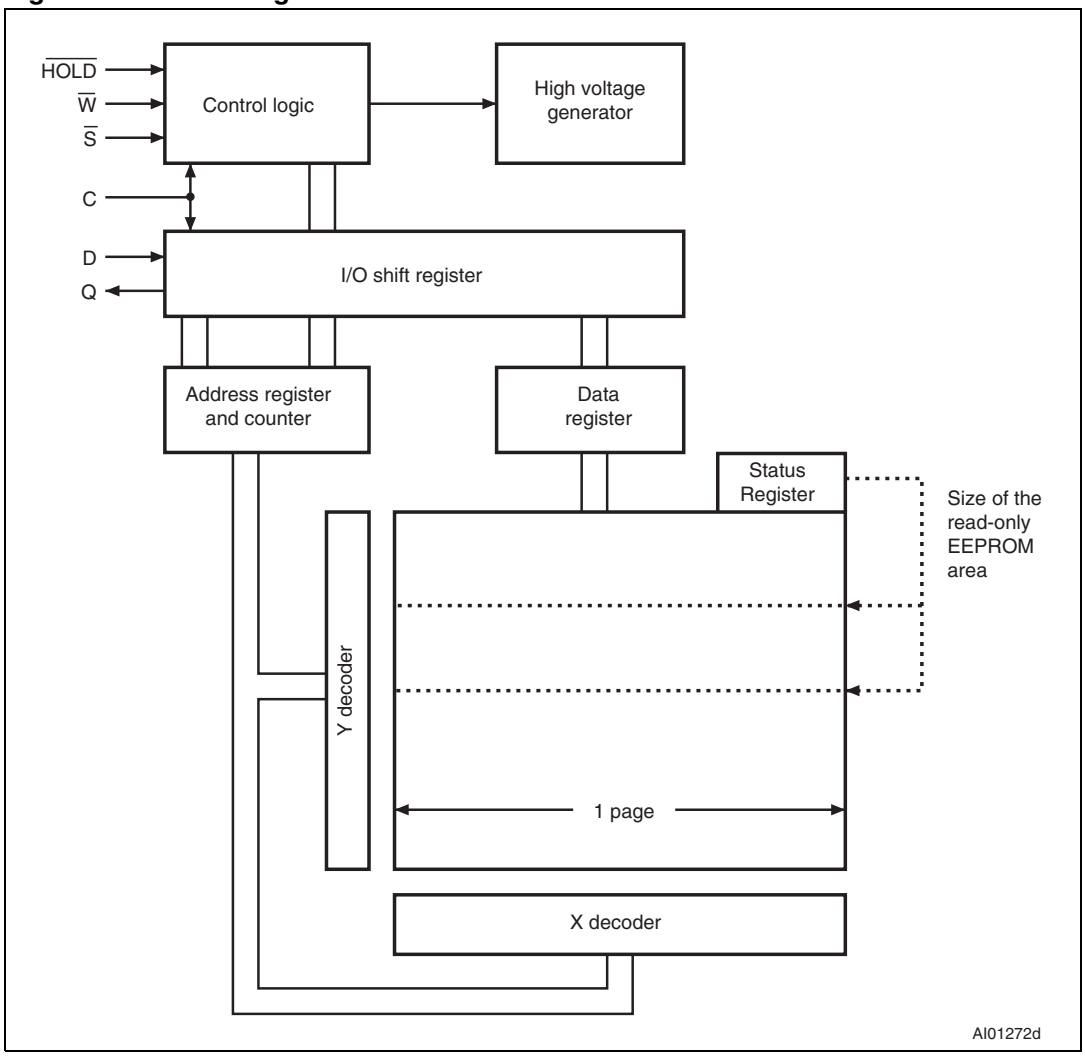


Caution: As EEPROM cells lose their charge (and so their binary value) when exposed to ultra violet (UV) light, EEPROM dice delivered in wafer form or in WLCSP package by STMicroelectronics must never be exposed to UV light.

2 Memory organization

The memory is organized as shown in the following figure.

Figure 4. Block diagram



3 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Section 9: DC and AC parameters*). These signals are described next.

3.1 Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

3.2 Serial Data Input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

3.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) change from the falling edge of Serial Clock (C).

3.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. The device is in the Standby Power mode, unless an internal Write cycle is in progress. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

3.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

3.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all Write instructions.

3.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

3.8 V_{SS} ground

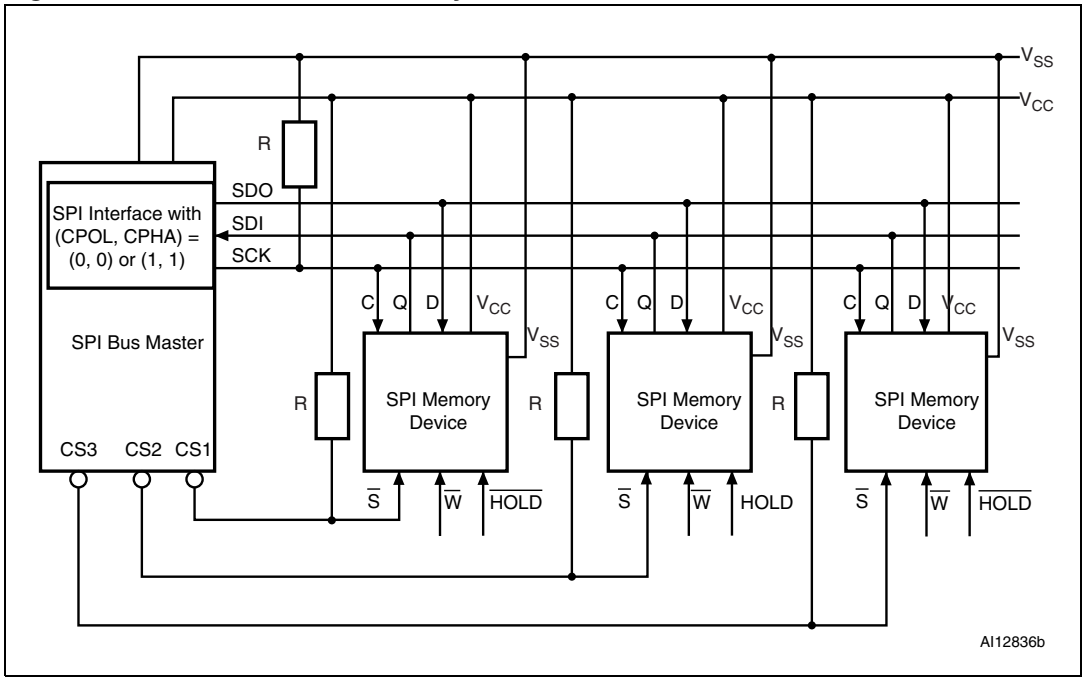
V_{SS} is the reference for all signals, including the V_{CC} supply voltage.

4 Connecting to the SPI bus

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 5. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

Figure 5 shows an example of three memory devices connected to an SPI bus master. Only one memory device is selected at a time, so only one memory device drives the Serial Data Output (Q) line at a time. The other memory devices are high impedance.

The pull-up resistor R (represented in *Figure 5*) ensures that a device is not selected if the Bus Master leaves the $\overline{S}$ line in the high impedance state.

In applications where the Bus Master may leave all SPI bus lines in high impedance at the same time (for example, if the Bus Master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high): this ensures that $\overline{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met. The typical value of R is 100 kΩ.

4.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

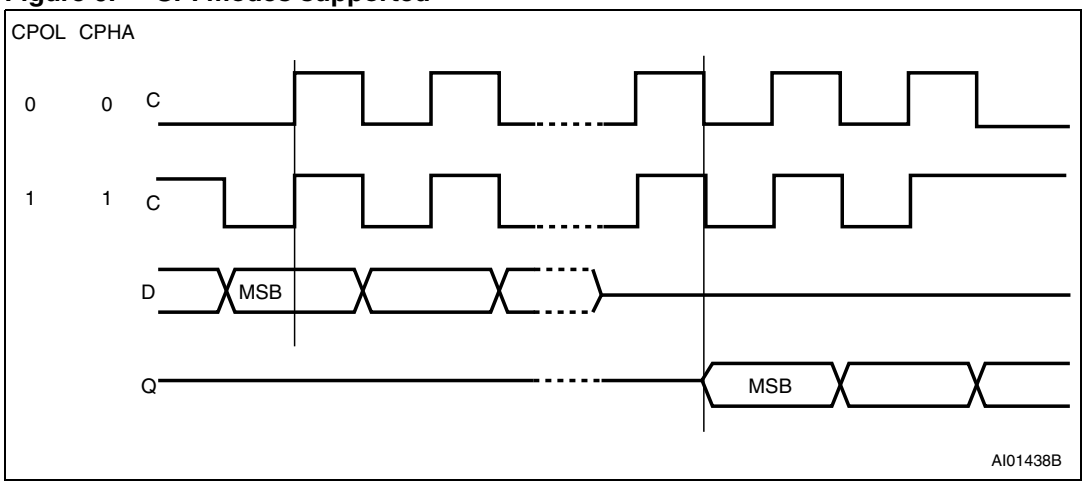
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 6*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 6. SPI modes supported



5 Operating features

5.1 Supply voltage (V_{CC})

5.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 9: DC and AC parameters*). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} device pins.

5.1.2 Device reset

In order to prevent erroneous instruction decoding and inadvertent Write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until VCC reaches the POR threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 9: DC and AC parameters*).

At power-up, when V_{CC} passes over the POR threshold, the device is reset and is in the following state:

- in Standby Power mode,
- deselected,
- Status Register values:
  - The Write Enable Latch (WEL) bit is reset to 0.
  - The Write In Progress (WIP) bit is reset to 0.
  - The SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).

It is important to note that the device must not be accessed until V_{CC} reaches a valid and stable level within the specified [V_{CC}(min), V_{CC}(max)] range, as defined under Operating conditions in *Section 9: DC and AC parameters*.

5.1.3 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 5*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined under Operating conditions in *Section 9: DC and AC parameters*, and the rise time must not vary faster than 1 V/µs.

5.1.4 Power-down

During power-down (continuous decrease of the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined under Operating conditions in *Section 9: DC and AC parameters*), the device must be:

- deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC}),
- in Standby Power mode (there should not be any internal write cycle in progress).

5.2 Active Power and Standby Power modes

When Chip Select ($\overline{S}$) is low, the device is selected, and in the Active Power mode. The device consumes I_{CC}.

When Chip Select ($\overline{S}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes into the Standby Power mode, and the device consumption drops to I_{CC1}, as specified in DC characteristics (see *Section 9: DC and AC parameters*).

5.3 Hold condition

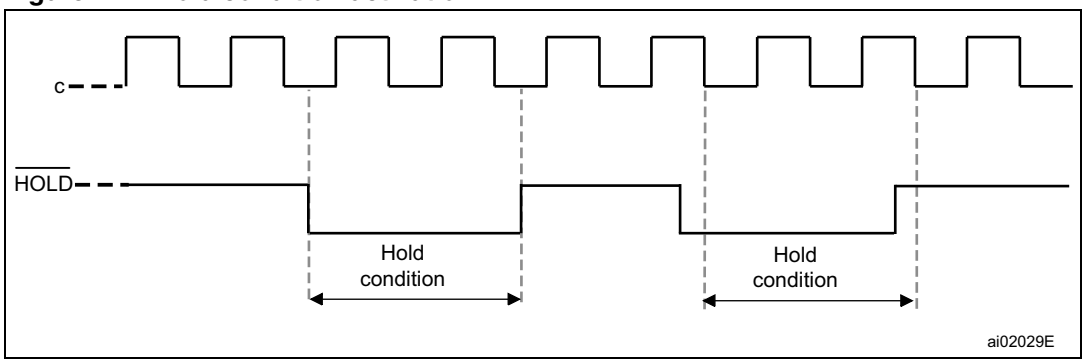
The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) low.

During the Hold condition, the Serial Data Output (Q) is high impedance, and the Serial Data Input (D) and the Serial Clock (C) are Don't Care.

Normally, the device is kept selected for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition has the effect of resetting the state of the device, and this mechanism can be used if required to reset any processes that had been in progress.(a)(b)

Figure 7. Hold condition activation



The Hold condition starts when the Hold (HOLD) signal is driven low when Serial Clock (C) is already low (as shown in *Figure 7*).

a. This resets the internal logic, except the WEL and WIP bits of the Status Register.

b. In the specific case where the device has shifted in a Write command (Inst + Address + data bytes, each data byte being exactly 8 bits), deselecting the device also triggers the Write cycle of this decoded command.

The Hold condition ends when the Hold (HOLD) signal is driven high when Serial Clock (C) is already low.

Figure 7 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

5.4 Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.3: Read Status Register (RDSR)* for a detailed description of the Status Register bits.

5.5 Data protection and protocol control

The device features the following data protection mechanisms:

- Before accepting the execution of the Write and Write Status Register instructions, the device checks whether the number of clock pulses comprised in the instructions is a multiple of eight.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit.
- The Block Protect (BP1, BP0) bits in the Status Register are used to configure part of the memory as read-only.
- The Write Protect ($\overline{W}$) signal is used to protect the Block Protect (BP1, BP0) bits in the Status Register.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points should be noted in the previous sentence:

- The “last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The “next rising edge of Serial Clock (C)” might (or might not) be the next bus transaction for some other device on the SPI bus.

Table 2. Write-protected block size

Status Register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	none	none
0	1	Upper quarter	0600h - 07FFh
1	0	Upper half	0400h - 07FFh
1	1	Whole memory	0000h - 07FFh

6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 3*.

If an invalid instruction is sent (one not contained in *Table 3*), the device automatically deselects itself.

Table 3. Instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

Table 4. Address range bits

Address significant bits	A10-A0(1)

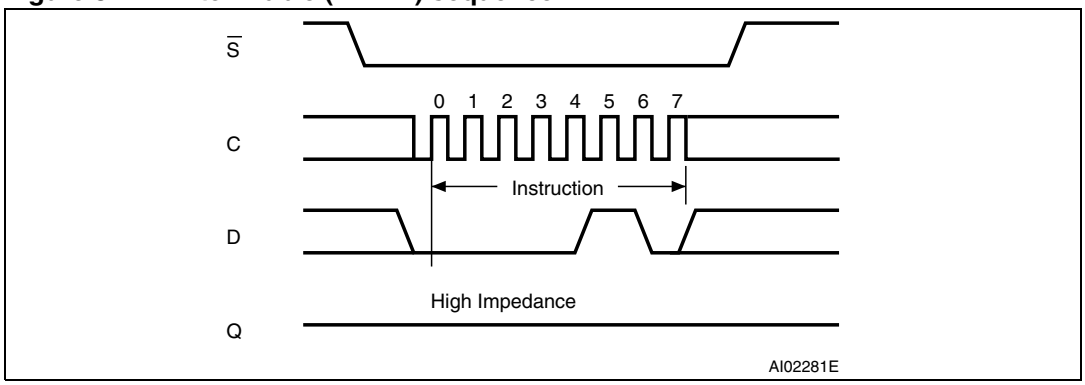
1. Upper MSBs are Don't Care.

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 8*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 8. Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

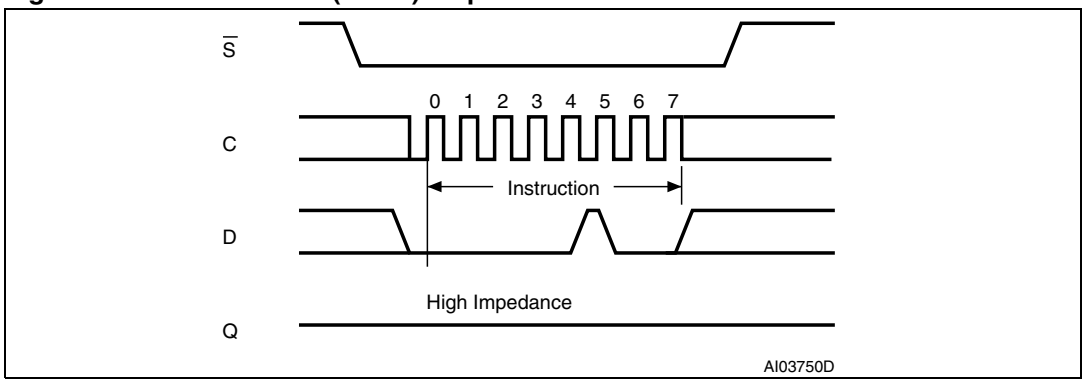
As shown in *Figure 9*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

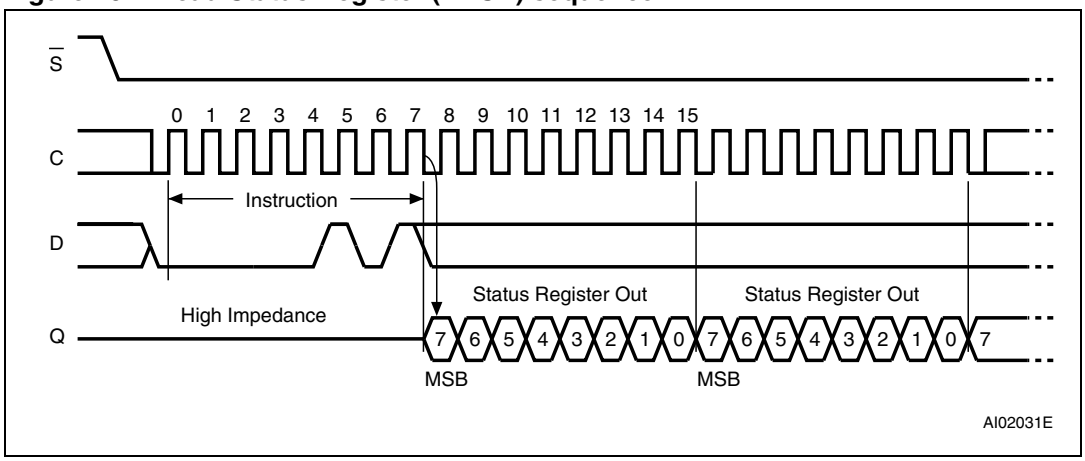
Figure 9. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction is used to read the Status Register. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 10*.

Figure 10. Read Status Register (RDSR) sequence



The status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0, no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set. When set to 0, the internal Write Enable Latch is reset, and no Write or Write Status Register instruction is accepted.

The WEL bit is returned to its reset state by the following events:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Write (WRITE) instruction completion

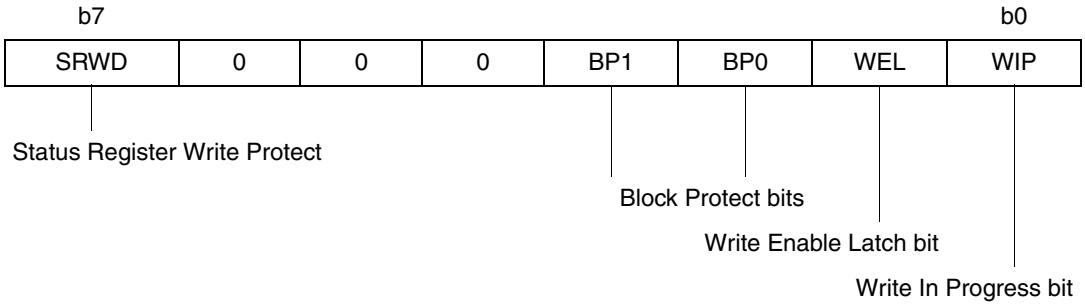
6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non volatile. They define the size of the area to be software-protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 2*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal enable the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 5. Status Register format



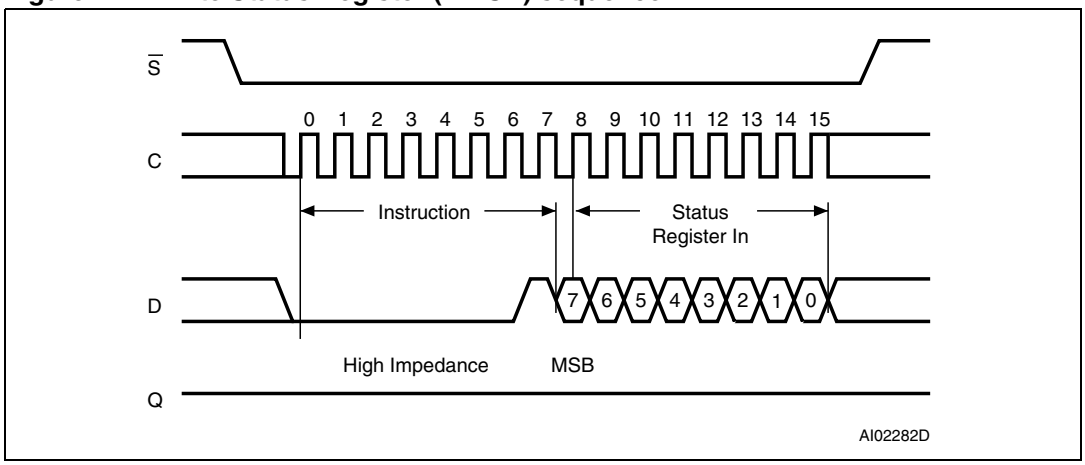
6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction is used to write new values to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must have been previously executed.

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) low, followed by the instruction code, the data byte on Serial Data input (D) and Chip Select ($\overline{S}$) driven high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed.

The instruction sequence is shown in *Figure 11*.

Figure 11. Write Status Register (WRSR) sequence



Driving the Chip Select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed Write cycle that takes t_W to complete (as specified in AC tables under *Section 9: DC and AC parameters*).

While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in progress (WIP) bit: the WIP bit is 1 during the self-timed Write cycle t_W, and 0 when the Write cycle is complete. The WEL bit (Write Enable Latch) is also reset at the end of the Write cycle t_W.

The Write Status Register (WRSR) instruction enables the user to change the values of the BP1, BP0 and SRWD bits:

- The Block Protect (BP1, BP0) bits define the size of the area that is to be treated as read-only, as defined in *Table 2*.
- The SRWD (Status Register Write Disable) bit, in accordance with the signal read on the Write Protect pin ($\overline{W}$), enables the user to set or reset the Write protection mode of the Status Register itself, as defined in *Table 6*. When in Write-protected mode, the Write Status Register (WRSR) instruction is not executed.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W Write cycle.

The Write Status Register (WRSR) instruction has no effect on the b6, b5, b4, b1, b0 bits in the Status Register. Bits b6, b5, b4 are always read as 0.

Table 6. Protection modes

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the Status Register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software-protected (SPM)	Status Register is writable (if the WREN instruction has set the WEL bit). The values in the BP1 and BP0 bits can be changed.	Write-protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware-protected (HPM)	Status Register is Hardware write-protected. The values in the BP1 and BP0 bits cannot be changed.	Write-protected	Ready to accept Write instructions

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register. See *Table 2*.

The protection features of the device are summarized in *Table 6*.

When the Status Register Write Disable (SRWD) bit in the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction), regardless of the logic level applied on the Write Protect ($\overline{W}$) input pin.

When the Status Register Write Disable (SRWD) bit in the Status Register is set to 1, two cases should be considered, depending on the state of the Write Protect ($\overline{W}$) input pin:

- If Write Protect ($\overline{W}$) is driven high, it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction).
- If Write Protect ($\overline{W}$) is driven low, it is not possible to write to the Status Register even if the WEL bit has previously been set by a WREN instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area, which are Software-protected (SPM) by the Block Protect (BP1, BP0) bits in the Status Register, are also hardware-protected against data modification.

Regardless of the order of the two events, the Hardware-protected mode (HPM) can be entered by:

- either setting the SRWD bit after driving the Write Protect ($\overline{W}$) input pin low,
- or driving the Write Protect ($\overline{W}$) input pin low after setting the SRWD bit.

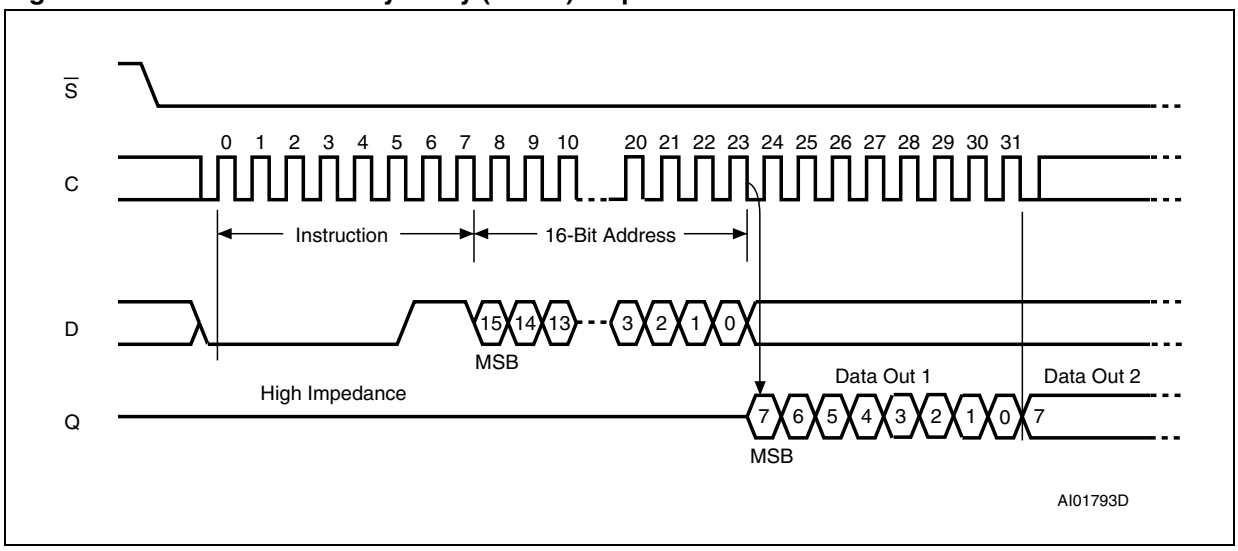
Once the Hardware-protected mode (HPM) has been entered, the only way of exiting it is to pull high the Write Protect ($\overline{W}$) input pin.

If the Write Protect ($\overline{W}$) input pin is permanently tied high, the Hardware-protected mode (HPM) can never be activated, and only the Software-protected mode (SPM), using the Block Protect (BP1, BP0) bits in the Status Register, can be used.

6.5 Read from Memory Array (READ)

As shown in *Figure 12*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

Figure 12. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in *Table 4*, the most significant address bits are Don't Care.

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is incremented automatically, and the byte of data at the new address is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

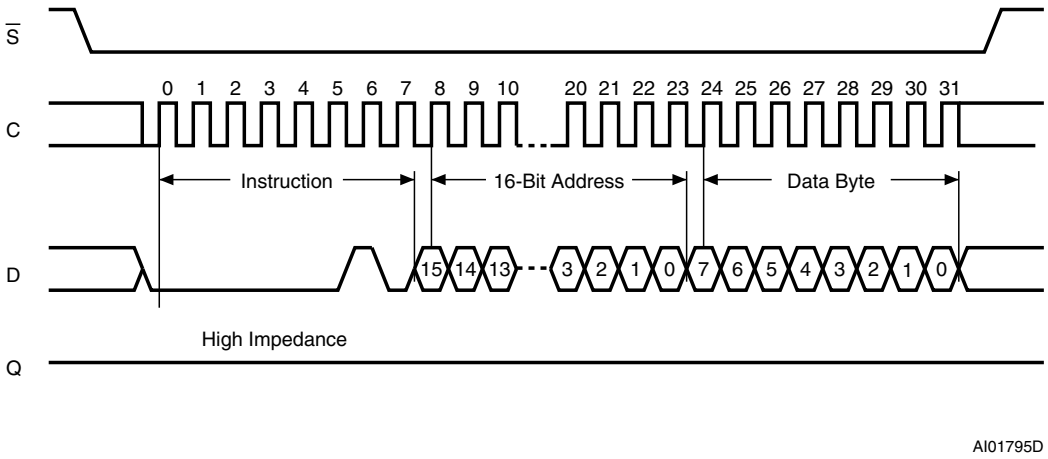
The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

6.6 Write to Memory Array (WRITE)

As shown in *Figure 13*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed Write cycle, triggered by the Chip Select ($\overline{S}$) rising edge, continues for a period t_W (as specified in AC characteristics in *Section 9: DC and AC parameters*), at the end of which the Write in Progress (WIP) bit is reset to 0.

Figure 13. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 4*, the most significant address bits are Don't Care.

In the case of *Figure 13*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. However, if Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 14*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

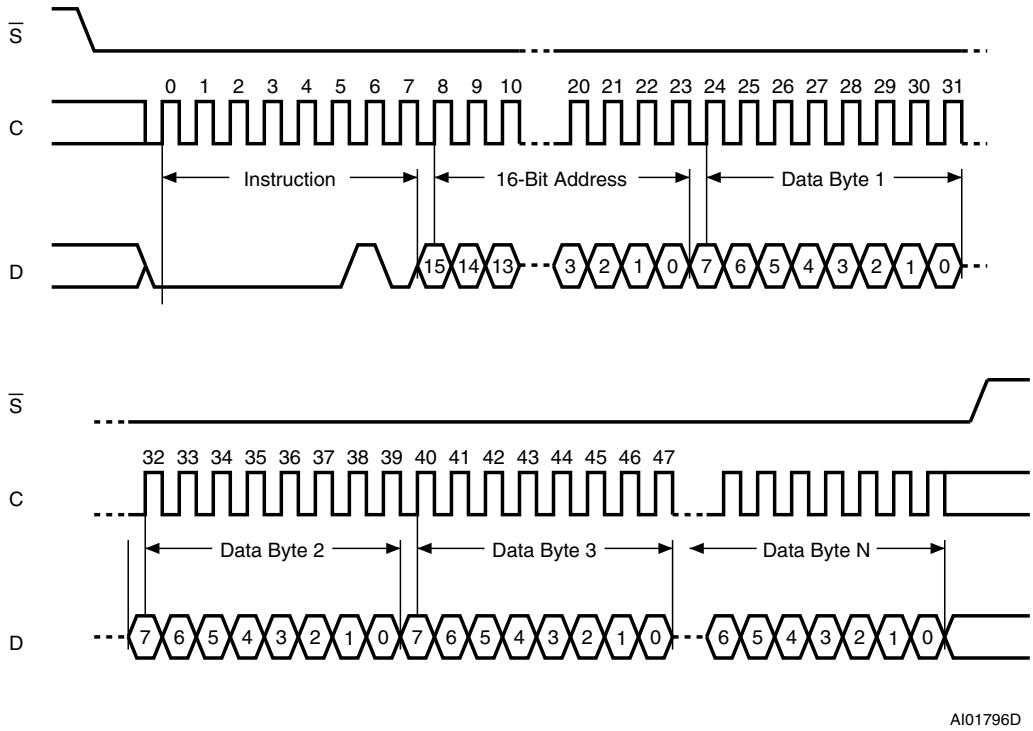
Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If more bytes are sent than will fit up to the end of the page, a condition known as "roll-over" occurs. In case of roll-over, the bytes exceeding the page size are overwritten from location 0 of the same page.

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before),
- if a Write cycle is already in progress,
- if the device has not been deselected, by driving high Chip Select ($\overline{S}$), at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in),
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 14. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 4*, the most significant address bits are Don't Care.

7 Power-up and delivery state

7.1 Power-up state

After power-up, the device is in the following state:

- Standby power mode,
- deselected (after power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started),
- not in the Hold condition,
- the Write Enable Latch (WEL) is reset to 0,
- Write In Progress (WIP) is reset to 0.

The SRWD, BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

7.2 Initial delivery state

The device is delivered with the memory array bits and identification page bits set to all 1s (each byte = FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

8 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_O	Output voltage	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
I_{OL}	DC output current (Q = 0)		5	mA
I_{OH}	DC output current (Q = 1)		5	mA
V_{ESD}	Electrostatic discharge voltage (human body model)(2)		4000	V

1. Compliant with JEDEC Std J-STD-020 (for small body, Sn-Pb or Pb assembly), with the ST ECOPACK® 7191395 specification, and with the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω, R2=500 Ω).

9 DC and AC parameters

This section summarizes the operating conditions and the DC/AC characteristics of the device.

Table 8. Operating conditions (M95160, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	4.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 9. Operating conditions (M95160-W, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 10. Operating conditions (M95160-R, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 11. Operating conditions (M95160-F, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 12. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times		50	ns
	Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}		V
	Input and output timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 15. AC measurement I/O waveform

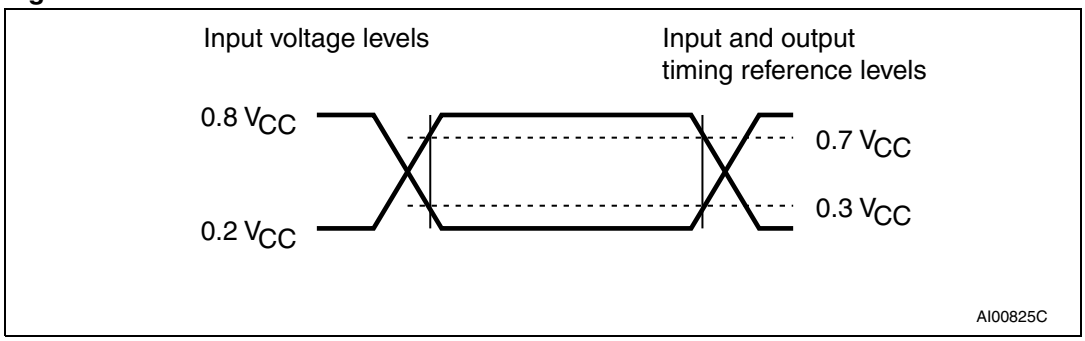


Table 13. Capacitance

Symbol	Parameter	Test conditions(1)	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V		8	pF
	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 5 MHz.

Table 14. Memory cell data retention

Parameter	Test conditions	Min.	Unit
Data retention(1)	TA = 55 °C	40	Year
Cycling	TA = 25 °C	1 million	Cycle

1. The data retention behavior is checked in production. The 40-year limit is defined from characterization and qualification results.

Table 15. DC characteristics (M95160, device grade 6)

Symbol	Parameter	Test conditions in addition to those defined in *Table 8* and *Table 12*	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	C = 0.1 V_{CC}/0.9 V_{CC} at 10 MHz, V_{CC} = 5 V, Q = open		5	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 5 V, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}(1)	Output low voltage	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
V_{OH} (1)	Output high voltage	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V
V_{RES}(2)	Internal reset threshold voltage		2.5	3.5	V

1. For all 5 V range devices, the device meets the output requirements for both TTL and CMOS standards.
2. Characterized only, not tested in production.

Table 16. DC characteristics (M95160-W, device grade 6)

Symbol	Parameter	Test conditions in addition to those defined in *Table 9* and *Table 12*	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	C = 0.1 V_{CC}/0.9 V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open		2	mA
		C = 0.1 V_{CC}/0.9 V_{CC} at 10 MHz, V_{CC} = 2.5 V, Q = open		5	
I_{CC1}	Supply current (Standby Power mode)	$\overline{S} = V_{CC}$, 2.5 V <V_{CC} < 5.5 V $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not tested in production.

Table 17. DC characteristics (M95160-R, device grade 6)

Symbol	Parameter	Test conditions in addition to those defined in *Table 10* and *Table 12*(1)	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, voltage applied on Q = V_{SS} or V_{CC}		± 2	µA
I_{CCR}	Supply current (Read)	V_{CC} = 1.8 V, C = 0.1 V_{CC} or 0.9 V_{CC} f_C = 5 MHz, Q = open		2	mA
		V_{CC} = 2.5 V, C = 0.1 V_{CC} or 0.9 V_{CC}, f_C = 5 MHz, Q = open		3	
I_{CC1}	Supply current (Standby)	V_{CC} = 5.0 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
		V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		1	
		V_{CC} = 1.8 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		1	
V_{IL}	Input low voltage	2.5 V < V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	V
		1.8 V < V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	
V_{IH}	Input high voltage	2.5 V < V_{CC} < 5.5 V	0.7 V_{CC}	V_{CC}+1	V
		1.8 V < V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+1	
V_{OL}	Output low voltage	V_{CC} = 2.5 V, I_{OL} = 1.5 mA, or V_{CC} = 5.5 V, I_{OL} = 2 mA		0.2 V_{CC}	V
		V_{CC} = 1.8 V, I_{OL} = 0.15 mA		0.3	
V_{OH}	Output high voltage	V_{CC} = 2.5 V, I_{OH} = –0.4 mA, or V_{CC} = 5.5 V, I_{OH} = –2 mA, or V_{CC} = 1.8 V, I_{OH} = –0.1 mA	0.8 V_{CC}		V
V_{RES}(2)	Internal reset threshold voltage		1.0	1.65	V

1. If the application uses the M95160-R device with 2.5 V < V_{CC} < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 16: DC characteristics (M95160-W, device grade 6)*, rather than to the above table.
2. Characterized only, not tested in production.

Table 18. DC characteristics (M95160-F, device grade 6)

Symbol	Parameter	Test conditions in addition to those defined in *Table 11* and *Table 12*(1)	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	S = V_{CC}, voltage applied on Q = V_{SS} or V_{CC}		± 2	µA
I_{CCR}	Supply current (Read)	V_{CC} = 2.5 V, C = 0.1 V_{CC} or 0.9 V_{CC}, f_C = 5 MHz, Q = open		3	mA
		V_{CC} = 1.7 V, C = 0.1 V_{CC} or 0.9V_{CC} f_C = 3.5 MHz, Q = open		2	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 5.0 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		2	µA
		V_{CC} = 2.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	µA
		V_{CC} = 1.7 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	µA
V_{IL}	Input low voltage	2.5 V < V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	V
		1.8 < V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		1.7 V < V_{CC} < 1.8 V	–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage	2.5 V < V_{CC} < 5.5 V	0.7 V_{CC}	V_{CC}+1	V
		1.7 V < V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	V_{CC} = 2.5 V, I_{OL} = 1.5 mA, or V_{CC} = 5.5 V, I_{OL} = 2 mA		0.2 V_{CC}	V
		V_{CC} = 1.7 V, I_{OL} = 0.15 mA		0.2	V
V_{OH}	Output high voltage	V_{CC} = 2.5 V, I_{OH} = –0.4 mA, or V_{CC} = 5.5 V, I_{OH} = –2 mA, or V_{CC} = 1.7 V, I_{OH} = –0.1 mA	0.8 V_{CC}		V
V_{RES}(2)	Internal reset threshold voltage		1.0	1.65	V

1. If the application uses the M95160-F device with 2.5 V < V_{CC} < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 16: DC characteristics (M95160-W, device grade 6)*, rather than to the above table.
2. Characterized only, not tested in production.

Table 19. AC characteristics (M95160-W, device grade 6)

Test conditions specified in *Table 9* and *Table 12*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	30		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	30		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	30		ns
t_{CHSL}		$\overline{S}$ not active hold time	30		ns
t_{CH}(1)	t_{CLH}	Clock high time	40		ns
t_{CL}(1)	t_{CLL}	Clock low time	40		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	10		ns
t_{CHDX}	t_{DH}	Data in hold time	10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	30		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	30		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		40	ns
t_{CLQV}	t_V	Clock low to output valid		40	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		40	ns
t_{QHQL}(2)	t_{FO}	Output fall time		40	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		40	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		40	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Characterized only, not tested in production.

Table 20. AC characteristics (M95160-R, device grade 6)

Test conditions specified in *Table 10* and *Table 12*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60		ns
t_{CHSL}		$\overline{S}$ not active hold time	60		ns
t_{CH}(1)	t_{CLH}	Clock high time	80		ns
t_{CL}(1)	t_{CLL}	Clock low time	80		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	20		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	60		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	60		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		80	ns
t_{CLQV}	t_V	Clock low to output valid		80	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		80	ns
t_{QHQL}(2)	t_{FO}	Output fall time		80	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		80	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		80	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Characterized only, not tested in production.

Table 21. AC characteristics (M95160-F, device grade 6)

Test conditions specified in *Table 11* and *Table 12*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	3.5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	85		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	85		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	120		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	85		ns
t_{CHSL}		$\overline{S}$ not active hold time	85		ns
t_{CH}(1)	t_{CLH}	Clock high time	110		ns
t_{CL}(1)	t_{CLL}	Clock low time	110		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	30		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	85		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	85		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		0
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		0
t_{SHQZ}(2)	t_{DIS}	Output disable time		120	ns
t_{CLQV}	t_V	Clock low to output valid		120	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		100	ns
t_{QHQL}(2)	t_{FO}	Output fall time		100	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		110	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		110	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Characterized only, not tested in production.

The values in the following table must not be considered for any new design.

Table 22. AC characteristics (M95160, device grade 6)
End of life products: these values apply only to M95160-MN6TP/S devices

Test conditions specified in *Table 8* and *Table 12*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	25		ns
t_{CHSL}		$\overline{S}$ not active hold time	15		ns
t_{CH}(1)	t_{CLH}	Clock high time	40		ns
t_{CL} (1)	t_{CLL}	Clock low time	40		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		1	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	15		ns
t_{CHDX}	t_{DH}	Data in hold time	15		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	15		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	20		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		25	ns
t_{CLQV}	t_V	Clock low to output valid		35	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		20	ns
t_{QHQL}(2)	t_{FO}	Output fall time		20	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		25	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		35	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Characterized only, not tested in production.

The values in the following table must not be considered for any new design.

Table 23. AC characteristics (M95160-W, device grade 6) End of life products: these values apply only to M95160-WMN6TP/S and M95160-WDW6TP/S devices)

Test conditions specified in *Table 9* and *Table 12*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
t_{CH}(1)	t_{CLH}	Clock high time	90		ns
t_{CL}(1)	t_{CLL}	Clock low time	90		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		1	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		50	ns
t_{QHQL}(2)	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Characterized only, not tested in production.

Figure 16. Serial input timing

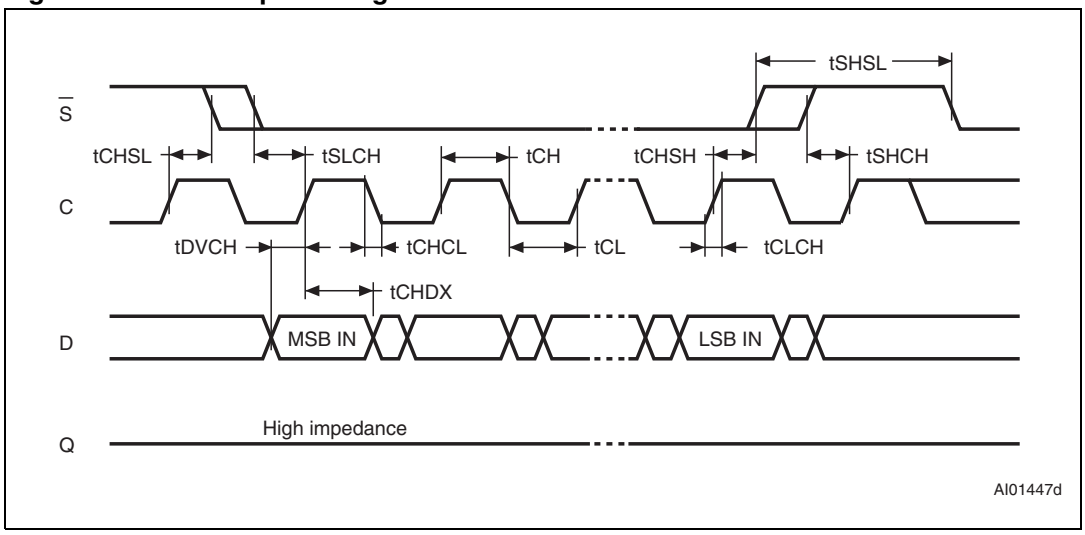


Figure 17. Hold timing

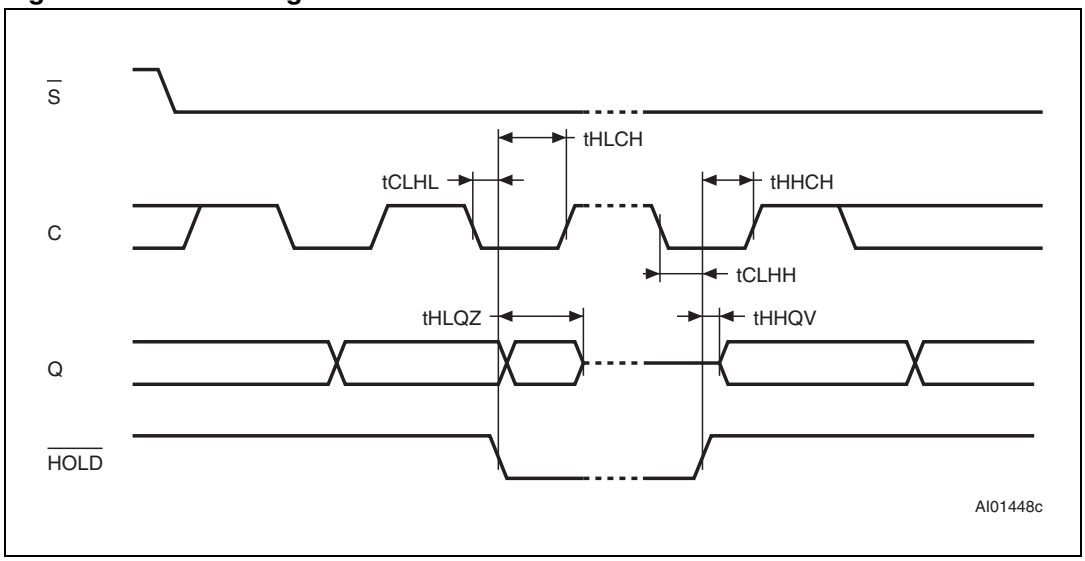
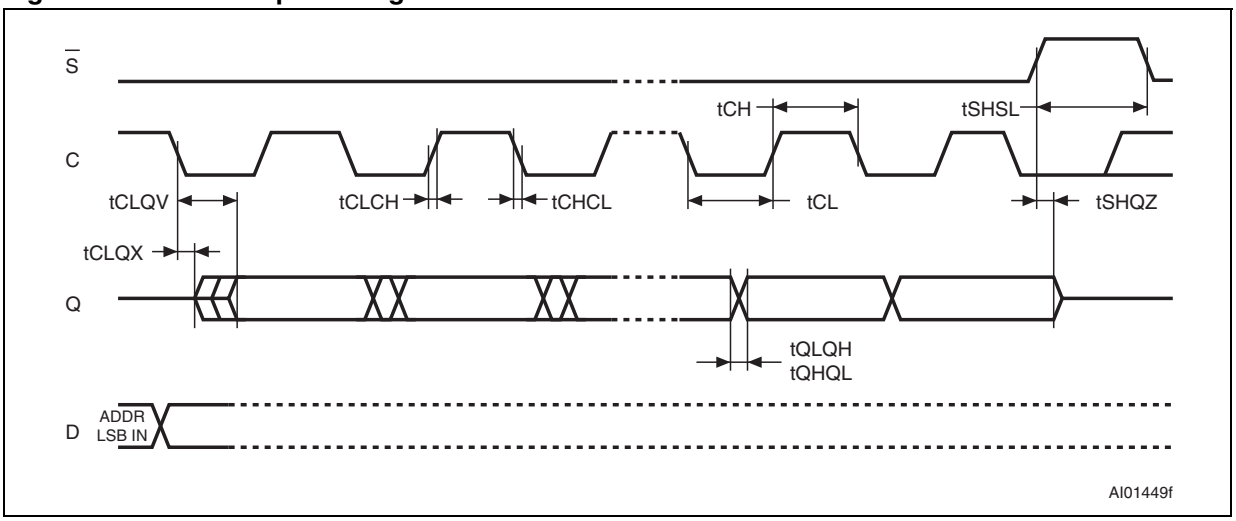


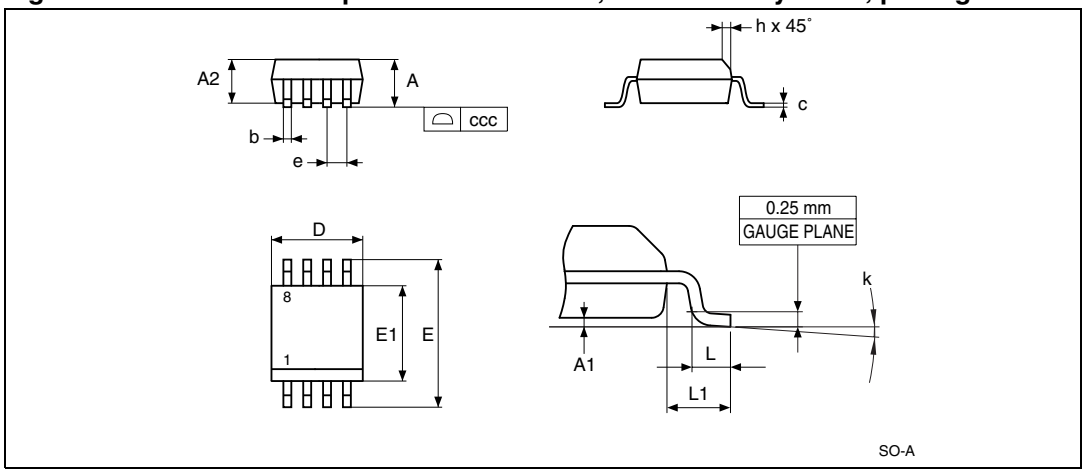
Figure 18. Serial output timing



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 19. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



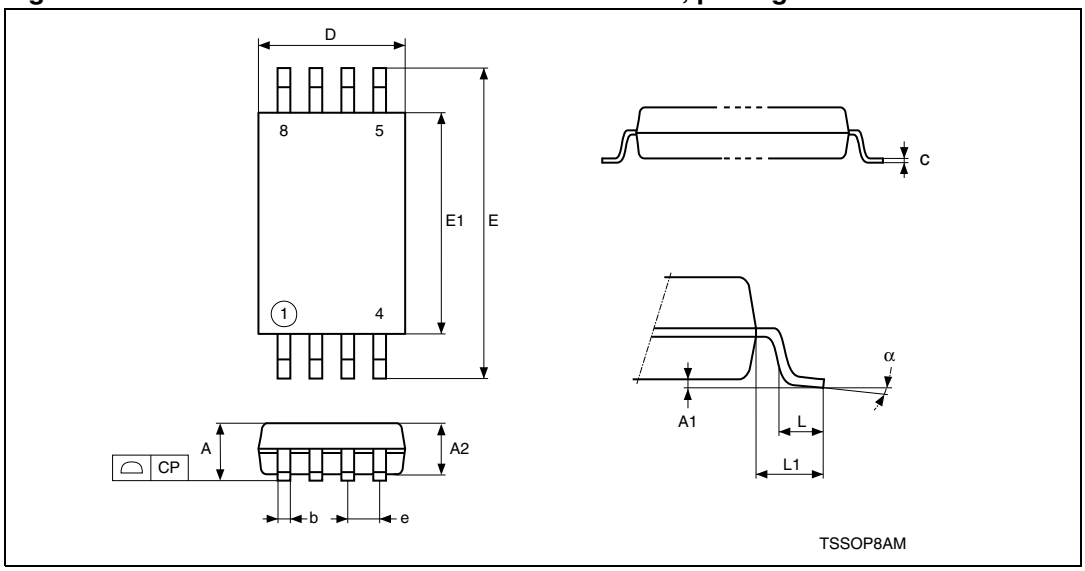
1. Drawing is not to scale.

Table 24. SO8N – 8-lead plastic small outline, 150 mils body width, mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.750			0.0689
A1		0.100	0.250		0.0039	0.0098
A2		1.250			0.0492	
b		0.280	0.480		0.0110	0.0189
c		0.170	0.230		0.0067	0.0091
ccc			0.100			0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270	-	-	0.0500	-	-
h		0.250	0.500		0.0098	0.0197
k		0°	8°		0°	8°
L		0.400	1.270		0.0157	0.0500
L1	1.040			0.0409		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 20. TSSOP8 – 8-lead thin shrink small outline, package outline



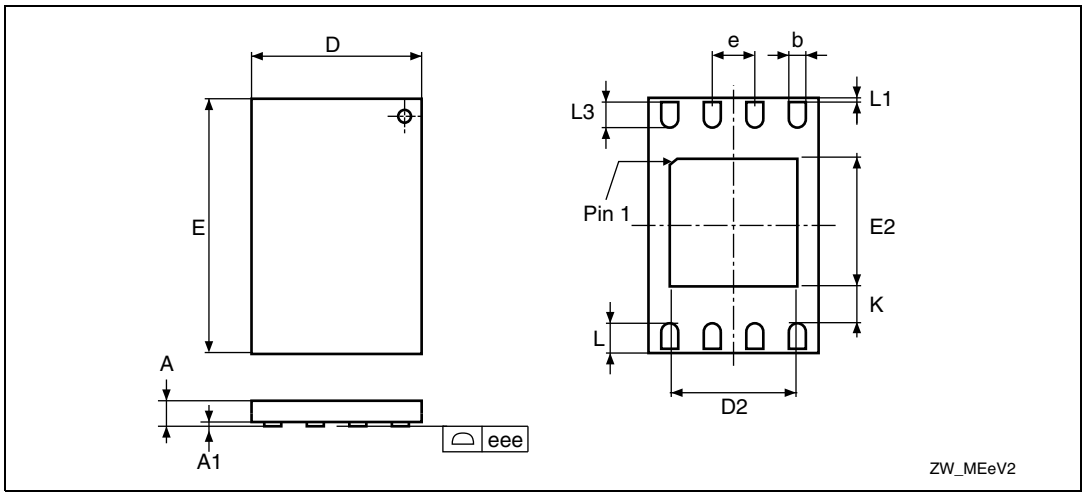
1. Drawing is not to scale.

Table 25. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°
N	8			8		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 21. UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat no lead, package outline



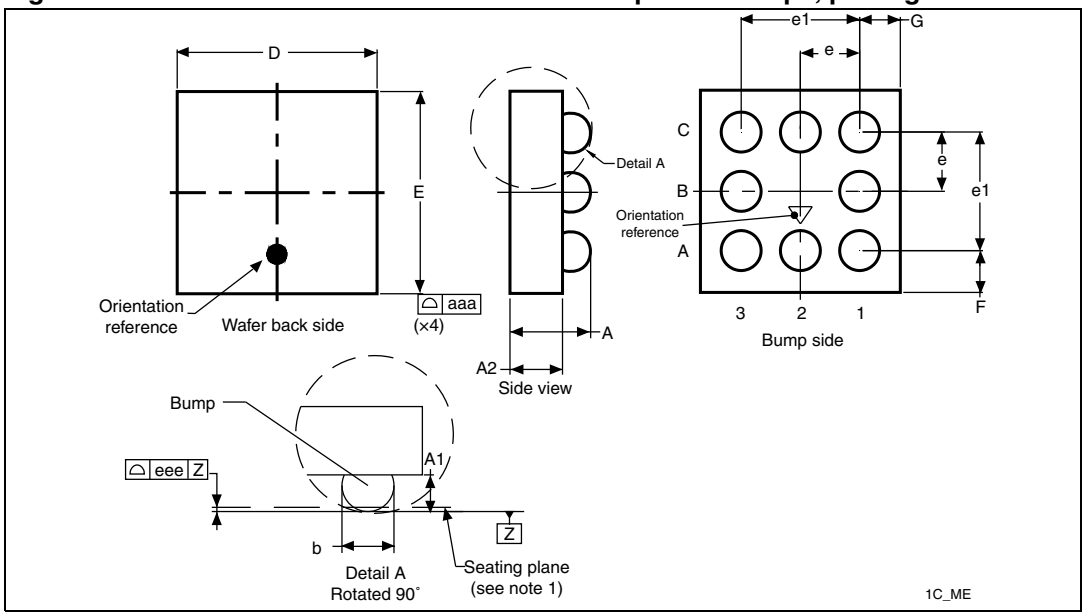
1. Drawing is not to scale.
2. The central pad (area E2 by D2 in the above illustration) is internally pulled to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 26. UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MC)		1.200	1.600		0.0472	0.0630
e	0.500			0.0197		
K (rev MC)		0.300			0.0118	
L		0.300	0.500		0.0118	0.0197
L1			0.150			0.0059
L3		0.300			0.0118	
eee[2]		0.080			0.0031	

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

Figure 22. WLCSP-R – 1.350 x 1.365 mm 0.4 mm pitch 8 bumps, package outline



1. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
2. Drawing is not to scale.
3. Preliminary data.

Table 27. WLCSP-R – 1.350 x 1.365 mm 0.4 mm pitch 8 bumps, package mechanical data (preliminary data)

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.545	0.490	0.600	0.0193	0.0215	0.0236
A1	0.190			0.0075		
A2	0.355			0.014		
b[2]	0.270	0.240	0.300	0.0106	0.0094	0.0118
D	1.350		1.475	0.0531		0.0581
E	1.365		1.490	0.0537		0.0587
e	0.400			0.0157		
e1	0.800			0.0315		
F	0.282			0.0111		
G	0.275			0.0108		
N (total number of terminals)	8			8		
aaa	0.110			0.0043		
eee	0.060			0.0024		

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

11 Part numbering

Table 28. Ordering information scheme

Example: M95160 W MN 6 T P /S

Device type

M95 = SPI serial access EEPROM

Device function

160 = 16 Kbit (2048 x 8)

Operating voltage

blank = V_{CC} = 4.5 to 5.5 V
W = V_{CC} = 2.5 to 5.5 V
R = V_{CC} = 1.8 to 5.5 V
F = V_{CC} = 1.7 to 5.5 V

Package(1)

MN = SO8 (150 mil width)
DW = TSSOP8 (169 mil width)
MC = UFDFPN8 (MLP8)
CS = WLCSP

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

Option

blank = Standard packing
T = Tape and reel packing

Plating technology

G or P = RoHS compliant and halogen-free
(ECOPACK®)

Process(2)

/G or /S= Manufacturing technology code

1. All packages are ECOPACK2® (RoHS compliant and halogen-free).
2. The process letters apply to WLCSP devices only. The process letters appear on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office for further information.

12 Revision history

Table 29. Document revision history

Date	Revision	Changes
22-Mar-2012	1	Initial release.
17-Dec-2012	2	Updated: – All information about package UFDFPN8 – Introduction of *Description* – *Section 7.2: Initial delivery state*
08-Jan-2013	3	Updated plating technology in *Section 11: Part numbering*.

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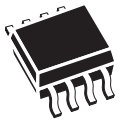
M95080 M95080-W M95080-R

8-Kbit serial SPI bus EEPROM with high-speed clock

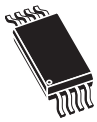
Datasheet – production data

Features

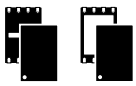
- Compatible with the Serial Peripheral Interface (SPI) bus
- Memory array
  - 8 Kb (1 Kbyte) of EEPROM
  - Page size: 32 bytes
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Write Protect: quarter, half or whole memory array
- High-speed clock: 10 MHz
- Single supply voltage:
  - 4.5 V to 5.5 V for M95080
  - 2.5 V to 5.5 V for M95080-W
  - 1.8 V to 5.5 V for M95080-R
- Operating temperature range: from -40°C up to +85°C
- Enhanced ESD protection
- More than 1 million Write cycles
- More than 40-year data retention
- Packages
  - RoHS compliant and halogen-free (ECOPACK®)



SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width



UFDFPN8 (MB, MC)
2 × 3 mm (MLP)

Contents

List of tables

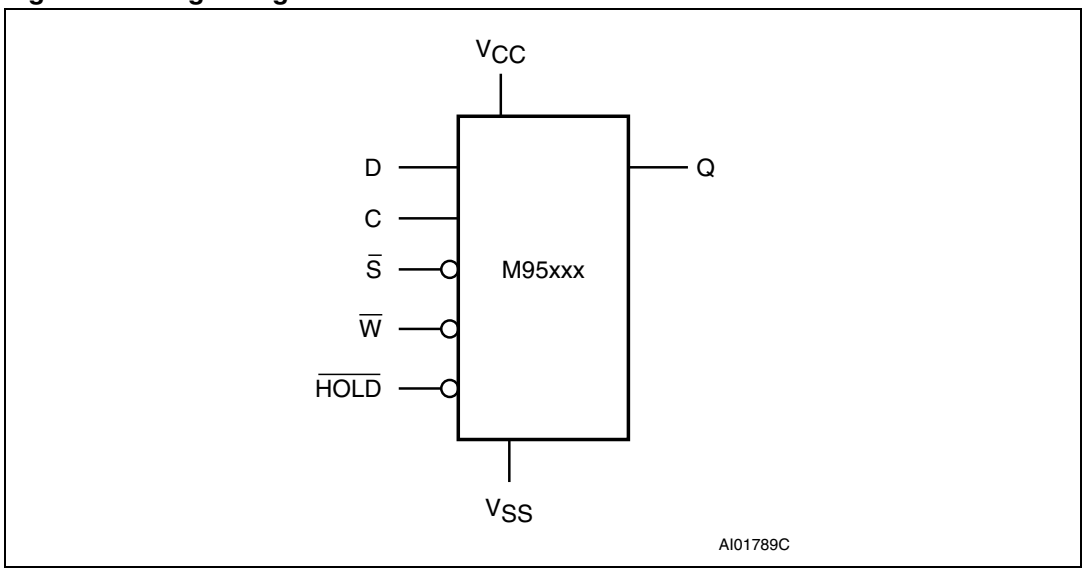
List of figures

1 Description

The M95080 devices are Electrically Erasable PROgrammable Memories (EEPROMs) organized as 1024 x 8 bits, accessed through the SPI bus.

The M95080 devices can operate with a supply range from 1.8 V up to 5.5 V, and are guaranteed over the -40 °C/+85 °C temperature range.

Figure 1. Logic diagram

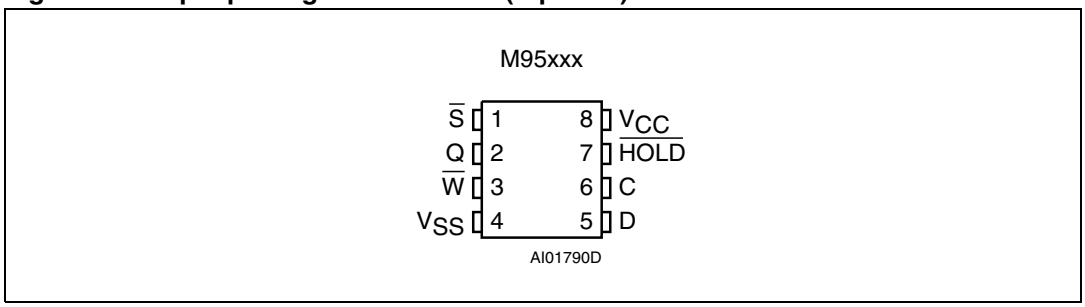


The SPI bus signals are C, D and Q, as shown in *Figure 1* and *Table 1*. The device is selected when Chip Select ($\overline{S}$) is driven low. Communications with the device can be interrupted when the $\overline{HOLD}$ is driven low.

Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data Input	Input
Q	Serial Data Output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. 8-pin package connections (top view)

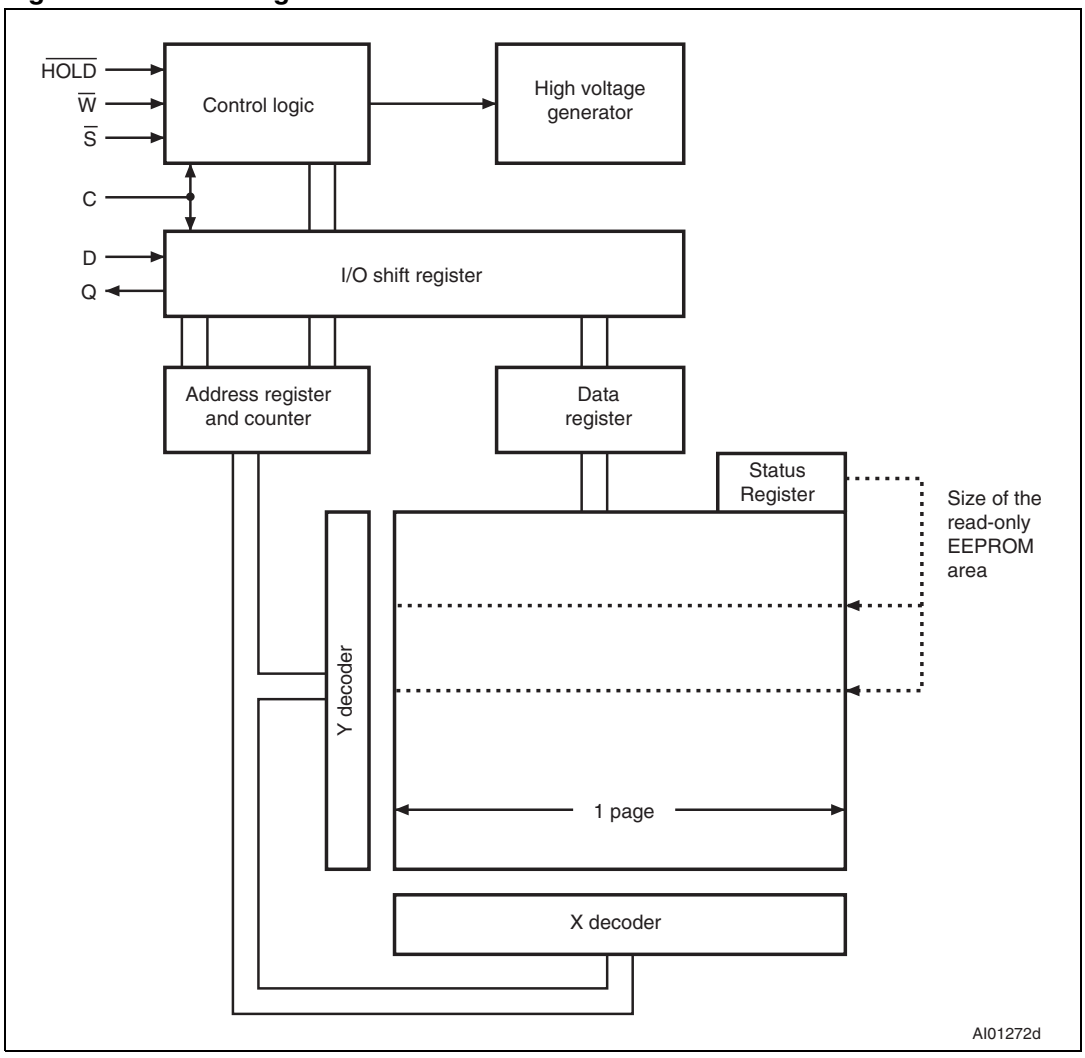


1. See *Section 10: Package mechanical data* section for package dimensions, and how to identify pin 1.

2 Memory organization

The memory is organized as shown in the following figure.

Figure 3. Block diagram



3 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Section 9: DC and AC parameters*). These signals are described next.

3.1 Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

3.2 Serial Data Input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

3.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) change from the falling edge of Serial Clock (C).

3.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. The device is in the Standby Power mode, unless an internal Write cycle is in progress. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

3.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

3.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all Write instructions.

3.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

3.8 V_{SS} ground

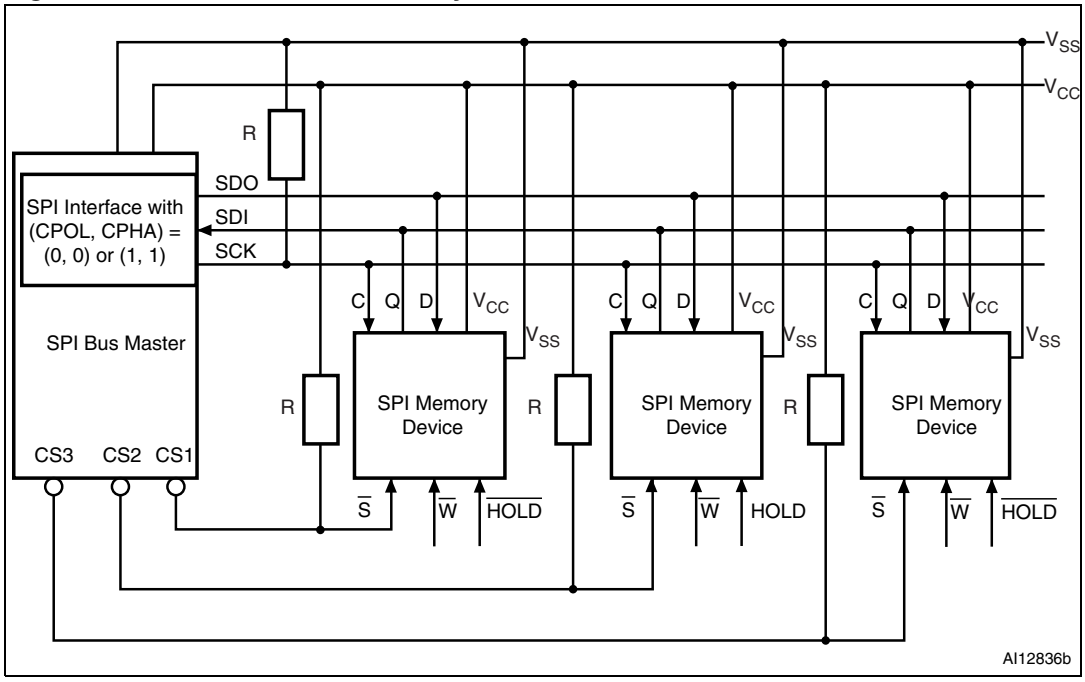
V_{SS} is the reference for all signals, including the V_{CC} supply voltage.

4 Connecting to the SPI bus

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 4. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

Figure 4 shows an example of three memory devices connected to an SPI bus master. Only one memory device is selected at a time, so only one memory device drives the Serial Data Output (Q) line at a time. The other memory devices are high impedance.

The pull-up resistor R (represented in *Figure 4*) ensures that a device is not selected if the Bus Master leaves the $\overline{S}$ line in the high impedance state.

In applications where the Bus Master may leave all SPI bus lines in high impedance at the same time (for example, if the Bus Master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high): this ensures that $\overline{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met. The typical value of R is 100 kΩ.

4.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

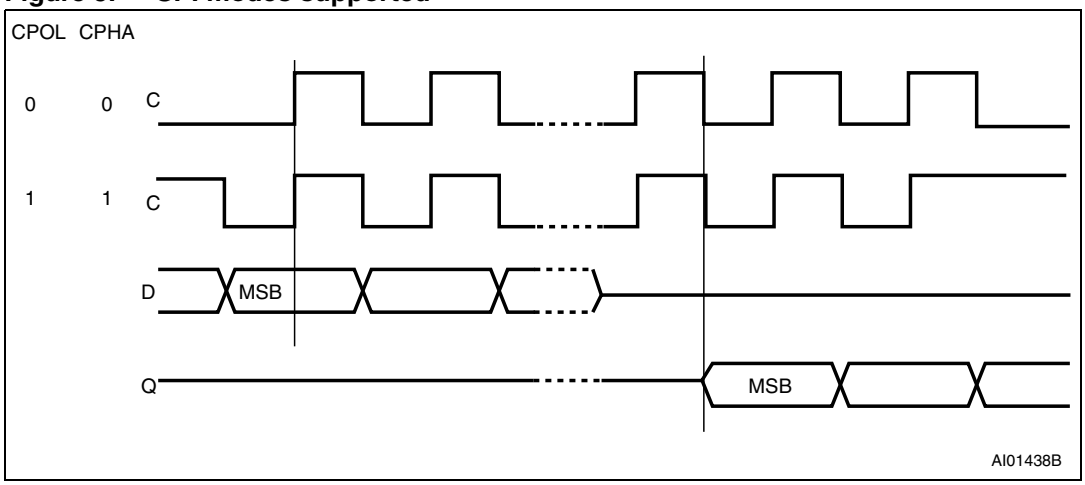
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 5*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 5. SPI modes supported



5 Operating features

5.1 Supply voltage (V_{CC})

5.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 9: DC and AC parameters*). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} device pins.

5.1.2 Device reset

In order to prevent erroneous instruction decoding and inadvertent Write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until VCC reaches the POR threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 9: DC and AC parameters*).

At power-up, when V_{CC} passes over the POR threshold, the device is reset and is in the following state:

- in Standby Power mode,
- deselected,
- Status Register values:
  - The Write Enable Latch (WEL) bit is reset to 0.
  - The Write In Progress (WIP) bit is reset to 0.
  - The SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).

It is important to note that the device must not be accessed until V_{CC} reaches a valid and stable level within the specified [V_{CC}(min), V_{CC}(max)] range, as defined under Operating conditions in *Section 9: DC and AC parameters*.

5.1.3 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 4*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined under Operating conditions in *Section 9: DC and AC parameters*, and the rise time must not vary faster than 1 V/µs.

5.1.4 Power-down

During power-down (continuous decrease of the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined under Operating conditions in *Section 9: DC and AC parameters*), the device must be:

- deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC}),
- in Standby Power mode (there should not be any internal write cycle in progress).

5.2 Active Power and Standby Power modes

When Chip Select ($\overline{S}$) is low, the device is selected, and in the Active Power mode. The device consumes I_{CC}.

When Chip Select ($\overline{S}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes into the Standby Power mode, and the device consumption drops to I_{CC1}, as specified in DC characteristics (see *Section 9: DC and AC parameters*).

5.3 Hold condition

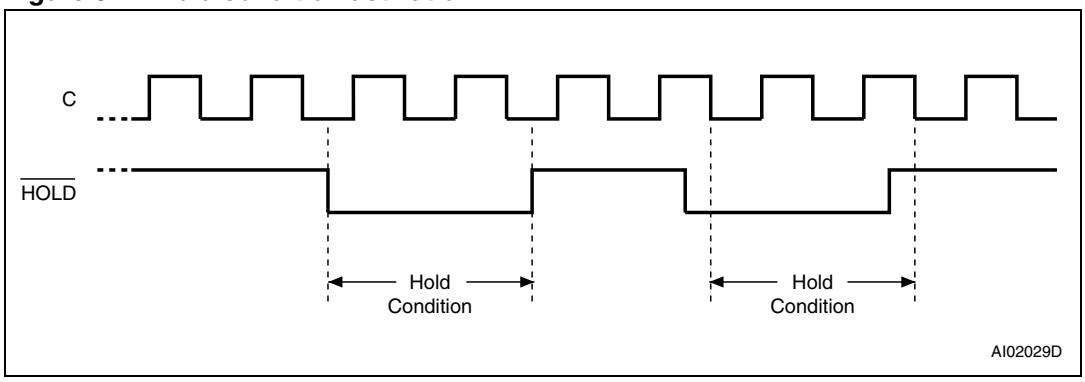
The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) low.

During the Hold condition, the Serial Data Output (Q) is high impedance, and the Serial Data Input (D) and the Serial Clock (C) are Don't Care.

Normally, the device is kept selected for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition has the effect of resetting the state of the device, and this mechanism can be used if required to reset any processes that had been in progress.[(a)(b)]

Figure 6. Hold condition activation



The Hold condition starts when the Hold (HOLD) signal is driven low when Serial Clock (C) is already low (as shown in *Figure 6*).

a. This resets the internal logic, except the WEL and WIP bits of the Status Register.

b. In the specific case where the device has shifted in a Write command (Inst + Address + data bytes, each data byte being exactly 8 bits), deselecting the device also triggers the Write cycle of this decoded command.

The Hold condition ends when the Hold (HOLD) signal is driven high when Serial Clock (C) is already low.

Figure 6 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

5.4 Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.3: Read Status Register (RDSR)* for a detailed description of the Status Register bits.

5.5 Data protection and protocol control

The device features the following data protection mechanisms:

- Before accepting the execution of the Write and Write Status Register instructions, the device checks whether the number of clock pulses comprised in the instructions is a multiple of eight.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit.
- The Block Protect (BP1, BP0) bits in the Status Register are used to configure part of the memory as read-only.
- The Write Protect ($\overline{W}$) signal is used to protect the Block Protect (BP1, BP0) bits in the Status Register.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points should be noted in the previous sentence:

- The “last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The “next rising edge of Serial Clock (C)” might (or might not) be the next bus transaction for some other device on the SPI bus.

Table 2. Write-protected block size

Status Register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	none	none
0	1	Upper quarter	0300h - 03FFh
1	0	Upper half	0200h - 03FFh
1	1	Whole memory	0000h - 03FFh

6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 3*.

If an invalid instruction is sent (one not contained in *Table 3*), the device automatically deselects itself.

Table 3. Instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

Table 4. Address range bits

Address significant bits	A9-A0(1)

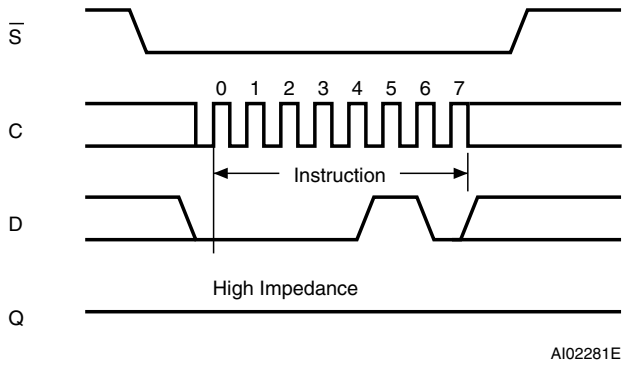
1. Upper MSBs are Don't Care.

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 7*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 7. Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

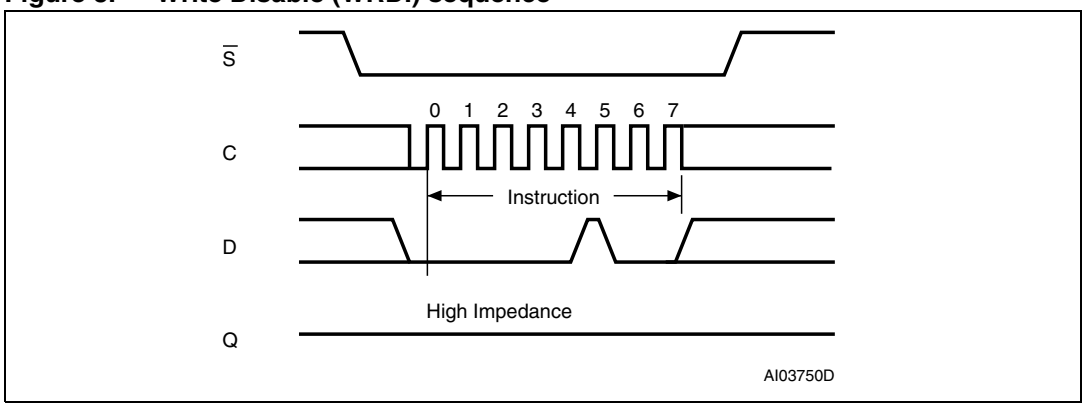
As shown in *Figure 8*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

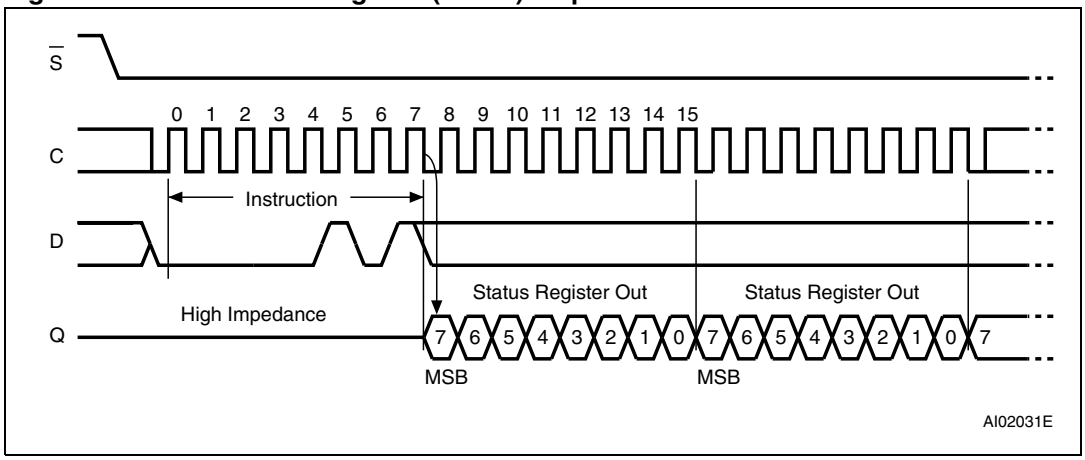
Figure 8. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction is used to read the Status Register. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 9*.

Figure 9. Read Status Register (RDSR) sequence



The status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0, no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set. When set to 0, the internal Write Enable Latch is reset, and no Write or Write Status Register instruction is accepted.

The WEL bit is returned to its reset state by the following events:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Write (WRITE) instruction completion

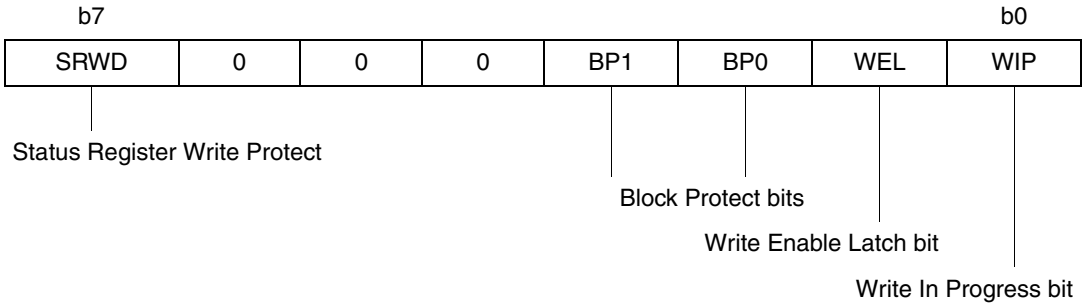
6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non volatile. They define the size of the area to be software-protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 2*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal enable the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 5. Status Register format



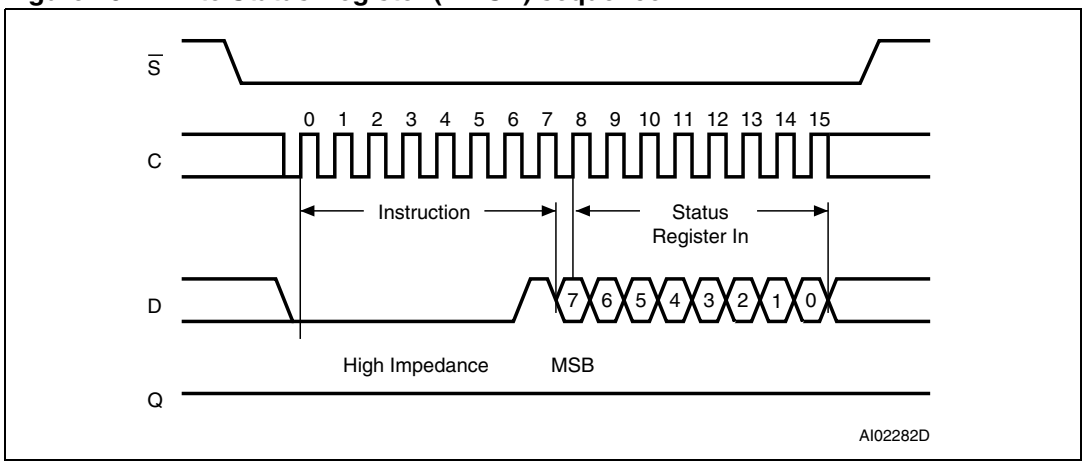
6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction is used to write new values to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must have been previously executed.

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) low, followed by the instruction code, the data byte on Serial Data input (D) and Chip Select ($\overline{S}$) driven high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed.

The instruction sequence is shown in *Figure 10*.

Figure 10. Write Status Register (WRSR) sequence



Driving the Chip Select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed Write cycle that takes t_W to complete (as specified in AC tables under *Section 9: DC and AC parameters*).

While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in progress (WIP) bit: the WIP bit is 1 during the self-timed Write cycle t_W, and 0 when the Write cycle is complete. The WEL bit (Write Enable Latch) is also reset at the end of the Write cycle t_W.

The Write Status Register (WRSR) instruction enables the user to change the values of the BP1, BP0 and SRWD bits:

- The Block Protect (BP1, BP0) bits define the size of the area that is to be treated as read-only, as defined in *Table 2*.
- The SRWD (Status Register Write Disable) bit, in accordance with the signal read on the Write Protect pin ($\overline{W}$), enables the user to set or reset the Write protection mode of the Status Register itself, as defined in *Table 6*. When in Write-protected mode, the Write Status Register (WRSR) instruction is not executed.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W Write cycle.

The Write Status Register (WRSR) instruction has no effect on the b6, b5, b4, b1, b0 bits in the Status Register. Bits b6, b5, b4 are always read as 0.

Table 6. Protection modes

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the Status Register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software-protected (SPM)	Status Register is writable (if the WREN instruction has set the WEL bit). The values in the BP1 and BP0 bits can be changed.	Write-protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware-protected (HPM)	Status Register is Hardware write-protected. The values in the BP1 and BP0 bits cannot be changed.	Write-protected	Ready to accept Write instructions

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register. See *Table 2*.

The protection features of the device are summarized in *Table 6*.

When the Status Register Write Disable (SRWD) bit in the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction), regardless of the logic level applied on the Write Protect ($\overline{W}$) input pin.

When the Status Register Write Disable (SRWD) bit in the Status Register is set to 1, two cases should be considered, depending on the state of the Write Protect ($\overline{W}$) input pin:

- If Write Protect ($\overline{W}$) is driven high, it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction).
- If Write Protect ($\overline{W}$) is driven low, it is not possible to write to the Status Register even if the WEL bit has previously been set by a WREN instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area, which are Software-protected (SPM) by the Block Protect (BP1, BP0) bits in the Status Register, are also hardware-protected against data modification.

Regardless of the order of the two events, the Hardware-protected mode (HPM) can be entered by:

- either setting the SRWD bit after driving the Write Protect ($\overline{W}$) input pin low,
- or driving the Write Protect ($\overline{W}$) input pin low after setting the SRWD bit.

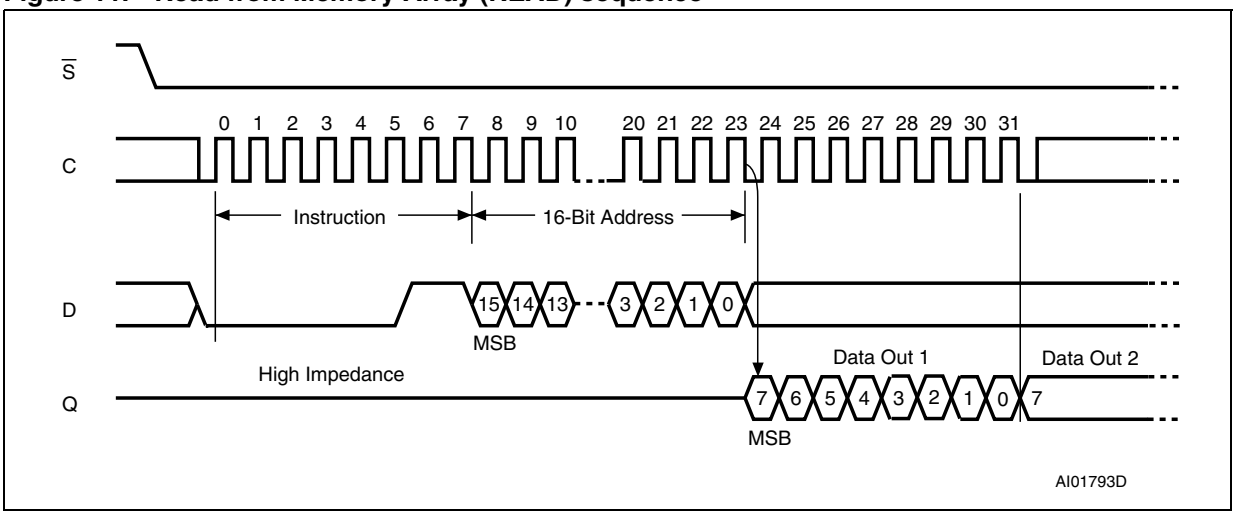
Once the Hardware-protected mode (HPM) has been entered, the only way of exiting it is to pull high the Write Protect ($\overline{W}$) input pin.

If the Write Protect ($\overline{W}$) input pin is permanently tied high, the Hardware-protected mode (HPM) can never be activated, and only the Software-protected mode (SPM), using the Block Protect (BP1, BP0) bits in the Status Register, can be used.

6.5 Read from Memory Array (READ)

As shown in *Figure 11*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

Figure 11. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in *Table 4*, the most significant address bits are Don't Care.

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is incremented automatically, and the byte of data at the new address is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

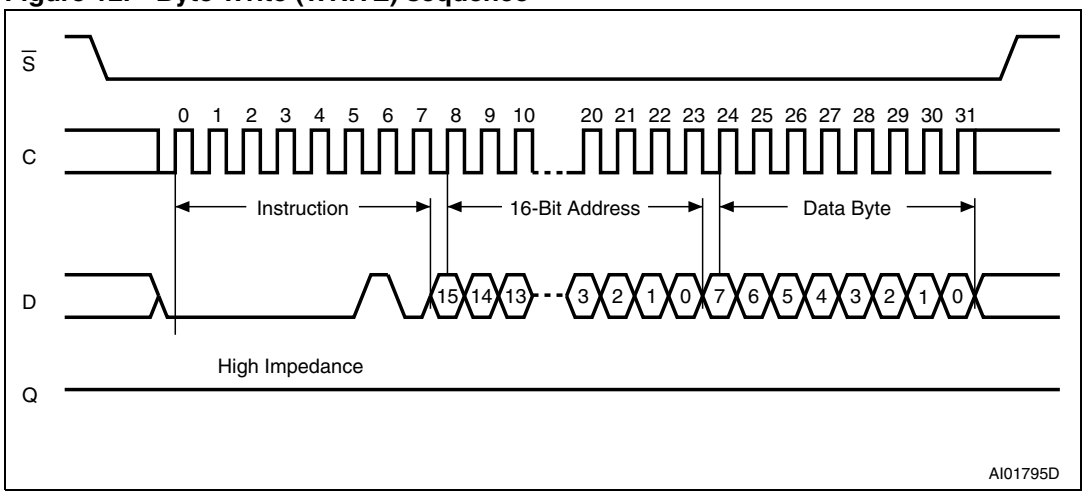
The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

6.6 Write to Memory Array (WRITE)

As shown in *Figure 12*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed Write cycle, triggered by the Chip Select ($\overline{S}$) rising edge, continues for a period t_W (as specified in AC characteristics in *Section 9: DC and AC parameters*), at the end of which the Write in Progress (WIP) bit is reset to 0.

Figure 12. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 4*, the most significant address bits are Don't Care.

In the case of *Figure 12*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. However, if Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 13*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

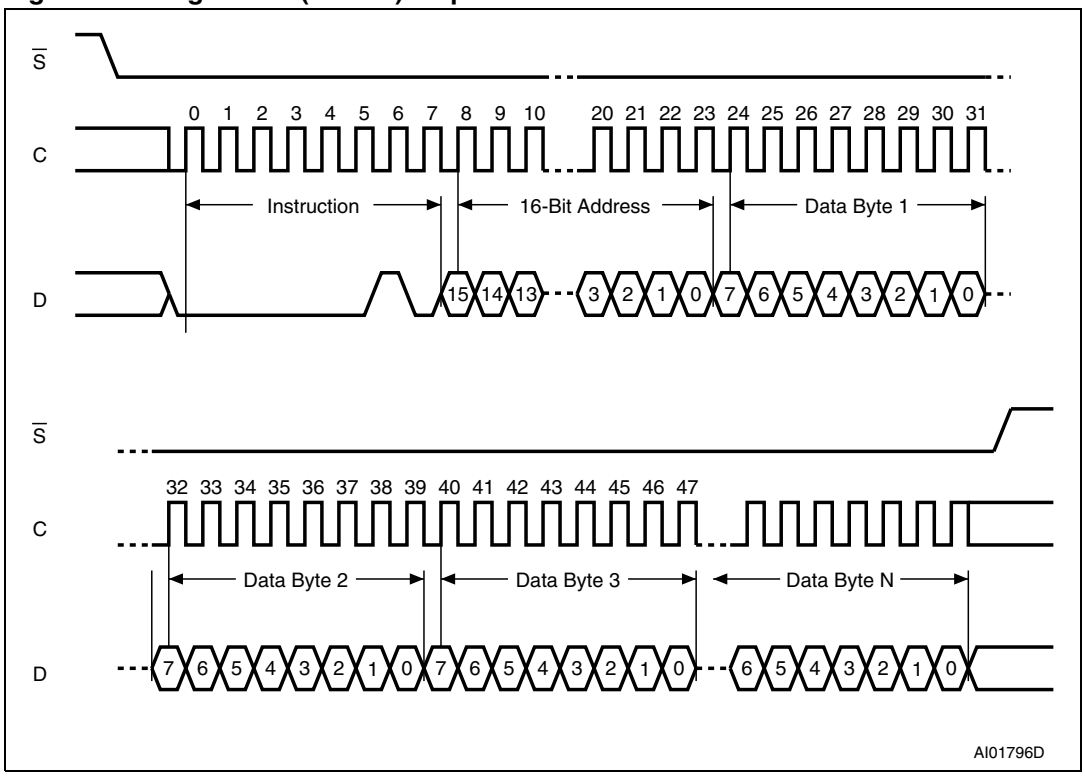
Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 32 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before),
- if a Write cycle is already in progress,
- if the device has not been deselected, by driving high Chip Select ($\overline{S}$), at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in),
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 13. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 4*, the most significant address bits are Don't Care.

7 Power-up and delivery state

7.1 Power-up state

After power-up, the device is in the following state:

- Standby power mode,
- deselected (after power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started),
- not in the Hold condition,
- the Write Enable Latch (WEL) is reset to 0,
- Write In Progress (WIP) is reset to 0.

The SRWD, BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

7.2 Initial delivery state

The device is delivered with the memory array set to all 1s (each byte = FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

8 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_O	Output voltage	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
I_{OL}	DC output current (Q = 0)		5	mA
I_{OH}	DC output current (Q = 1)		5	mA
V_{ESD}	Electrostatic discharge voltage (human body model)(2)		4000	V

1. Compliant with JEDEC Std J-STD-020 (for small body, Sn-Pb or Pb assembly), with the ST ECOPACK® 7191395 specification, and with the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. Positive and negative pulses applied on pin pairs, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω, R2=500 Ω).

9 DC and AC parameters

This section summarizes the operating conditions and the DC/AC characteristics of the device.

Table 8. Operating conditions (M95080, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	4.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 9. Operating conditions (M95080-W, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 10. Operating conditions (M95080-R, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 11. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times		50	ns
	Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}		V
	Input and output timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 14. AC measurement I/O waveform

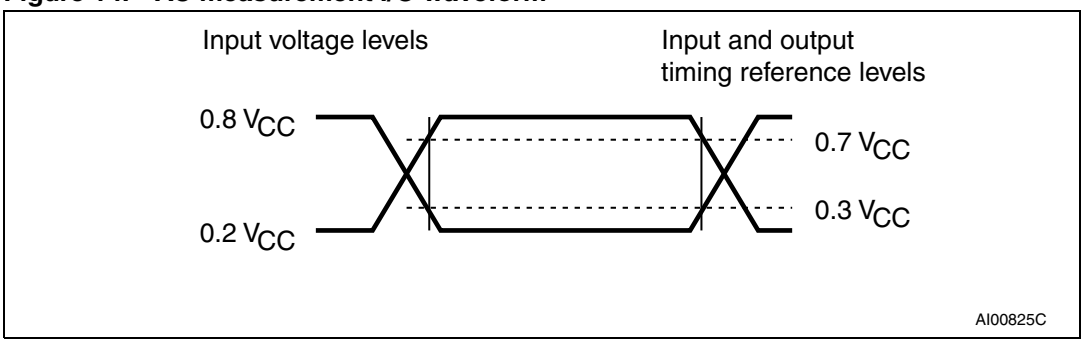


Table 12. Capacitance

Symbol	Parameter	Test conditions(1)	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V		8	pF
	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 5 MHz.

Table 13. DC characteristics (M95080, device grade 6)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	C = 0.1 V_{CC}/0.9 V_{CC} at 10 MHz, V_{CC} = 5 V, Q = open		5	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 5 V, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}(1)	Output low voltage	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
V_{OH} (1)	Output high voltage	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V
V_{RES}(2)	Internal reset threshold voltage		2.5	3.5	V

1. For all 5 V range devices, the device meets the output requirements for both TTL and CMOS standards.
2. Characterized only, not tested in production.

Table 14. DC characteristics (M95080-W, device grade 6)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	C = 0.1 V_{CC}/0.9 V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open		2	mA
		C = 0.1 V_{CC}/0.9 V_{CC} at 10 MHz, V_{CC} = 2.5 V, Q = open		5	
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, 2.5 V <V_{CC} < 5.5 V $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not tested in production.

Table 15. DC characteristics (M95080-R, device grade 6)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, voltage applied on Q = V_{SS} or V_{CC}		± 2	µA
I_{CCR}	Supply current (Read)	V_{CC} = 1.8 V, C = 0.1 V_{CC} or 0.9 V_{CC} f_C = 5 MHz, Q = open		2	mA
		V_{CC} = 2.5 V, C = 0.1 V_{CC} or 0.9 V_{CC}, f_C = 5 MHz, Q = open		3	
		$V_{CC} \geq$ 2.5 V, C = 0.1 V_{CC} or 0.9 V_{CC}, f_C = 10 MHz, Q = open		5	
I_{CC1}	Supply current (Standby)	V_{CC} = 5.0 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
		V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		1	
		V_{CC} = 1.8 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		1	
V_{IL}	Input low voltage	2.5 V < V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	V
		1.8 V < V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	
V_{IH}	Input high voltage	2.5 V < V_{CC} < 5.5 V	0.7 V_{CC}	V_{CC}+1	V
		1.8 V < V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+1	
V_{OL}	Output low voltage	V_{CC} = 2.5 V, I_{OL} = 1.5 mA, or V_{CC} = 5.5 V, I_{OL} = 2 mA		0.2 V_{CC}	V
		V_{CC} = 1.8 V, I_{OL} = 0.15 mA		0.3	
V_{OH}	Output high voltage	V_{CC} = 2.5 V, I_{OH} = –0.4 mA, or V_{CC} = 5.5 V, I_{OH} = –2 mA, or V_{CC} = 1.8 V, I_{OH} = –0.1 mA	0.8 V_{CC}		V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not tested in production.

Table 16. AC characteristics (M95080-W, device grade 6)

Test conditions specified in *Table 9* and *Table 11*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	30		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	30		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	30		ns
t_{CHSL}		$\overline{S}$ not active hold time	30		ns
t_{CH}(1)	t_{CLH}	Clock high time	40		ns
t_{CL}(1)	t_{CLL}	Clock low time	40		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	10		ns
t_{CHDX}	t_{DH}	Data in hold time	10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	30		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	30		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		40	ns
t_{CLQV}	t_V	Clock low to output valid		40	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		40	ns
t_{QHQL}(2)	t_{FO}	Output fall time		40	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		40	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		40	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Characterized only, not tested in production.

Table 17. AC characteristics (M95080-R, device grade 6)

Test conditions specified in *Table 10* and *Table 11*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60		ns
t_{CHSL}		$\overline{S}$ not active hold time	60		ns
t_{CH}(1)	t_{CLH}	Clock high time	80		ns
t_{CL}(1)	t_{CLL}	Clock low time	80		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	20		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	60		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	60		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		80	ns
t_{CLQV}	t_V	Clock low to output valid		80	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		80	ns
t_{QHQL}(2)	t_{FO}	Output fall time		80	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		80	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		80	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Characterized only, not tested in production.

The values in the following table must not be considered for any new design.

Table 18. AC characteristics (M95080, device grade 6)
End of life products: these values apply only to M95080-MN6TP/S devices

Test conditions specified in *Table 8* and *Table 11*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	25		ns
t_{CHSL}		$\overline{S}$ not active hold time	15		ns
t_{CH}(1)	t_{CLH}	Clock high time	40		ns
t_{CL} (1)	t_{CLL}	Clock low time	40		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		1	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	15		ns
t_{CHDX}	t_{DH}	Data in hold time	15		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	15		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	20		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		25	ns
t_{CLQV}	t_V	Clock low to output valid		35	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		20	ns
t_{QHQL}(2)	t_{FO}	Output fall time		20	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		25	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		35	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Characterized only, not tested in production.

The values in the following table must not be considered for any new design.

Table 19. AC characteristics (M95080-W, device grade 6) End of life products: these values apply only to M95080-WMN6TP/S and M95080-WDW6TP/S devices)

Test conditions specified in *Table 9* and *Table 11*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
t_{CH}(1)	t_{CLH}	Clock high time	90		ns
t_{CL}(1)	t_{CLL}	Clock low time	90		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		1	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		50	ns
t_{QHQL}(2)	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Characterized only, not tested in production.

Figure 15. Serial input timing

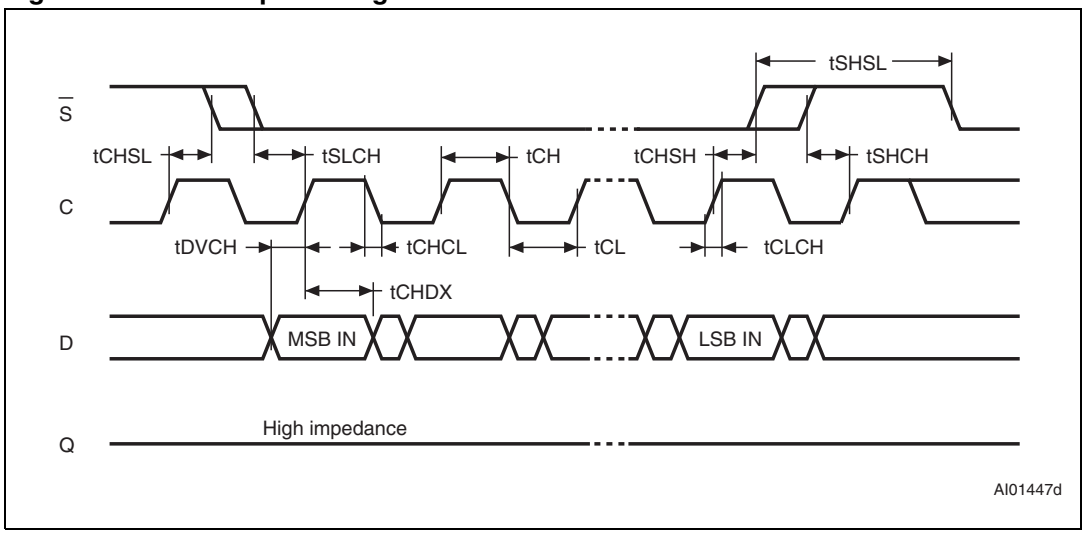


Figure 16. Hold timing

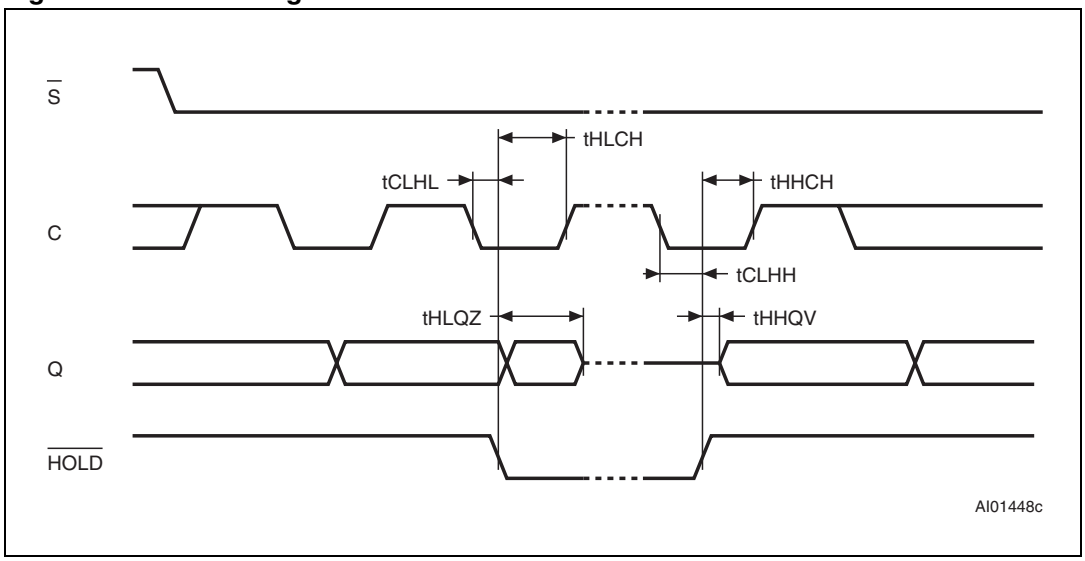
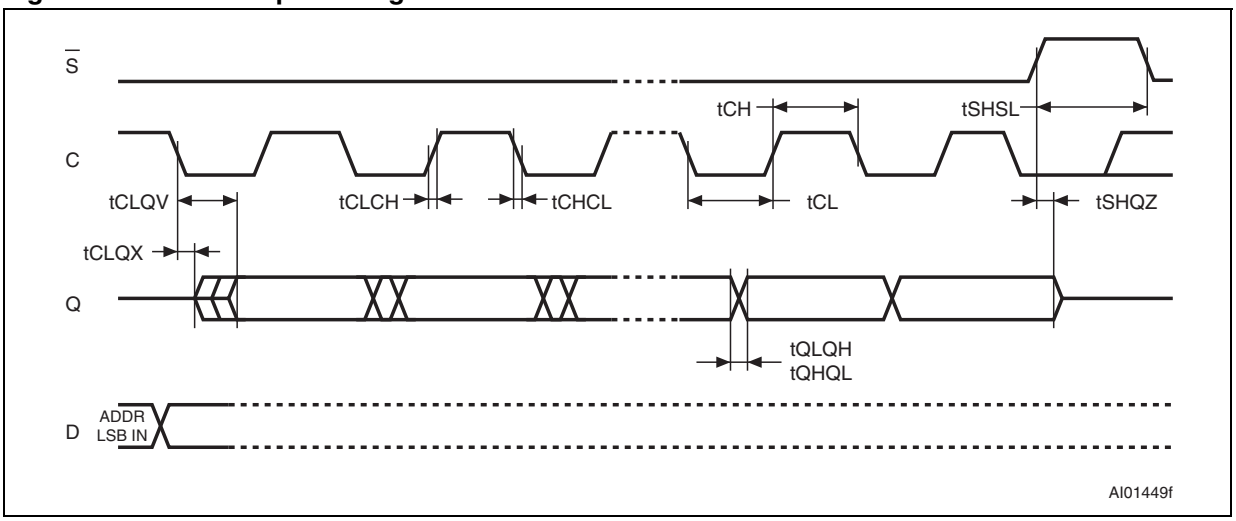


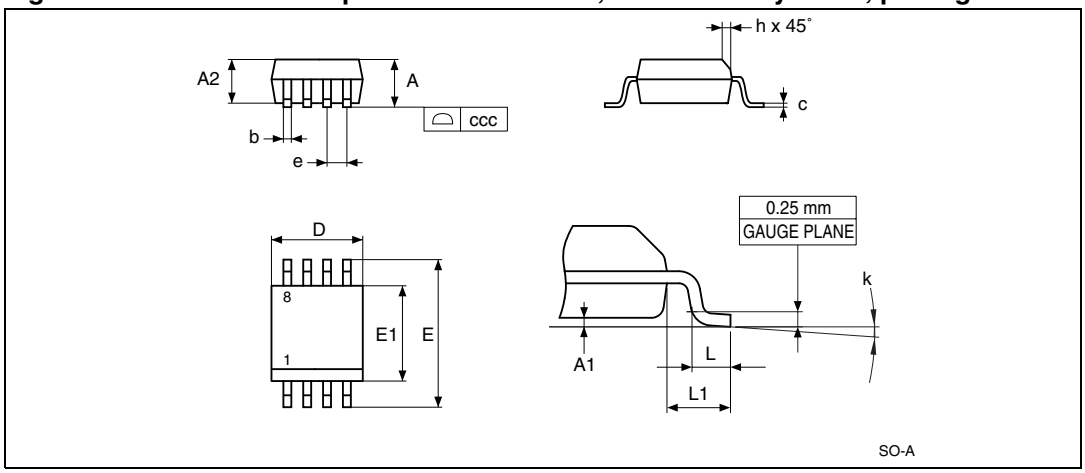
Figure 17. Serial output timing



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 18. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



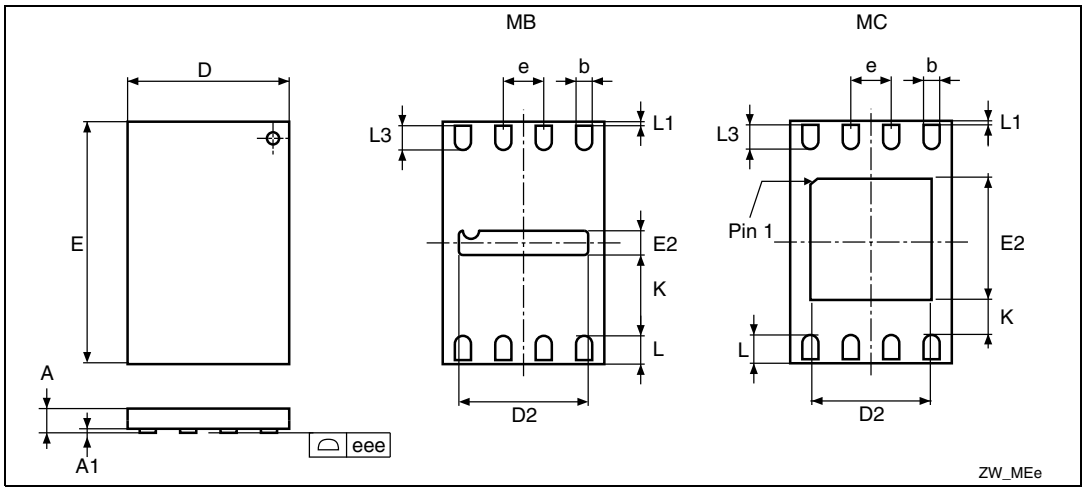
1. Drawing is not to scale.

Table 20. SO8N – 8-lead plastic small outline, 150 mils body width, mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.750			0.0689
A1		0.100	0.250		0.0039	0.0098
A2		1.250			0.0492	
b		0.280	0.480		0.0110	0.0189
c		0.170	0.230		0.0067	0.0091
ccc			0.100			0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270	-	-	0.0500	-	-
h		0.250	0.500		0.0098	0.0197
k		0°	8°		0°	8°
L		0.400	1.270		0.0157	0.0500
L1	1.040			0.0409		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 19. UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline



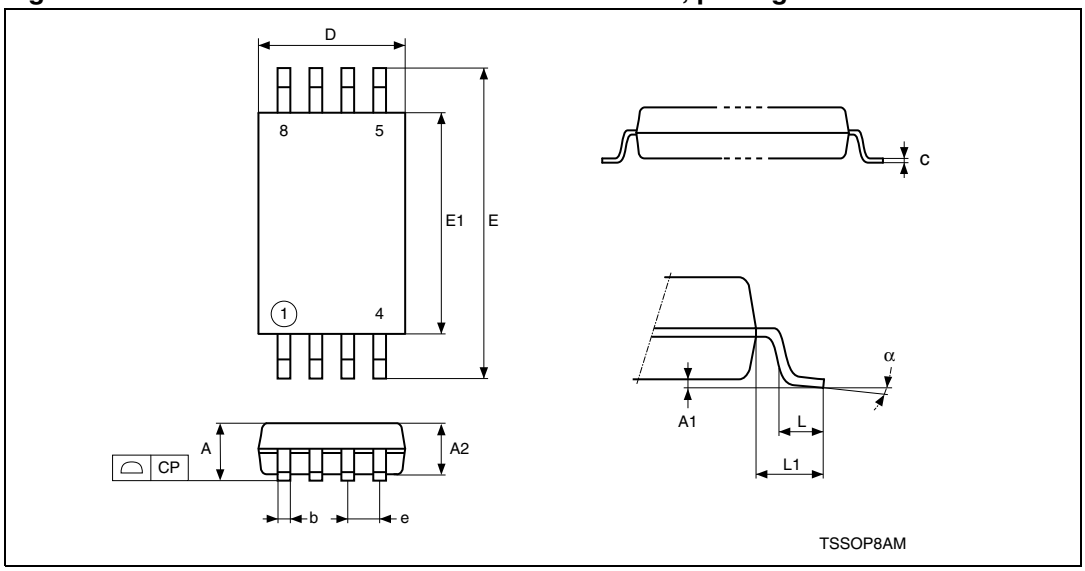
1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is internally pulled to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 21. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MB)	1.600	1.500	1.700	0.0630	0.0591	0.0669
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MB)	0.200	0.100	0.300	0.0079	0.0039	0.0118
E2 (rev MC)		1.200	1.600		0.0472	0.0630
e	0.500			0.0197		
K (rev MB)		0.800			0.0315	
K (rev MC)		0.300			0.0118	
L		0.300	0.500		0.0118	0.0197
L1			0.150			0.0059
L3		0.300			0.0118	
eee(2)		0.080			0.0031	

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

Figure 20. TSSOP8 – 8-lead thin shrink small outline, package outline



1. Drawing is not to scale.

Table 22. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°
N	8			8		

1. Values in inches are converted from mm and rounded to four decimal digits.

11 Part numbering

Table 23. Ordering information scheme

Example: M95080 W MN 6 T P /S

Device type

M95 = SPI serial access EEPROM

Device function

080 = 8 Kbit (1024 x 8)

Operating voltage

blank = V_{CC} = 4.5 to 5.5 V
W = V_{CC} = 2.5 to 5.5 V
R = V_{CC} = 1.8 to 5.5 V

Package

MN = SO8 (150 mil width)
DW = TSSOP8 (169 mil width)
MB or MC = UFDFPN8 (MLP8)

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

Option

blank = Standard packing
T = Tape and reel packing

Plating technology

G or P = RoHS compliant and halogen-free
(ECOPACK®)

Process(1)

/G or /S = Manufacturing technology code

1. The process letters appear on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office.

12 Revision history

Table 24. Document revision history

Date	Revision	Changes
22-Mar-2012	1	Initial release.

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M950x0-W M950x0-R

4 Kbit, 2 Kbit and 1 Kbit serial SPI bus EEPROM with high-speed clock

Datasheet - production data

SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

UFDFPN8 (MC)
2 x 3 mm

Features

- Compatible with SPI bus serial interface (Positive clock SPI modes)
- Single supply voltage:
  - 2.5 V to 5.5 V for M950x0-W
  - 1.8 V to 5.5 V for M950x0-R
- High speed 10 MHz clock rate, 5 ms write time
- Status register
- Byte and Page Write (up to 16 bytes)
- Self-timed programming cycle
- Adjustable size read-only EEPROM area
- Enhanced ESD protection
- More than 1 million write cycles
- More than 40-year data retention
- Packages RoHS-compliant and Halogen-free (ECOPACK2®)

Table 1. Device summary

Reference	Part number
M950x0-W	M95040-W
	M95020-W
	M95010-W
M950x0-R	M95040-R
	M95020-R
	M95010-R

Contents

List of tables

List of figures

1 Description

The M95010/ M95020/M95040 devices (M950x0) are electrically erasable programmable memories (EEPROMs) organized as 128/256/512 x 8 bits respectively, accessed through the SPI bus.

The M950x0 can operate over an ambient temperature range of -40 °C / +85 °C. and with the following supply voltage range: M950x0-W: 2.5 V to 5.5 V, and M950x0-R: 1.8 V to 5.5 V.

Figure 1. Logic diagram

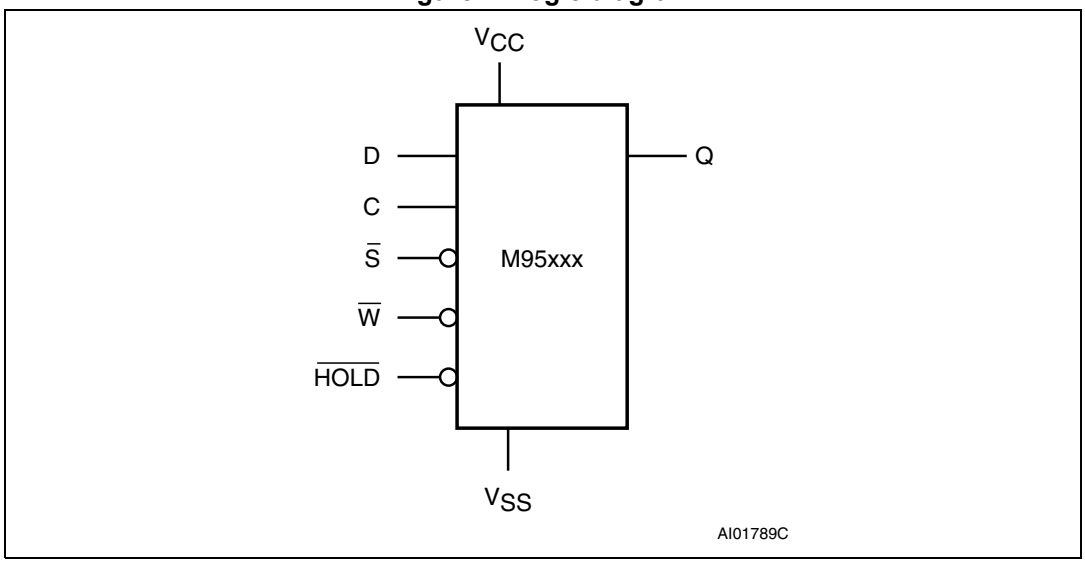
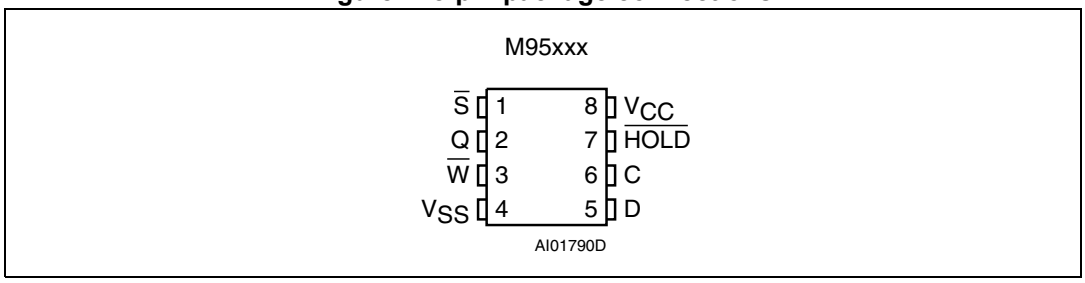


Figure 2. 8-pin package connections



1. See *Section 10: Package mechanical data* for package dimensions, and how to identify pin-1.

Table 2. Signal names

Signal name	Function
C	Serial Clock
D	Serial Data input
Q	Serial Data output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply voltage
V_{SS}	Ground

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals can be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Table 12: DC characteristics (M950x0-W, device grade 6)* and *Table 13: DC characteristics (M950x0-R, device grade 6)*. These signals are described next.

2.1 Serial Data Output (Q)

This output signal transfers data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data Input (D)

This input signal transfers data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

2.6 Write Protect ($\overline{W}$)

This input signal controls whether the memory is write protected. When Write Protect ($\overline{W}$) is held low, writes to the memory are disabled, but other operations remain enabled.
Write Protect ($\overline{W}$) must either be driven high or low, but must not be left floating.

2.7 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.8 Supply voltage (V_{CC})

2.8.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 8: Operating conditions (M950x0-W)* and *Table 9: Operating conditions (M950x0-R)*). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).
In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

2.8.2 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the internal reset threshold voltage (this threshold is defined in *Table 8: Operating conditions (M950x0-W)* and *Table 9: Operating conditions (M950x0-R)* as V_{RES}).

When V_{CC} passes over the POR threshold, the device is reset and is in the following state:

- Standby Power mode
- Deselected (note that, to be executed, an instruction must be preceded by a falling edge on Chip Select ($\overline{S}$))
- Status register value:
  - Write Enable Latch (WEL) is reset to 0
  - Write In Progress (WIP) is reset to 0
  - SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits)

When the device is in the above state, it must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range defined in *Table 8: Operating conditions (M950x0-W)* and *Table 9: Operating conditions (M950x0-R)*.

2.8.3 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 3: Bus master and memory devices on the SPI bus*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 8: Operating conditions (M950x0-W)* and *Table 9: Operating conditions (M950x0-R)* and the rise time must not vary faster than 1 V/µs.

2.8.4 Power-down

During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in *Table 8: Operating conditions (M950x0-W)* and *Table 9: Operating conditions (M950x0-R)*), the device must be:

- Deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC})
- In Standby Power mode (there should not be any internal write cycle in progress).

3 Connecting to the SPI bus

The device is fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

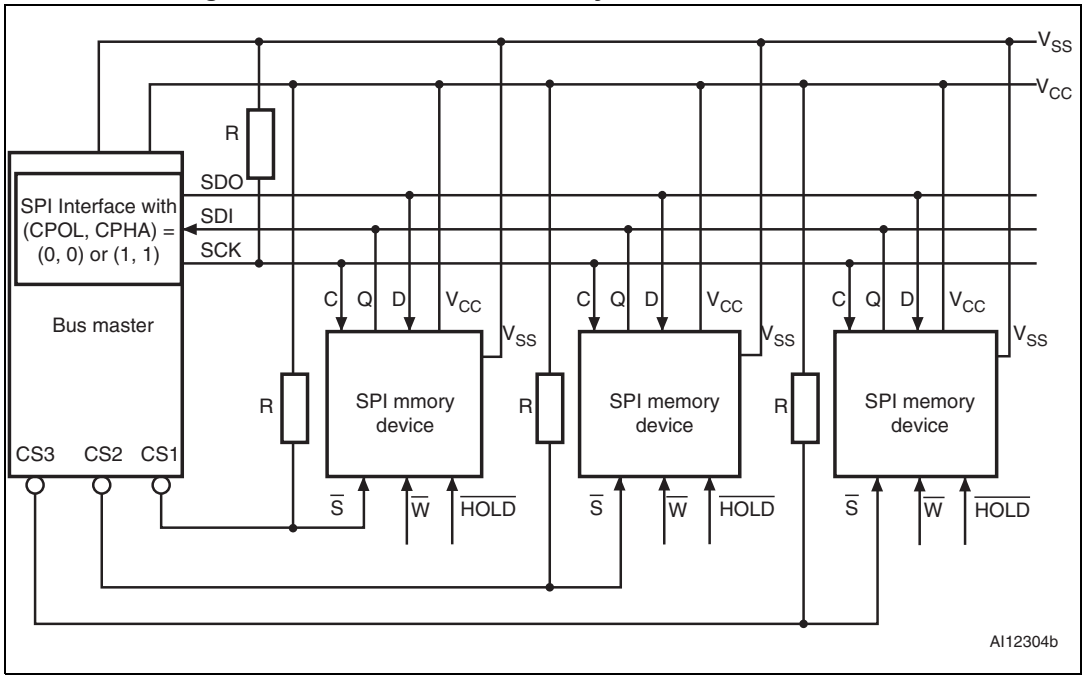
All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 3: Bus master and memory devices on the SPI bus shows an example of three memory devices connected to an MCU, on an SPI bus. Only one memory device is selected at a time, so only one memory device drives the Serial Data output (Q) line at a time, the other memory devices are high impedance.

The pull-up resistor R (represented in *Figure 3: Bus master and memory devices on the SPI bus*) ensures that a device is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state.

In applications where the bus master might enter a state where all SPI bus inputs/outputs would be in high impedance at the same time (for example, if the bus master is reset during the transmission of an Instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high): this ensures that $\overline{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met. The typical value of R is 100 kΩ..

Figure 3. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

3.1 SPI modes

The device can be driven by a microcontroller with its SPI peripheral running in either of the following modes:

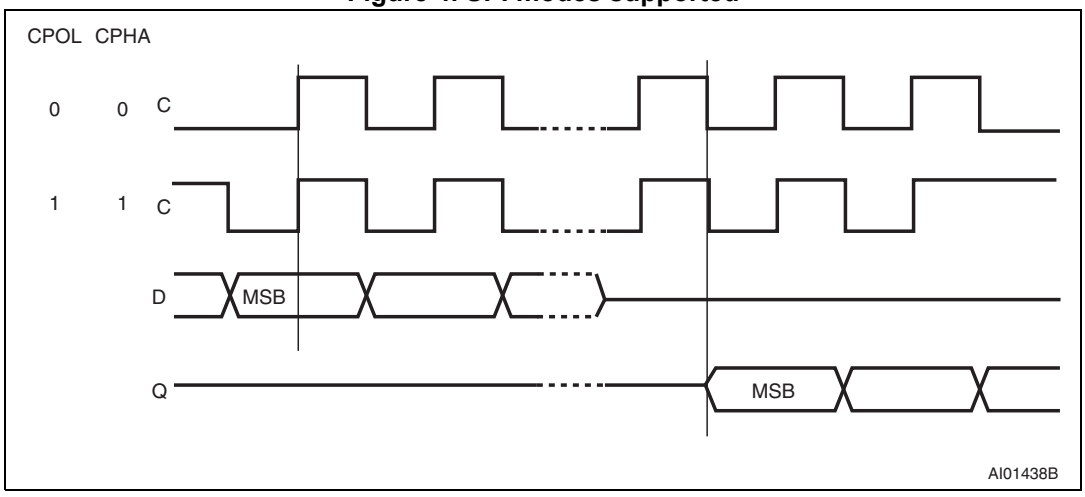
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4: SPI modes supported*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. SPI modes supported



4 Operating features

4.1 Hold condition

The Hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{\text{S}}$) low.

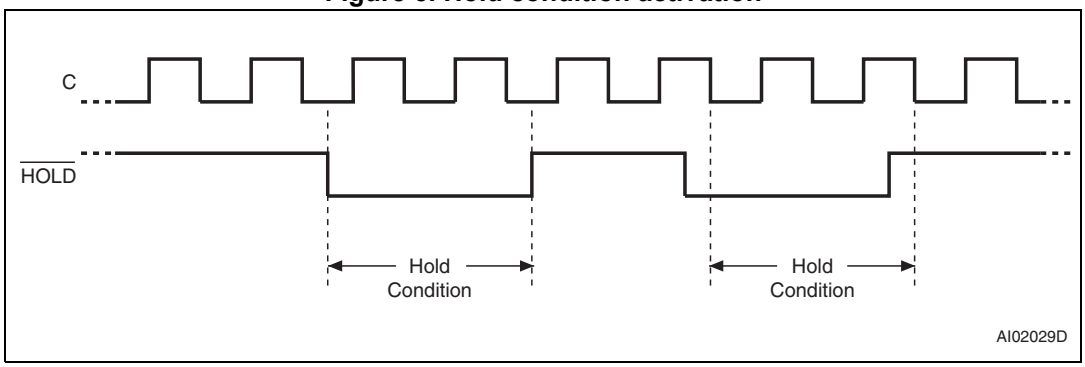
Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{\text{HOLD}}$) signal is driven low at the same time as Serial Clock (C) already being low (as shown in *Figure 5: Hold condition activation*).

The Hold condition ends when the Hold ($\overline{\text{HOLD}}$) signal is driven high at the same time as Serial Clock (C) already being low.

Figure 5: Hold condition activation also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

Figure 5. Hold condition activation



4.2 Status register

Figure 6: Block diagram shows the position of the Status register in the control logic of the device. This register contains a number of control bits and status bits, as shown in *Table 5: Status register format* and as detailed in *Section 6.3: Read Status Register (RDSR)*.

4.3 Data protection and protocol control

To help protect the device from data corruption in noisy or poorly controlled environments, a number of safety features have been built in to the device. The main security measures can be summarized as follows:

- WEL bit is reset at power-up.
- Chip Select ($\overline{S}$) must rise after the eighth clock count (or multiple thereof) in order to start a non-volatile Write cycle (in the memory array or in the Status register).
- Accesses to the memory array are ignored during the non-volatile programming cycle, and the programming cycle continues unaffected.
- Invalid Chip Select ($\overline{S}$) and Hold ($\overline{HOLD}$) transitions are ignored.

For any instruction to be accepted and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches the last bit of the instruction, and before the next rising edge of Serial Clock (C).

For this, “the last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except in the case of RDSR and READ instructions). Moreover, the “next rising edge of CLOCK” might (or might not) be the next bus transaction for some other device on the bus.

When a Write cycle is in progress, the device protects it against external interruption by ignoring any subsequent READ, WRITE or WRSR instruction until the present cycle is complete.

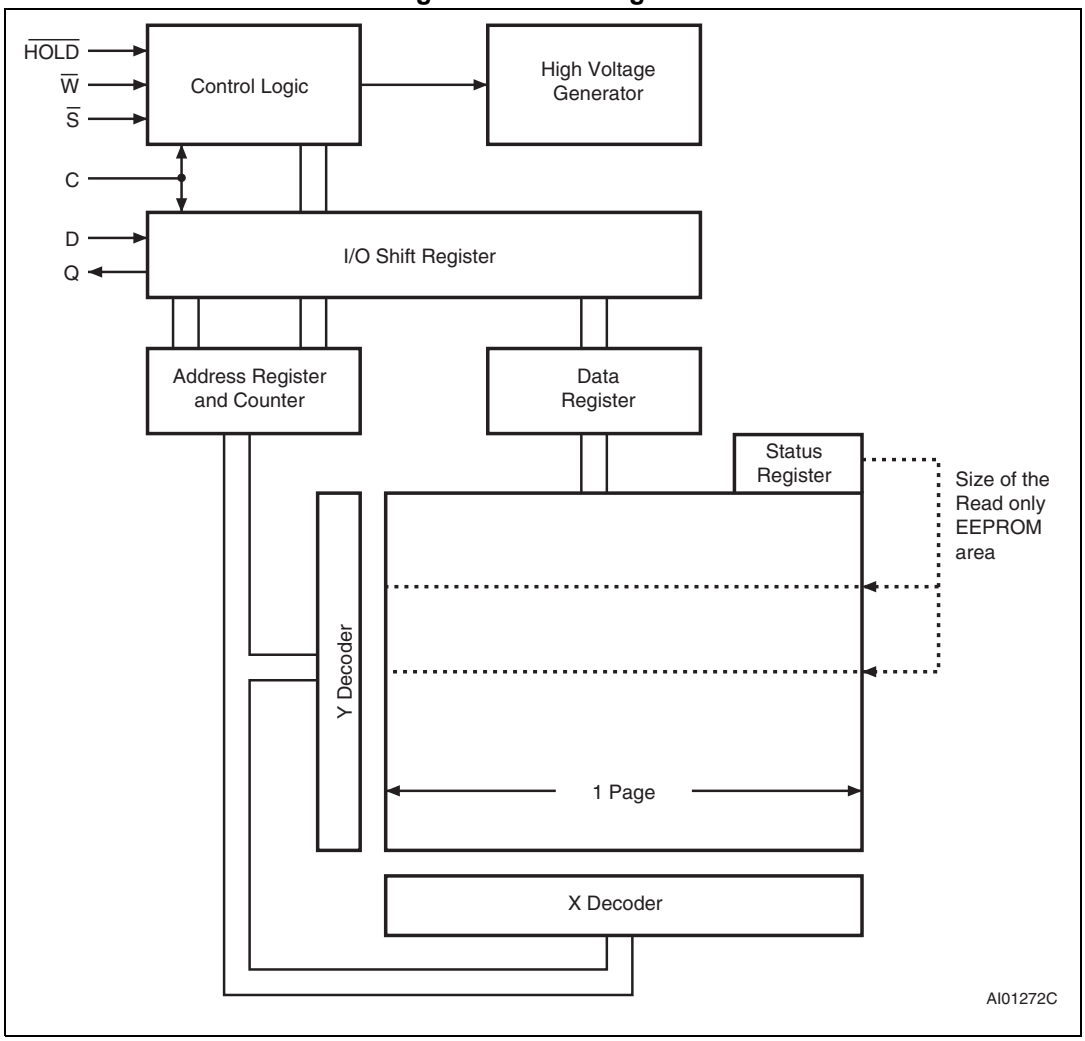
Table 3. Write-protected block size

Status register bits		Protected block	Protected array addresses		
BP1	BP0		M95040	M95020	M95010
0	0	none	none	none	none
0	1	Upper quarter	180h - 1FFh	C0h - FFh	60h - 7Fh
1	0	Upper half	100h - 1FFh	80h - FFh	40h - 7Fh
1	1	Whole memory	000h - 1FFh	00h - FFh	00h - 7Fh

5 Memory organization

The memory is organized as shown in *Figure 6: Block diagram*.

Figure 6. Block diagram



6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 4: Instruction set*.

If an invalid instruction is sent (one not contained in *Table 4: Instruction set*), the device automatically deselects itself.

Table 4. Instruction set

Instruction	Description	Instruction Format
WREN	Write Enable	0000 X110(1)
WRDI	Write Disable	0000 X100(1)
RDSR	Read Status Register	0000 X101(1)
WRSR	Write Status Register	0000 X001(1)
READ	Read from Memory Array	0000 $A_8$011(2)
WRITE	Write to Memory Array	0000 $A_8$010(2)

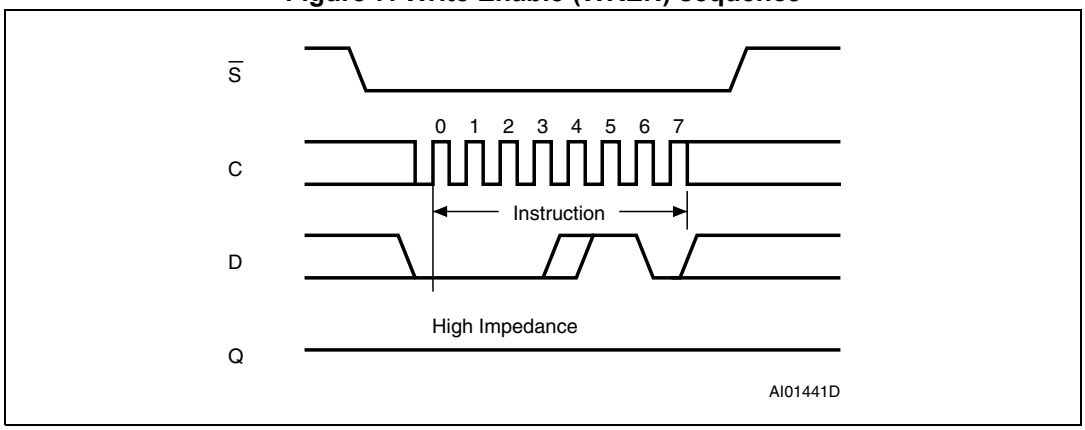
1. X = Don't Care.
2. A_8 = 1 for the upper half of the memory array of the M95040, and 0 for the lower half, and is Don't Care for other devices.

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 7: Write Enable (WREN) sequence*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 7. Write Enable (WREN) sequence



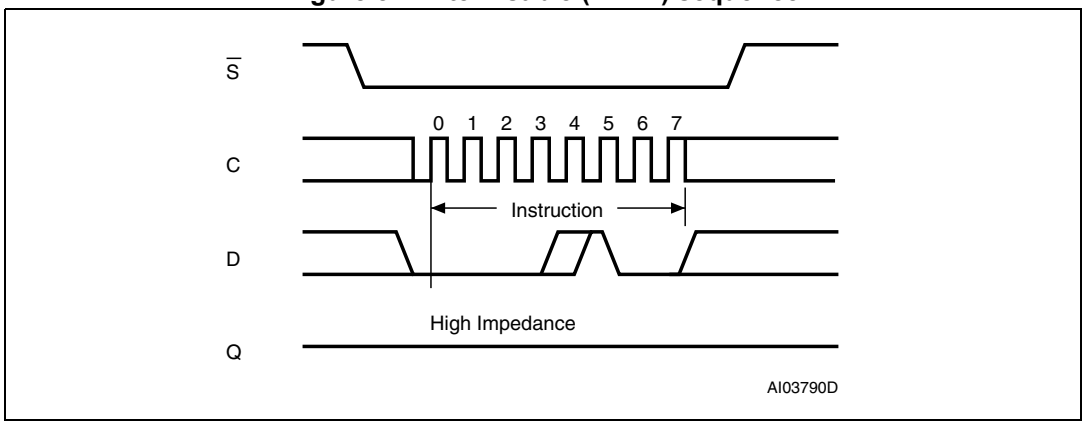
6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device. As shown in *Figure 8: Write Disable (WRDI) sequence*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit is reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion
- Write Protect ($\overline{W}$) line being held low.

Figure 8. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register instruction is used to read the Status Register.

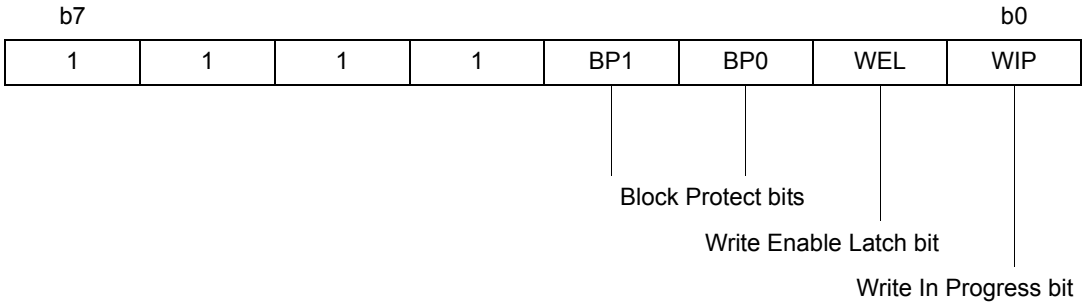
As shown in *Figure 9*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte are then shifted in, on Serial Data Input (D). The current state of the bits in the Status register is shifted out, on Serial Data Out (Q). The Read Cycle is terminated by driving Chip Select ($\overline{S}$) high.

The Status Register is always readable, even if a Write or Write Status Register cycle is in progress. During a Write Status Register cycle, the values of the non-volatile bits (BP0, BP1) become available when a new RDSR instruction is executed, after completion of the Write cycle. On the other hand, the two read-only bits (Write Enable Latch (WEL), Write In Progress (WIP)) are dynamically updated during the ongoing Write cycle.

It is possible to read the Status Register contents continuously, as described in *Figure 9*.

Bits b7, b6, b5 and b4 are always read as 1. The status and control bits of the Status register are as follows:

Table 5. Status register format



6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

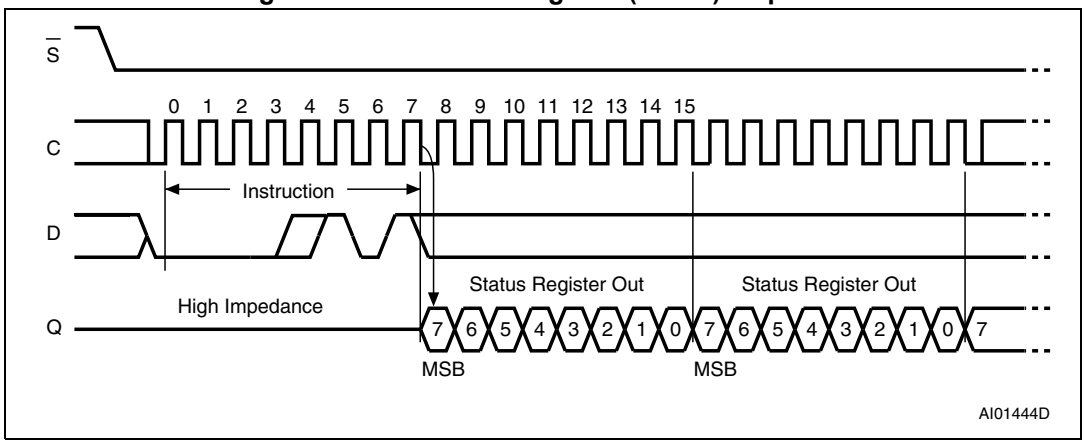
6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 3: Write-protected block size*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

Figure 9. Read Status Register (RDSR) sequence



6.4 Write Status Register (WRSR)

A Write Status Register (WRSR) instruction allows new values to be written to the Status register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed.

The WRSR instruction is entered by driving Chip Select ($\overline{S}$) low, sending the instruction code followed by the data byte on Serial Data input (D), and driving the Chip Select ($\overline{S}$) signal high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the WRSR instruction is not executed.

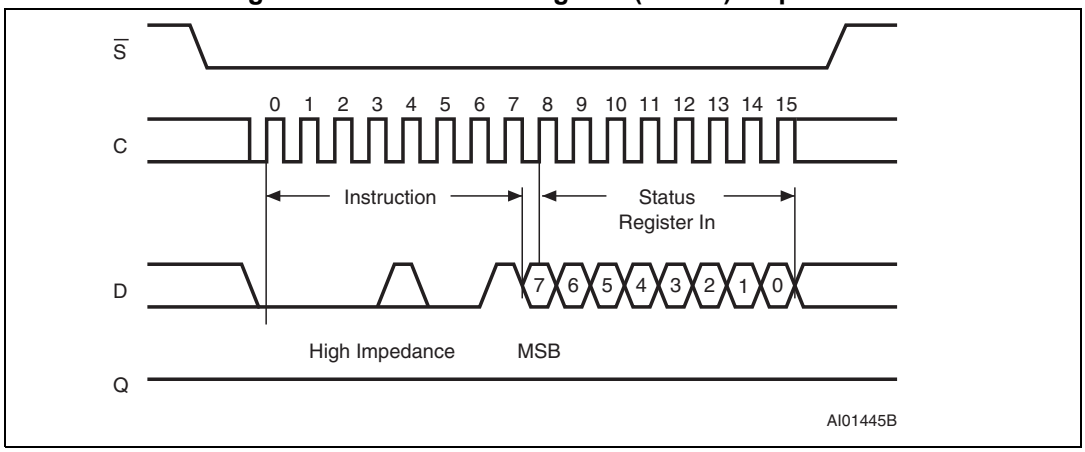
Driving the Chip Select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed write cycle that takes t_W to complete (as specified in *Table 12: DC characteristics (M950x0-W, device grade 6)* to *Table 15: AC characteristics (M950x0-R, device grade 6)*). The instruction sequence is shown in *Figure 10: Write Status Register (WRSR) sequence*.

While the Write Status Register cycle is in progress, the Status register may still be read to check the value of the Write in progress (WIP) bit: the WIP bit is 1 during the self-timed write cycle t_W, and, 0 when the write cycle is complete. The WEL bit (Write enable latch) is also reset at the end of the write cycle t_W.

The WRSR instruction allows the user to change the values of the BP1, BP0 bits which define the size of the area that is to be treated as read only, as defined in *Table 3: Write-protected block size*. The contents of the BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W write cycle.

The WRSR instruction has no effect on the b7, b6, b5, b4, b1 and b0 bits in the Status register which are always read as 0.

Figure 10. Write Status Register (WRSR) sequence



The WRSR instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, after the eighth bit, b0, of the data byte has been latched in
- if Write Protect ($\overline{W}$) is low during the WRSR command (instruction, address and data)

6.5 Read from Memory Array (READ)

As shown in *Figure 11: Read from Memory Array (READ) sequence*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address byte are then shifted in, on Serial Data Input (D). For the M95040, the most significant address bit, A8, is incorporated as bit b3 of the instruction byte, as shown in *Table 4: Instruction set*. The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, an internal bit-pointer is automatically incremented at each clock cycle, and the corresponding data bit is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

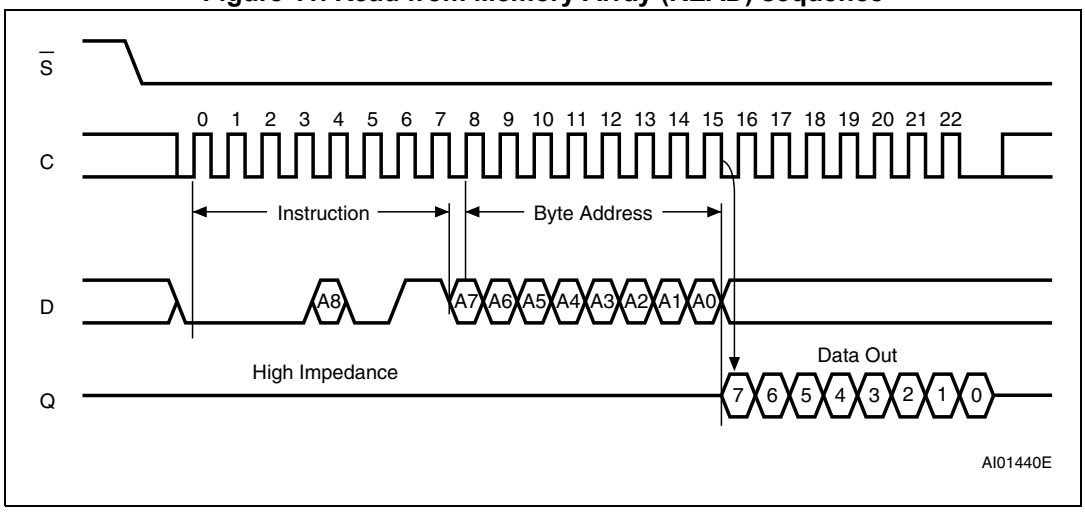
The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Table 6. Address range bits

Device	M95040	M95020	M95010
Address Bits	A8-A0	A7-A0	A6-A0

Figure 11. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in *Table 6: Address range bits*, the most significant address bits are Don't Care.

6.6 Write to Memory Array (WRITE)

As shown in *Figure 12: Byte Write (WRITE) sequence*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data input (D). The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed Write cycle, triggered by the rising edge of Chip Select ($\overline{S}$), continues for a period t_W (as specified in *Table 12: DC characteristics (M950x0-W, device grade 6)* to *Table 15: AC characteristics (M950x0-R, device grade 6)*). After this time, the Write in Progress (WIP) bit is reset to 0.

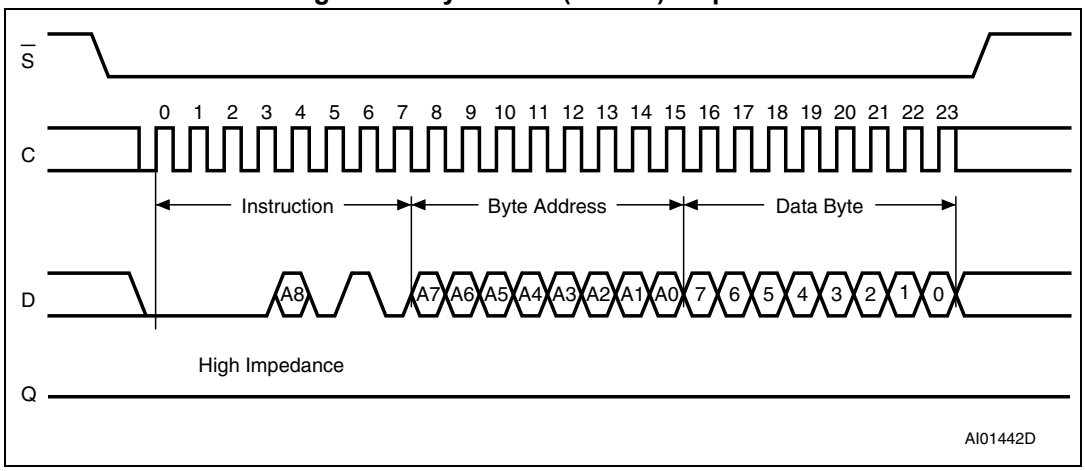
In the case of *Figure 12: Byte Write (WRITE) sequence*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. If, though, Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 13: Page Write (WRITE) sequence*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle. If Chip Select ($\overline{S}$) still continues to be driven low, the next byte of input data is shifted in, and used to overwrite the byte at the start of the current page.

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the rising edge of Serial Clock (C) that latches the last data bit, and before the next rising edge of Serial Clock (C) occurs anywhere on the bus)
- if Write Protect ($\overline{W}$) is low or if the addressed page is in the area protected by the Block Protect (BP1 and BP0) bits

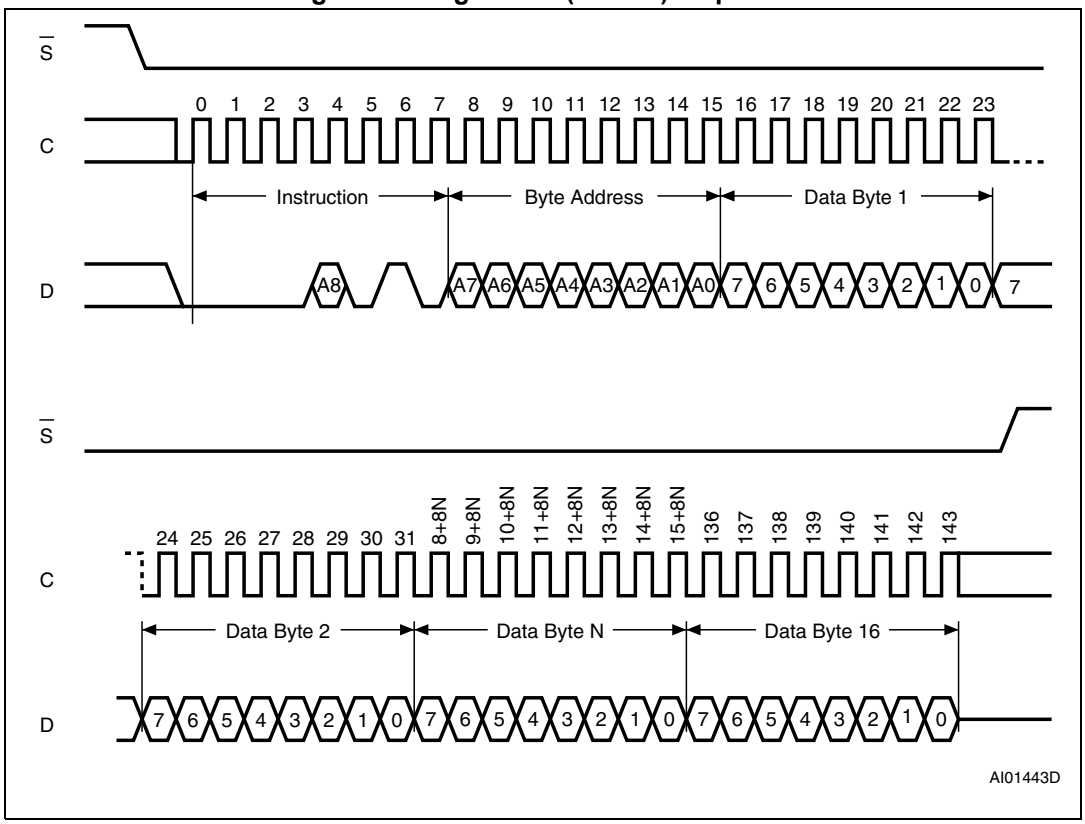
Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 12. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 6: Address range bits*, the most significant address bits are Don't Care.

Figure 13. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 6: Address range bits*, the most significant address bits are Don't Care.

7 Power-up and delivery states

7.1 Power-up state

After Power-up, the device is in the following state:

- Low power Standby Power mode
- Deselected (after Power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started)
- Not in Hold Condition
- Write Enable Latch (WEL) is reset to 0
- Write In Progress (WIP) is reset to 0

The BP1 and BP0 bits of the Status register are unchanged from the previous power-down (they are non-volatile bits).

7.2 Initial delivery state

The device is delivered with the memory array set at all 1s (FFh).
The Block Protect (BP1 and BP0) bits are initialized to 0.

8 Maximum rating

Stressing the device outside the ratings listed in *Table 7: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
V_O	Output voltage	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	V_{CC}+1.0	V
I_{OL}	DC output current (Q = 0)	-	5	mA
I_{IH}	DC output current (Q = 1)	-	5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body Model) voltage(2)	-	4000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2011/65/EU.
2. Positive and negative pulses applied on pin pairs, according to the AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100pF, R1=1500 Ω, R2=500 Ω).

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 8. Operating conditions (M950x0-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C

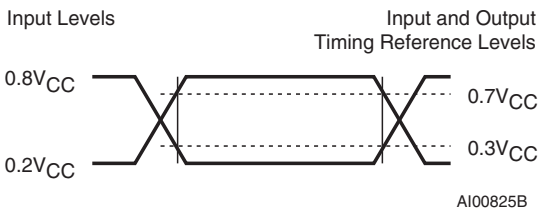
Table 9. Operating conditions (M950x0-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 10. AC test measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times	-	50	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 14. AC test measurement I/O waveform(1)



1. Output Hi-Z is defined as the point where data out is no longer driven.

Table 11. Capacitance (1)

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V	-	8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V	-	8	pF
	Input capacitance (other pins)	V_{IN} = 0 V	-	6	pF

1. Sampled only, not 100% tested, at TA=25 °C and a frequency of 5 MHz

.

Table 12. DC characteristics (M950x0-W, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}	-	± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}	-	± 2	µA
I_{CC}	Supply current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open	-	2	mA
I_{CC1}	Supply current (Standby Power mode)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} V_{CC} = 2.5 V	-	1	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V	-	0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}	-	V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not 100% tested.

Table 13. DC characteristics (M950x0-R, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}	-	± 2	µA
I_{LO}	Output leakage current	S = V_{CC}, voltage applied on Q = V_{SS} or V_{CC}	-	± 2	µA
I_{CCR}	Supply current (Read)	V_{CC} = 2.5 V, C = 0.1 V_{CC} or 0.9V_{CC}, f_C = 5 MHz, Q = open	-	3	mA
		V_{CC} = 1.8 V, C = 0.1V_{CC} or 0.9V_{CC} at max clock frequency, Q = open	-	2	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 5.0 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	2	µA
		V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	1	µA
		V_{CC} = 1.8 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	1	µA
V_{IL}	Input low voltage	2.5 V < V_{CC} < 5.5 V	–0.45	0.3V_{CC}	V
		1.8 V < V_{CC} < 2.5 V	–0.45	0.25V_{CC}	V
V_{IH}	Input high voltage	2.5 V < V_{CC} < 5.5 V	0.7V_{CC}	V_{CC}+1	V
		1.8 V < V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	V_{CC} = 2.5 V, I_{OL} = 1.5 mA, or V_{CC} = 5.5 V, I_{OL} = 2 mA	-	0.2V_{CC}	V
		V_{CC} = 1.8 V, I_{OL} = 0.15 mA	-	0.3	V
V_{OH}	Output high voltage	V_{CC} = 2.5 V, I_{OH} = –0.4 mA, or V_{CC} = 5.5 V, I_{OH} = –2 mA, or V_{CC} = 1.8 V, I_{OH} = –0.1 mA	0.8V_{CC}	-	V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not 100% tested.

Table 14. AC characteristics (M950x0-W, device grade 6)

Test conditions specified in *Table 10* and *Table 8*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	15	-	ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	15	-	ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40	-	ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	25	-	ns
t_{CHSL}		$\overline{S}$ not active hold time	15	-	ns
t_{CH}(1)	t_{CLH}	Clock high time	40	-	ns
t_{CL}(1)	t_{CLL}	Clock low time	40	-	ns
t_{CLCH}(2)	t_{RC}	Clock rise time	-	1	µs
t_{CHCL}(2)	t_{FC}	Clock fall time	-	1	µs
t_{DVCH}	t_{DSU}	Data in setup time	15	-	ns
t_{CHDX}	t_{DH}	Data in hold time	15	-	ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	15	-	ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	20	-	ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0	-	ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0	-	ns
t_{SHQZ}(2)	t_{DIS}	Output disable time	-	25	ns
t_{CLQV}	t_V	Clock low to output valid	-	35	ns
t_{CLQX}	t_{HO}	Output hold time	0	-	ns
t_{QLQH}(2)	t_{RO}	Output rise time	-	20	ns
t_{QHQL}(2)	t_{FO}	Output fall time	-	20	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid	-	25	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z	-	35	ns
t_W	t_{WC}	Write time	-	5	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$
2. Value guaranteed by characterization, not 100% tested in production.

Table 15. AC characteristics (M950x0-R, device grade 6)

Test conditions specified in *Table 10* and *Table 9*[1]					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90	-	ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90	-	ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100	-	ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90	-	ns
t_{CHSL}		$\overline{S}$ not active hold time	90	-	ns
t_{CH}[2]	t_{CLH}	Clock high time	90	-	ns
t_{CL}[1]	t_{CLL}	Clock low time	90	-	ns
t_{CLCH}[3]	t_{RC}	Clock rise time	-	1	µs
t_{CHCL}[2]	t_{FC}	Clock fall time	-	1	µs
t_{DVCH}	t_{DSU}	Data in setup time	20	-	ns
t_{CHDX}	t_{DH}	Data in hold time	30	-	ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70	-	ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40	-	ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0	-	ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0	-	ns
t_{SHQZ}[2]	t_{DIS}	Output disable time	-	100	ns
t_{CLQV}	t_V	Clock low to output valid	-	80	ns
t_{CLQX}	t_{HO}	Output hold time	0	-	ns
t_{QLQH}[2]	t_{RO}	Output rise time	-	50	ns
t_{QHQL}[2]	t_{FO}	Output fall time	-	50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid	-	50	ns
t_{HLQZ}[2]	t_{HZ}	$\overline{HOLD}$ low to output high-Z	-	100	ns
t_W	t_{WC}	Write time	-	5	ms

1. The test flow guarantees the AC parameter values defined in this table (when V_{CC} = 1.8 V) and the AC parameter values defined in *Table 14: AC characteristics (M950x0-W, device grade 6)* (when V_{CC} = 2.5 or when V_{CC} = 5.0 V).
2. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, 1 / f_C(max)
3. Value guaranteed by characterization, not 100% tested in production.

Figure 15. Serial input timing

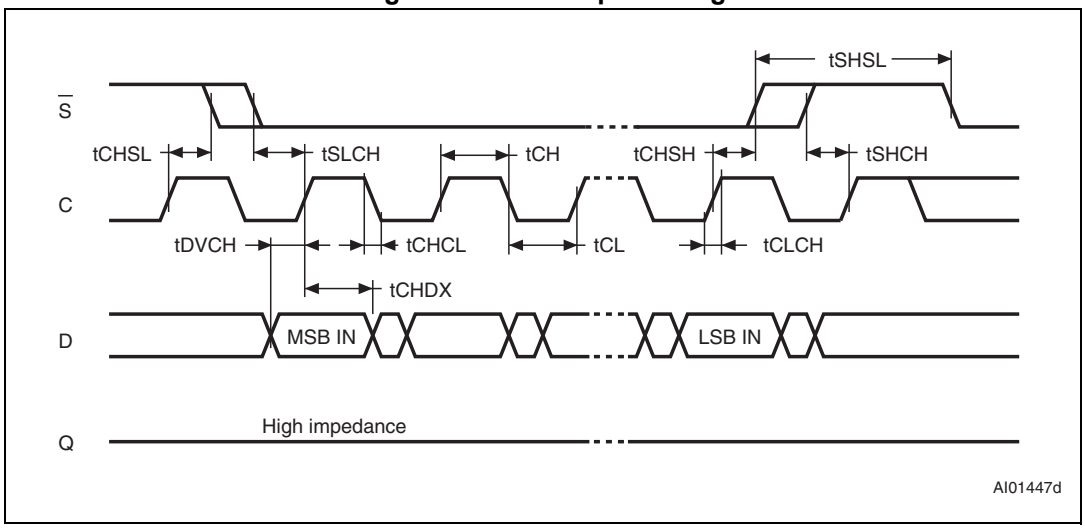


Figure 16. Hold timing

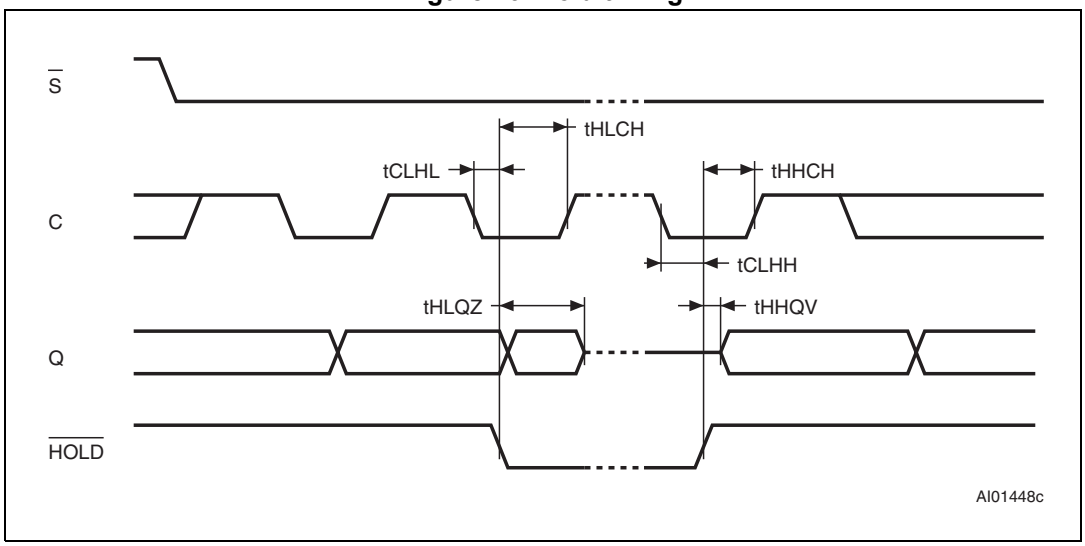
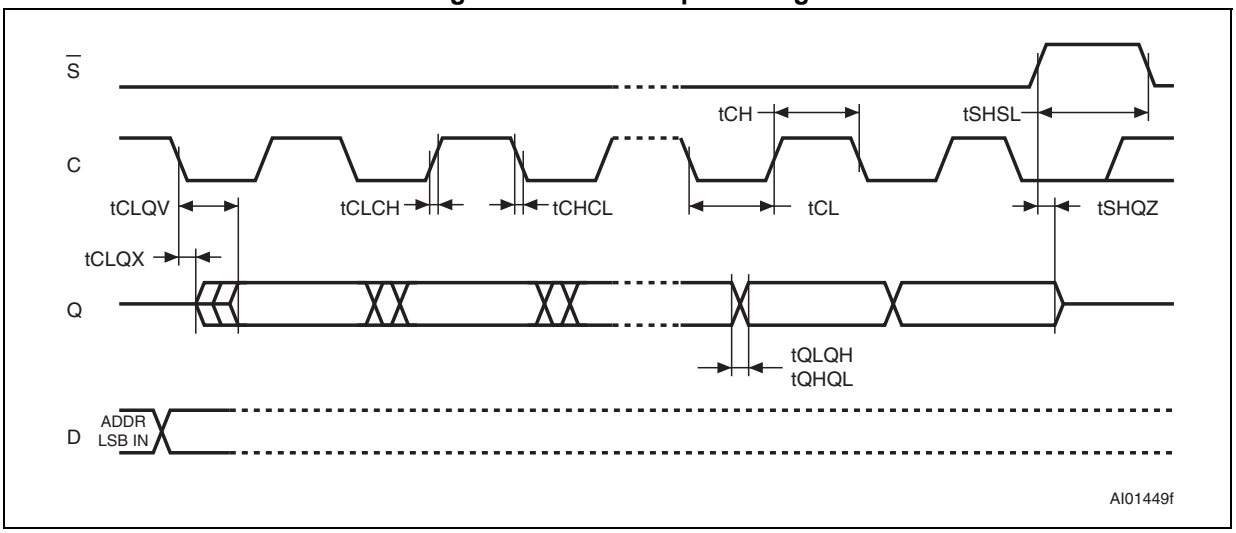


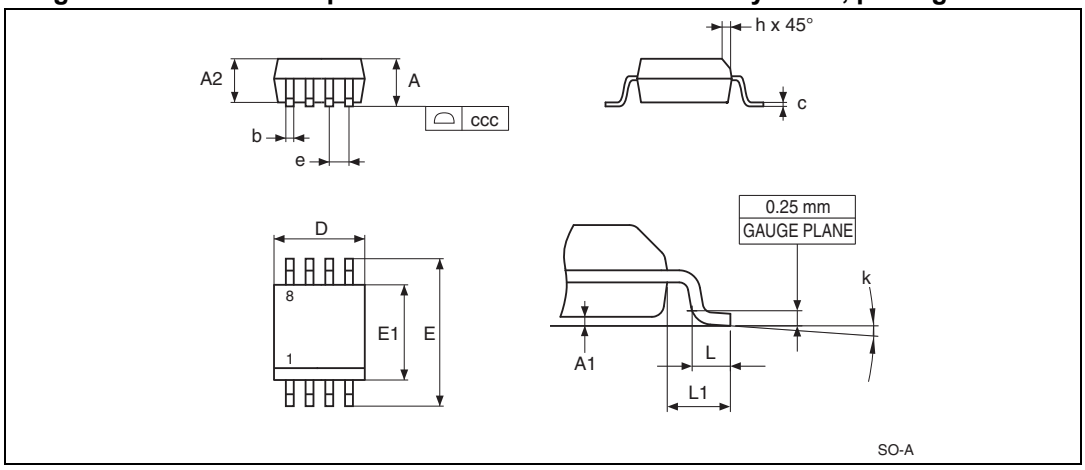
Figure 17. Serial output timing



10 Package mechanical data

In order to meet environmental requirements, ST offers the device in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 18. SO8N 8-lead plastic small outline 150 mils body width, package outline



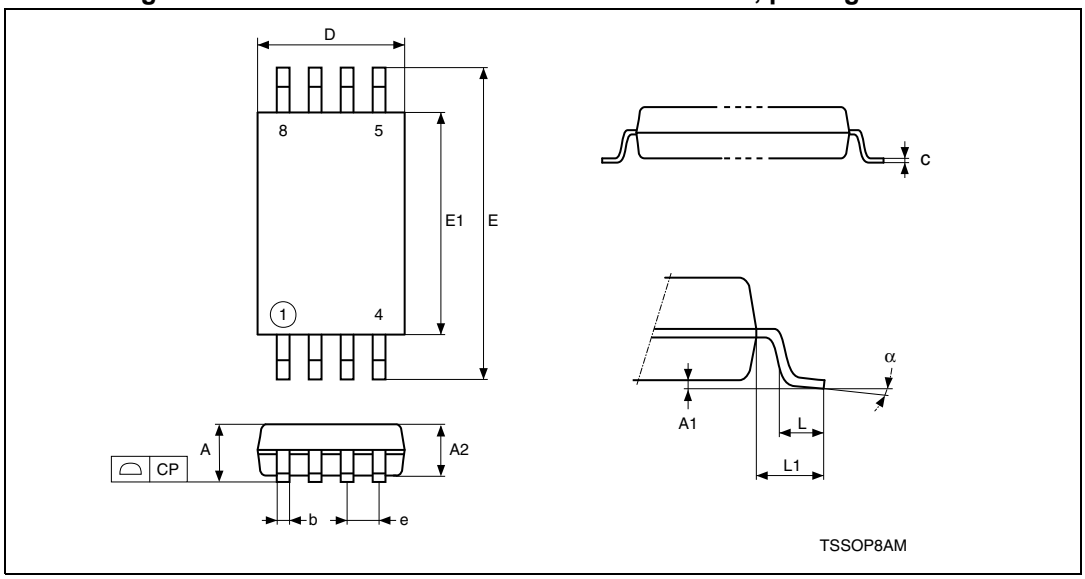
1. Drawing is not to scale.

Table 16. SO8N 8-lead plastic small outline, 150 mils body width, package mechanical data

Symbol	Millimeters			Inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.75	-	-	0.0689
A1	-	0.1	0.25	-	0.0039	0.0098
A2	-	1.25	-	-	0.0492	-
b	-	0.28	0.48	-	0.011	0.0189
c	-	0.17	0.23	-	0.0067	0.0091
ccc	-	-	0.1	-	-	0.0039
D	4.9	4.8	5	0.1929	0.189	0.1969
E	6	5.8	6.2	0.2362	0.2283	0.2441
E1	3.9	3.8	4	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h	-	0.25	0.5	-	0.0098	0.0197
k	-	0°	8°	-	0°	8°
L	-	0.4	1.27	-	0.0157	0.05
L1	1.04	-	-	0.0409	-	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 19. TSSOP8 8-lead thin shrink small outline, package outline



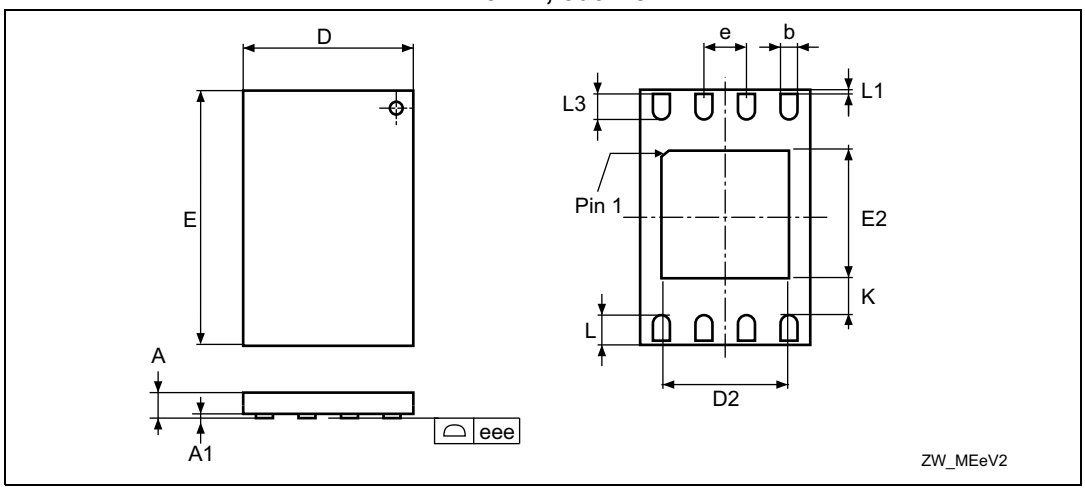
1. Drawing is not to scale.

Table 17. TSSOP8 8-lead thin shrink small outline, package mechanical data

Symbol	Millimeters			Inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.2	-	-	0.0472
A1	-	0.05	0.15	-	0.002	0.0059
A2	1	0.8	1.05	0.0394	0.0315	0.0413
b	-	0.19	0.3	-	0.0075	0.0118
c	-	0.09	0.2	-	0.0035	0.0079
CP	-	-	0.1	-	-	0.0039
D	3	2.9	3.1	0.1181	0.1142	0.122
e	0.65	-	-	0.0256	-	-
E	6.4	6.2	6.6	0.252	0.2441	0.2598
E1	4.4	4.3	4.5	0.1732	0.1693	0.1772
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1	-	-	0.0394	-	-
α	-	0°	8°	-	0°	8°
N (number of leads)	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 20. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, outline



1. Drawing is not to scale.
2. The central pad (area E2 by D2 in the above illustration) is pulled, internally, to V_{SS}. It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.
3. The circle in the top view of the package indicates the position of pin 1.

Table 18. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, data

Symbol	Millimeters			Inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MC)	-	1.200	1.600	-	0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MC)	-	1.200	1.600	-	0.0472	0.0630
e	0.500	-	-	0.0197	-	-
K (rev MC)	-	0.300	-	-	0.0118	-
L	-	0.300	0.500	-	0.0118	0.0197
L1	-	-	0.150	-	-	0.0059
L3	-	0.300	-	-	0.0118	-
eee[2]	-	0.080	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

11 Part numbering

Table 19. Ordering information scheme

Example: M95040 – W MN 6 T P

Device type
M95 = SPI serial access EEPROM

Device function
040 = 4 Kbit (512 x 8)
020 = 2 Kbit (256 x 8)
010 = 1 Kbit (128 x 8)

Operating voltage
W = V_{CC} = 2.5 to 5.5V
R = V_{CC} = 1.8 to 5.5V

Package
MN = SO8 (150 mil width)
DW = TSSOP8 (169 mil width)
MC = UFDFPN8 (MLP8) 2 × 3mm

Device grade
6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

Option
blank = Standard packing
T = Tape and reel packing

Plating technology
P or G = ECOPACK® (RoHS compliant)

12 Revision history

Table 20. Document revision history

Date	Version	Changes
10-May-2000	2.2	s/issuing three bytes/issuing two bytes/ in the 2nd sentence of the Byte Write Operation
16-Mar-2001	2.3	Human Body Model meets JEDEC std (Table 2). Minor adjustments to Figs 7,9,10,11 & Tab 9. Wording changes, according to the standard glossary Illustrations and Package Mechanical data updated
19-Jul-2001	2.4	Temperature range ‘3’ added to the -W supply voltage range in DC and AC characteristics
11-Oct-2001	3.0	Document reformatted using the new template
26-Feb-2002	3.1	Description of chip deselect after 8th clock pulse made more explicit
27-Sep-2002	3.2	Position of A8 in Read Instruction Sequence Figure corrected. Load Capacitance C_L changed
24-Oct-2002	3.3	Minimum values for tCHHL and tCHHH changed.
24-Feb-2003	3.4	Description of Read from Memory Array (READ) instruction corrected, and clarified
28-May-2003	3.5	New products, identified by the process letter W, added
25-Jun-2003	3.6	Correction to current products, identified by the process letter K not L. I_{CC} changed in DC characteristics, and t_{CHHL}, t_{CHHH} substituted in AC characteristics Voltage range -S upgraded by removing it, and adding the -R voltage range in its place Temperature range 5 removed.
21-Nov-2003	4.0	Table of contents, and Pb-free options added. V_{IL}(min) improved to -0.45V
02-Feb-2004	4.1	V_{IL}(max) and t_{CLQV}(max) changed
01-Mar-2004	5.0	Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) improved. Soldering temperature information clarified for RoHS compliant devices. New 5V and 2.5V devices, with process letter W, promoted from preliminary data to full data. Device Grade 3 clarified, with reference to HRCF and automotive environments
05-Oct-2004	6.0	Product List summary table added. Process identification letter “G” information added. Order information for Tape and Reel changed to T. AEC-Q100-002 compliance. Device Grade information clarified. tHHQX corrected to tHHQV. Signal Description updated. 10MHz, 5ms Write is now the present product. tCH+tCL<1/fC constraint clarified

Table 20. Document revision history

Date	Version	Changes
06-Nov-2006	7	Document converted to new template, *Table 5: Status register format* moved to below *Section 6.3: Read Status Register (RDSR)*. PDIP package removed. UFDFPN8 (MB) package added (see *Figure 20* and *Table 18*) and SO8N package specifications updated (see *Figure 18* and *Table 16*). Packages are ECOPACK® compliant. *Section 6.7: Cycling* added. *Section 2.8: Supply voltage (VCC)* added and information removed below *Section 4: Operating features*. *Figure 3: Bus master and memory devices on the SPI bus* modified. T_{LEAD} parameter modified, *Note 1* changed, and T_A added to *Table 7: Absolute maximum ratings*. Characteristics of previous product identified by process letter K removed. CL modified in *Table 10: AC test measurement conditions*. Note removed below *Table 13*. Information in *Table 13* is no longer Preliminary data, I_{CC}, I_{CC1} and V_{IL} modified. End timing line of t_{SHQZ} moved in *Figure 17*. t_{CHHL} and t_{CHHH} changed to t_{CLHL} and t_{CLHH}, respectively in *Figure 16*, *Table 18*, *Table 17*, *Table 14*, *Table 19* and *Table 15*. *Plating technology* and *Process* updated in *Table 19: Ordering information scheme*.
20-Mar-2008	8	*Section 2.8: Supply voltage (VCC)* updated. *Section 3: Connecting to the SPI bus* modified. *Section 6.6: Write to Memory Array (WRITE)* modified. Device grade 6 removed in the 4.5 to 5.5 V V_{CC} range (see*Table 8*). *Table 13: DC characteristics (M950x0-R, device grade 6)* modified. *Table 14: AC characteristics (M950x0-W, device grade 6)* modified: frequency changed from 5 MHz to 10 MHz. *Table 15: AC characteristics (M950x0-R, device grade 6)* modified: frequency changed from 2 MHz to 5 MHz. *Section 10: Package mechanical data*: – Inches are calculated from millimeters and rounded to the third decimal digit. – UFDFPN8 package specifications modified. Blank option removed below Plating technology in *Table 19: Ordering information scheme*. Table 25, Table 26 and Table 27 added.
24-Sep-2009	9	*Section 2.8: Supply voltage (VCC)* and *Section 6.4: Write Status Register (WRSR)* updated. *Section 6.6: Write to Memory Array (WRITE)* clarified. I_{OL} and I_{OH} added to *Table 7: Absolute maximum ratings*. V_{RES} added to DC characteristics tables *13*, *12*, *15* and *13*. t_{CLQV} modified in *Figure 15: AC characteristics (M950x0-R, device grade 6)*. Note added to *Table 15: AC characteristics (M950x0-R, device grade 6)*. *Figure 15: Serial input timing*, *Figure 16: Hold timing* and *Figure 17: Serial output timing* updated. Note added below *Figure 20: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, outline*. /W process option removed from *Table 19: Ordering information scheme*. ECOPACK text updated. Small text changes.

Table 20. Document revision history

Date	Version	Changes
02-Feb-2012	10	Document renamed from “M95040 M95020 M95010” to “M950x0 M950x0-W M950x0-R” Silhouette of UDFPN8 (MB or MC) on the cover page updated. *Section 6.3: Read Status Register (RDSR)* updated. Text modified in *Section 6.3.1: WIP bit*. *Table 7: Absolute maximum ratings* updated. *Figure 20: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, outline* modified. *Table 18: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, data* updated. Removed tables of available products from *Section 11: Part numbering*.
24-May-2013	11	Document renamed from “M95040 M95020 M95010” to “M950x0-W M950x0-R”. Silhouette of UDFPN8 (MB or MC) on the cover page updated. *Section 6.3: Read Status Register (RDSR)* updated. Text modified in *Section 6.3.1: WIP bit*. *Table 7: Absolute maximum ratings* updated. Tables 8, 13, 15, 17, 19 removed. *Figure 20: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, outline* modified. *Table 18: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, data* updated. Removed tables of available products from *Section 11: Part numbering*.

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