NTLUS3A39PZ

MOSFET – Power, Single, P-Channel, ESD, UDFN, 1.6x1.6x0.55 mm
-20 V, -5.2 A

ON Semiconductor®

www.onsemi.com

Features

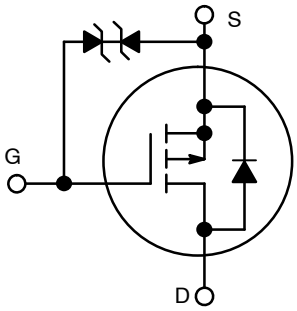
- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile UDFN 1.6 x 1.6 x 0.55 mm for Board Space Saving
- Ultra Low $R_{DS(on)}$
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Optimized for Power Management Applications for Portable Products, Such as Cell Phones, PMP, Media Tablets, DSC, GPS, and Others
- Battery Switch
- High Side Load Switch

MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
−20 V	39 mΩ @ −4.5 V	−5.2 A
	50 mΩ @ −2.5 V	
	81 mΩ @ −1.8 V	
	147 mΩ @ −1.5 V	



P−Channel MOSFET

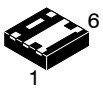
MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	−20	V
Gate-to-Source Voltage			V_{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−5.2	A
		T_A = 85°C		−3.7	
Continuous Drain Current (Note 1)	t ≤ 5 s	T_A = 25°C		−6.4	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.5	W
	t ≤ 5 s	T_A = 25°C		2.3	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−3.4	A
		T_A = 85°C		−2.4	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.6	W
Pulsed Drain Current		tp = 10 μs	I_{DM}	−17	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	°C
Source Current (Body Diode) (Note 2)			I_S	−1	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm^2, 2 oz. Cu.

MARKING DIAGRAM

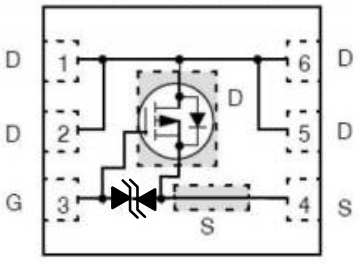


UDFN6
CASE 517AU

AE = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	85	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 3)	$R_{\theta JA}$	55	
Junction-to-Ambient – Steady State min Pad (Note 4)	$R_{\theta JA}$	200	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm^2, 2 oz. Cu.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA	−20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C		13		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −20 V, T_J = 25°C			−1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8.0 V			±10	μA
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA	−0.4		−1.0	V
Negative Threshold Temp. Coefficient	$V_{GS(TH)}/T_J$			3.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −4.0 A		30	39	mΩ
		V_{GS} = −2.5 V, I_D = −2.0 A		40	50	
		V_{GS} = −1.8 V, I_D = −1.2 A		55	81	
		V_{GS} = −1.5 V, I_D = −0.5 A		75	147	
Forward Transconductance	g_{FS}	V_{DS} = −5 V, I_D = −3.0 A		25		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = −15 V		920		pF
Output Capacitance	C_{OSS}			85		
Reverse Transfer Capacitance	C_{RSS}			80		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −15 V; I_D = −3.0 A		10.4		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.5		
Gate-to-Source Charge	Q_{GS}			1.2		
Gate-to-Drain Charge	Q_{GD}			3.0		
SWITCHING CHARACTERISTICS, VGS = 4.5 V (Note 6)						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −15 V, I_D = −3.0 A, R_G = 1 Ω		7.2		ns
Rise Time	t_r			12.2		
Turn-Off Delay Time	$t_{d(OFF)}$			34.7		
Fall Time	t_f			34.8		
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −1.0 A, T_J = 25°C		0.67	1.0	V
		V_{GS} = 0 V, I_S = −1.0 A, T_J = 125°C		0.56		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dis/dt = 100 A/μs, I_S = −1.0 A		11.1		ns
Charge Time	t_a			5.8		
Discharge Time	t_b			5.3		
Reverse Recovery Charge	Q_{RR}			4		nC

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

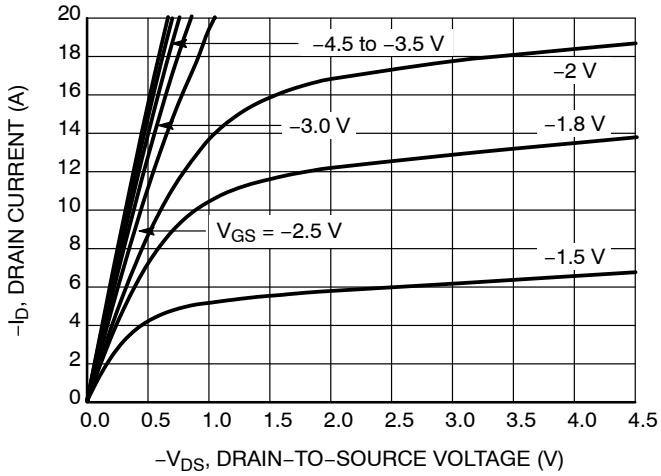


Figure 1. On−Region Characteristics

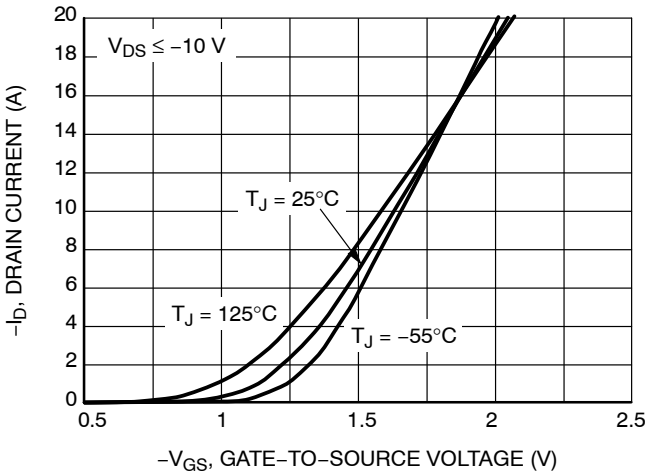


Figure 2. Transfer Characteristics

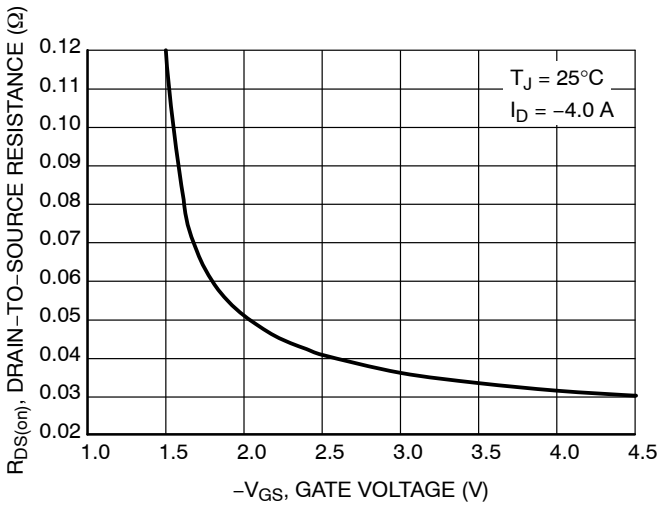


Figure 3. On−Resistance vs. Gate−to−Source Voltage

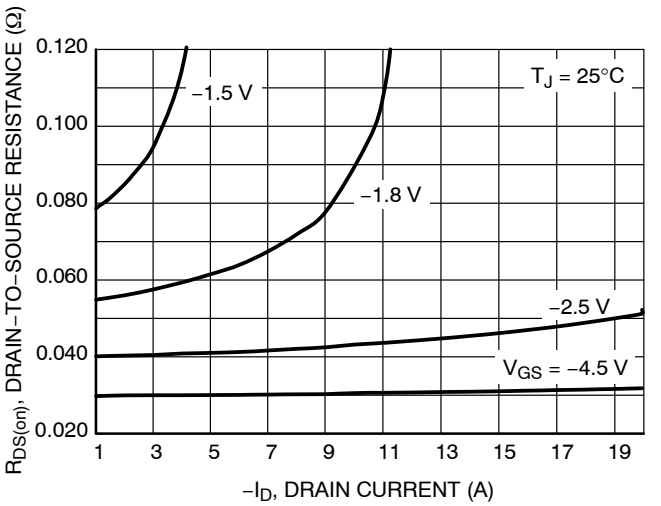


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

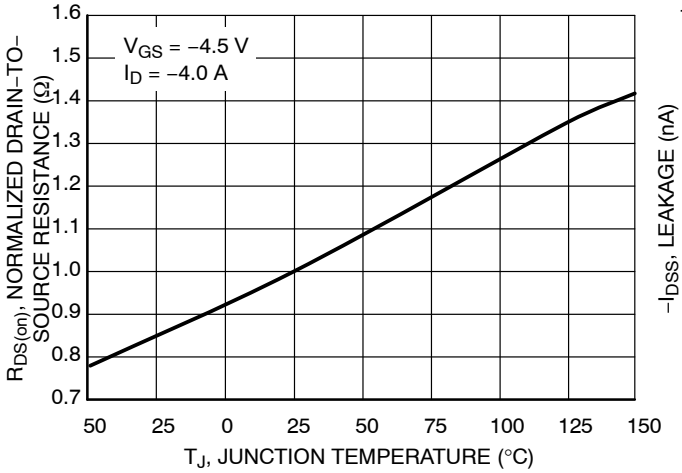


Figure 5. On−Resistance Variation with Temperature

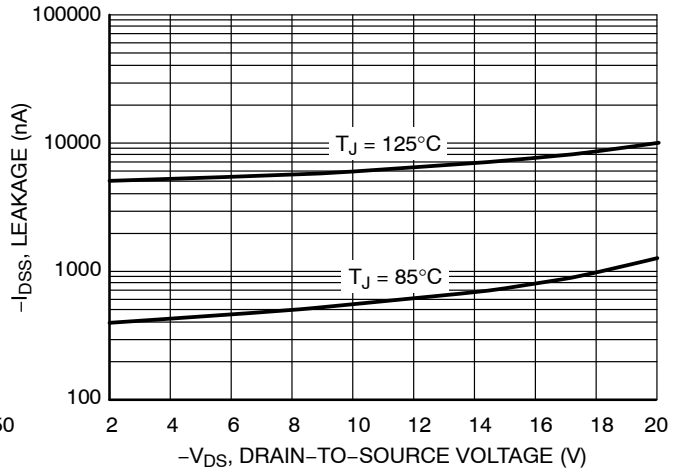


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

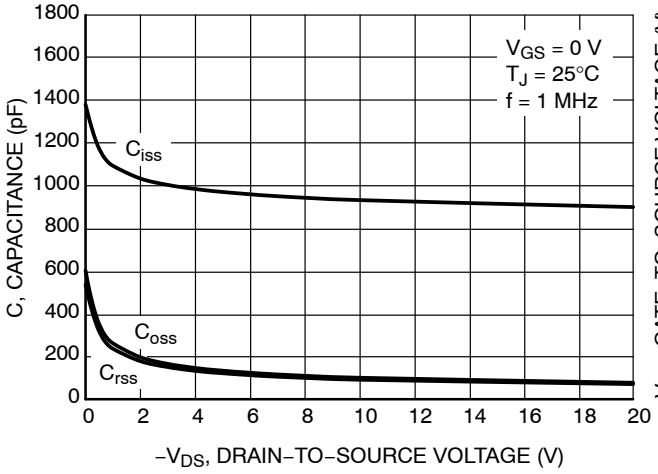


Figure 7. Capacitance Variation

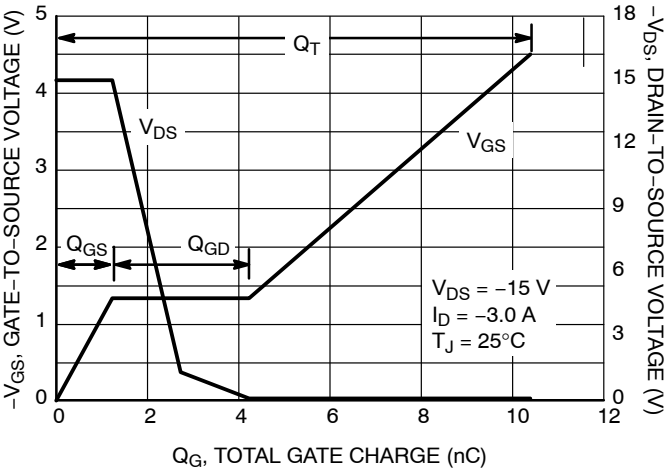


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

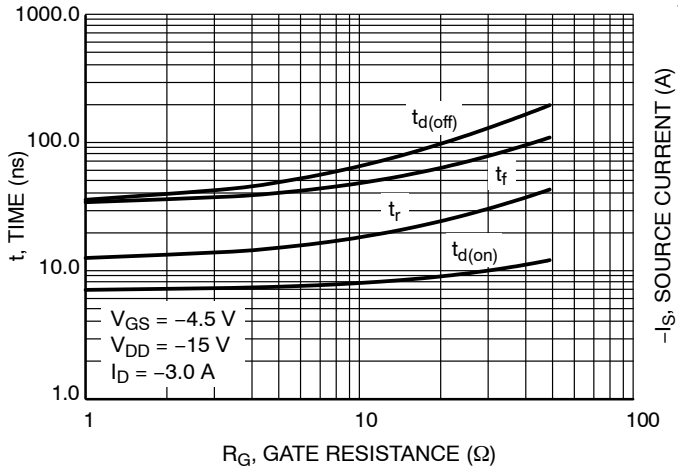


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

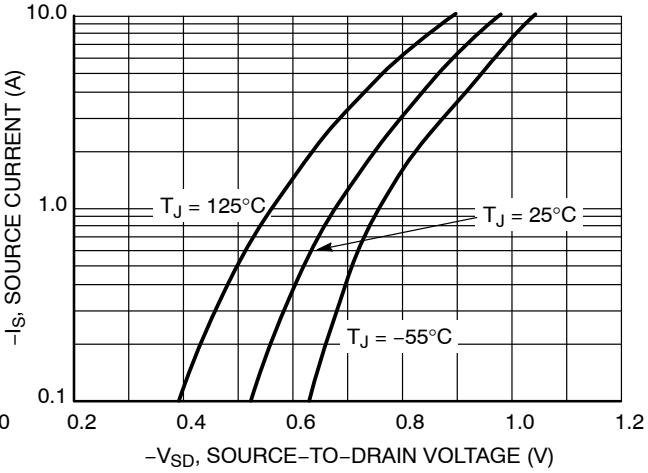


Figure 10. Diode Forward Voltage vs. Current

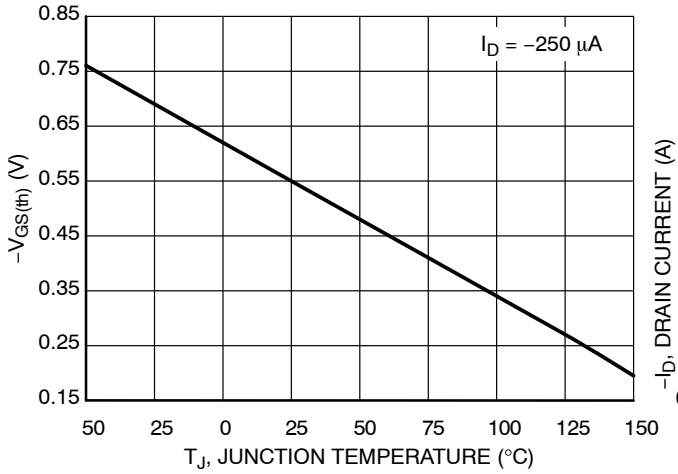


Figure 11. Threshold Voltage

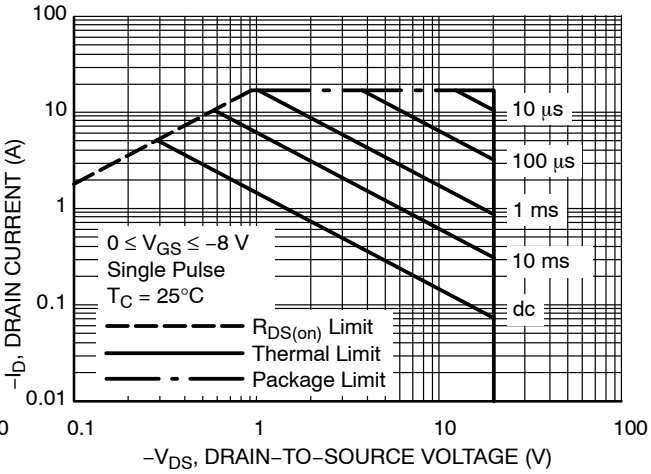


Figure 12. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

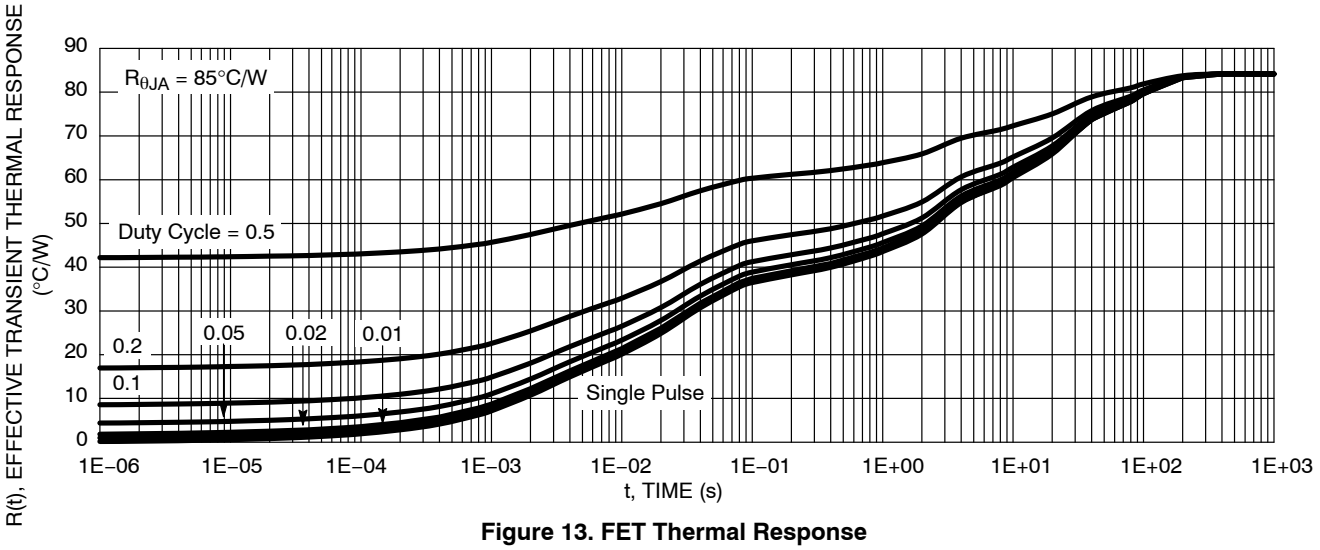


Figure 13. FET Thermal Response

DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NTLUS3A39PZTAG	UDFN6 (Pb−Free)	3000 / Tape & Reel
NTLUS3A39PZTBG	UDFN6 (Pb−Free)	3000 / Tape & Reel

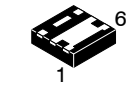
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

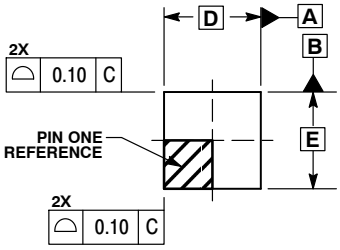
ON Semiconductor®

UDFN6 1.6x1.6, 0.5P
CASE 517AU−01
ISSUE O

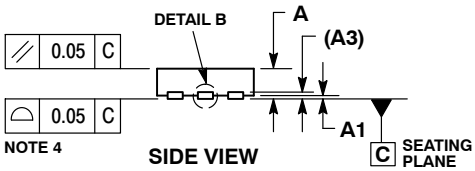
DATE 16 OCT 2008



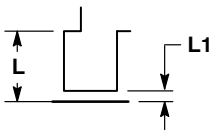
SCALE 4:1



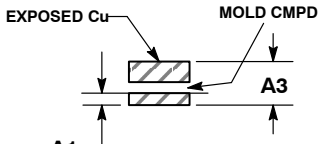
TOP VIEW



SIDE VIEW



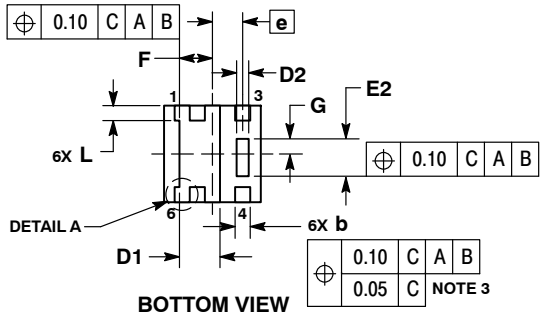
DETAIL A
OPTIONAL CONSTRUCTION



DETAIL B
OPTIONAL CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
D1	0.62	0.72
D2	0.15	0.25
E2	0.57	0.67
F	0.55 BSC	
G	0.25 BSC	
L	0.20	0.30
L1	−−−	0.15



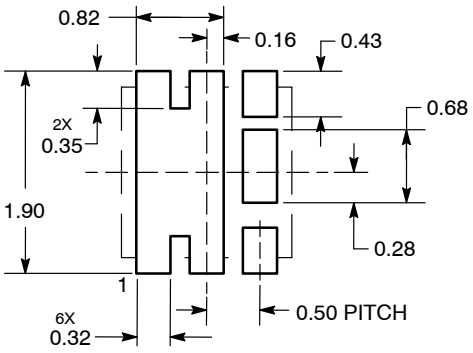
BOTTOM VIEW

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERMASK DEFINED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON35147E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**UDFN6, 1.6X1.6, 0.5P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales