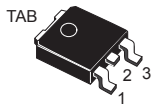
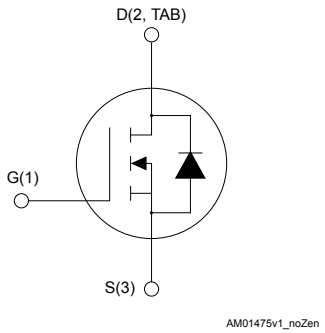
Automotive-grade N-channel 500 V, 730 mΩ typ., 11 A MDmesh II Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD9NM50N	500 V	790 mΩ	5 A

- AEC-Q101 qualified
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

STPOWER

Product status link
STD9NM50N

Product summary	
Order code	STD9NM50N
Marking	9NM50N
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	5	A
	Drain current (continuous) at T_C = 100 °C	3	
I_{DM} (1)	Drain current (pulsed)	20	A
P_{TOT}	Total power dissipation at T_C = 25 °C	45	W
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max)	2	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	140	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 5 A, di/dt ≤ 400 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$, V_{DS} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	2.78	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	50	°C/W

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	500			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 500 V			1	µA
		V_{GS} = 0 V, V_{DS} = 500 V, T_C = 125 °C (1)			100	
I_{GSS}	Gate body leakage current	V_{GS} = ±25 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.5 A		730	790	mΩ

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz,V_{GS} = 0 V	-	364	-	pF
C_{oss}	Output capacitance		-	33	-	pF
C_{rss}	Reverse transfer capacitance		-	1.2	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 50 V	-	147.5	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	5.4	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 5 A, V_{GS} = 0 to 10 V (see Figure 12. Test circuit for gate charge behavior)	-	14	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain charge		-	7	-	nC

1. *$C_{oss\ eq.}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	7	-	ns
t_r	Rise time		-	4.4	-	ns
$t_{d(off)}$	Turn-off delay time		-	25	-	ns
t_f	Fall time		-	8.8	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		20	A
V_{SD} (2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	187		ns
Q_{rr}	Reverse recovery charge		-	1.3		µC
I_{RRM}	Reverse recovery current		-	14		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	224		ns
Q_{rr}	Reverse recovery charge		-	1.5		µC
I_{RRM}	Reverse recovery current		-	13		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

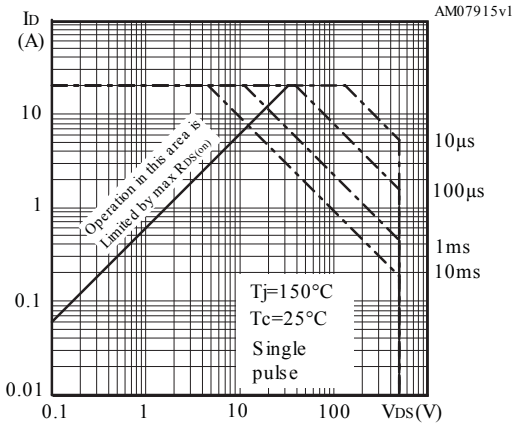


Figure 2. Normalized transient thermal impedance

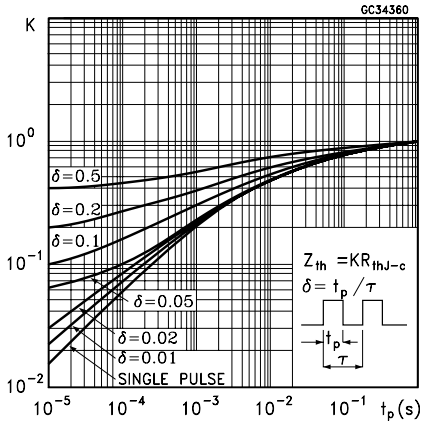


Figure 3. Typical output characteristics

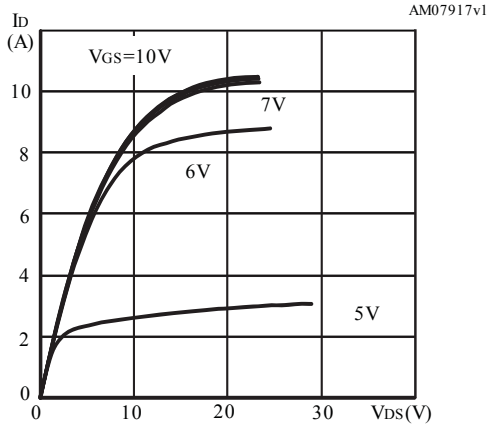


Figure 4. Typical transfer characteristics

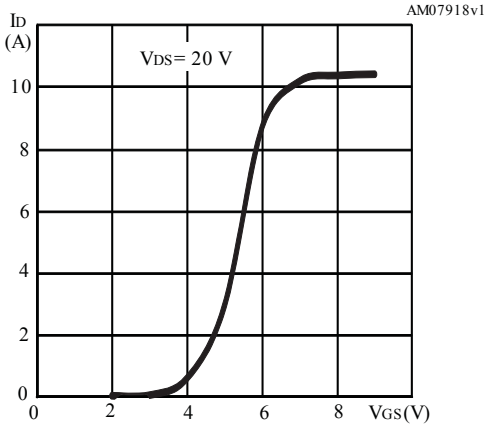


Figure 5. Typical gate charge characteristics

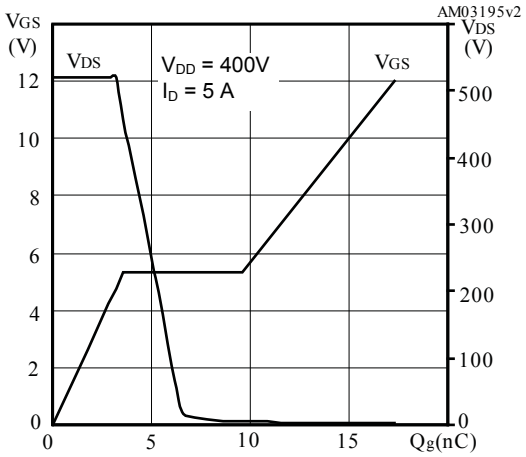


Figure 6. Typical drain-source on-resistance

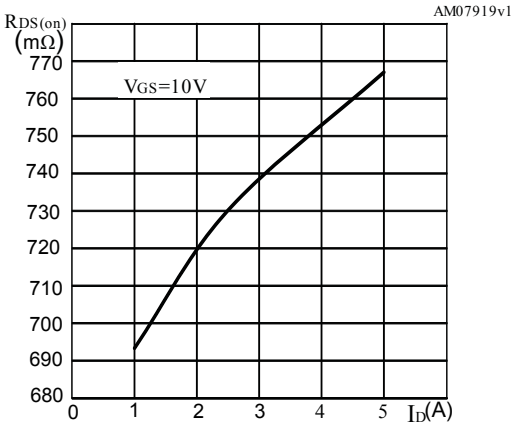


Figure 7. Typical capacitance characteristics

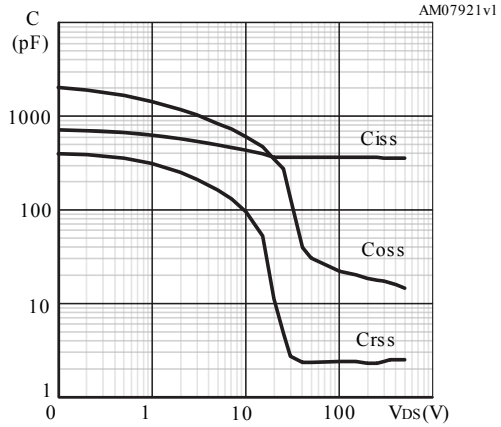


Figure 8. Normalized gate threshold vs temperature

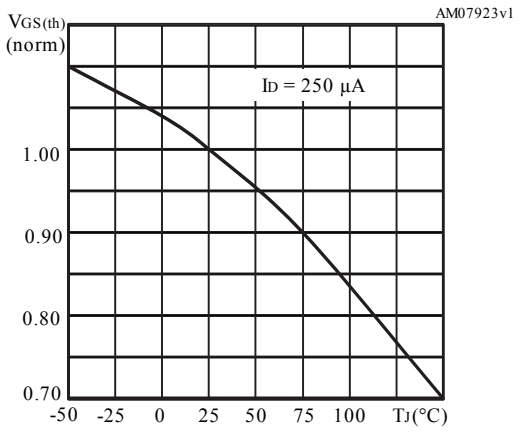


Figure 9. Normalized on-resistance vs temperature

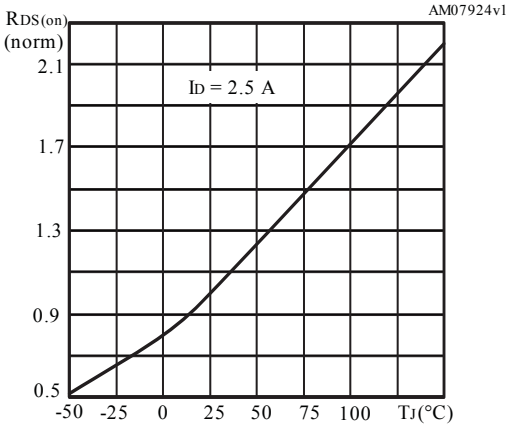
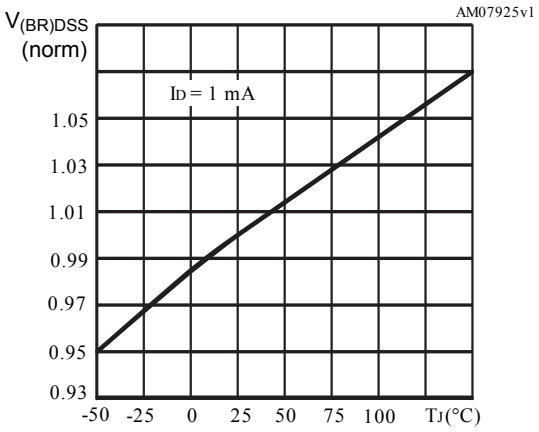


Figure 10. Normalized breakdown voltage vs temperature



3 Test circuits

Figure 11. Test circuit for resistive load switching times

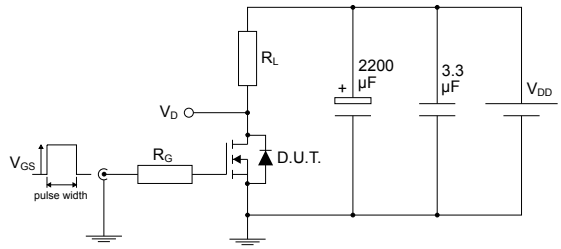


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Figure 12. Test circuit for gate charge behavior

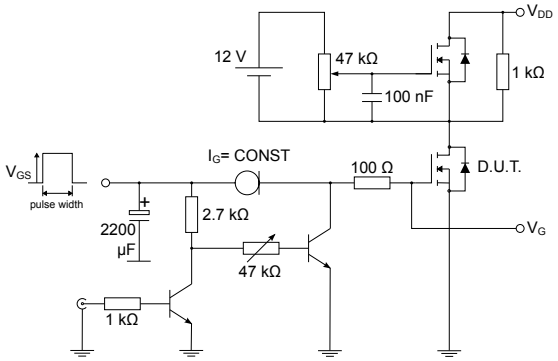

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Figure 13. Test circuit for inductive load switching and diode recovery times

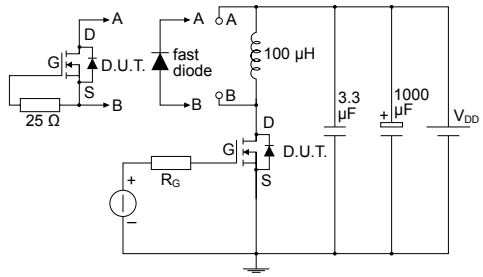

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Figure 14. Unclamped inductive load test circuit

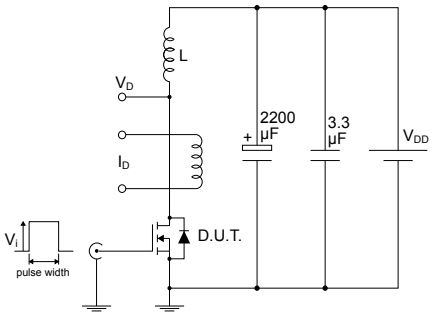

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Figure 15. Unclamped inductive waveform

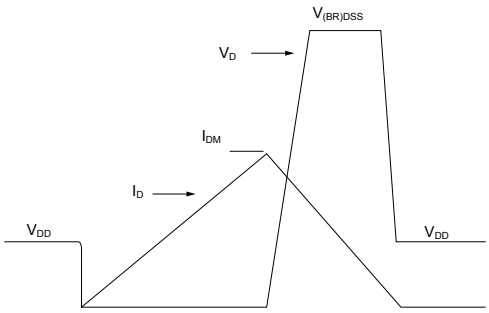

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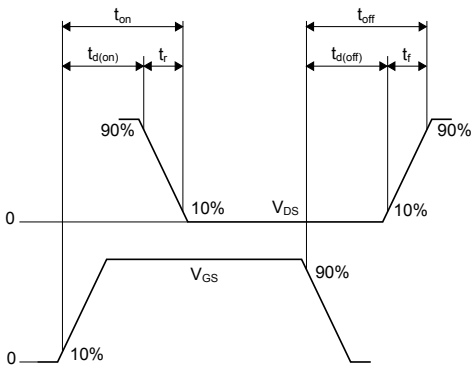
Figure 16. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 17. DPAK (TO-252) type A2 package outline

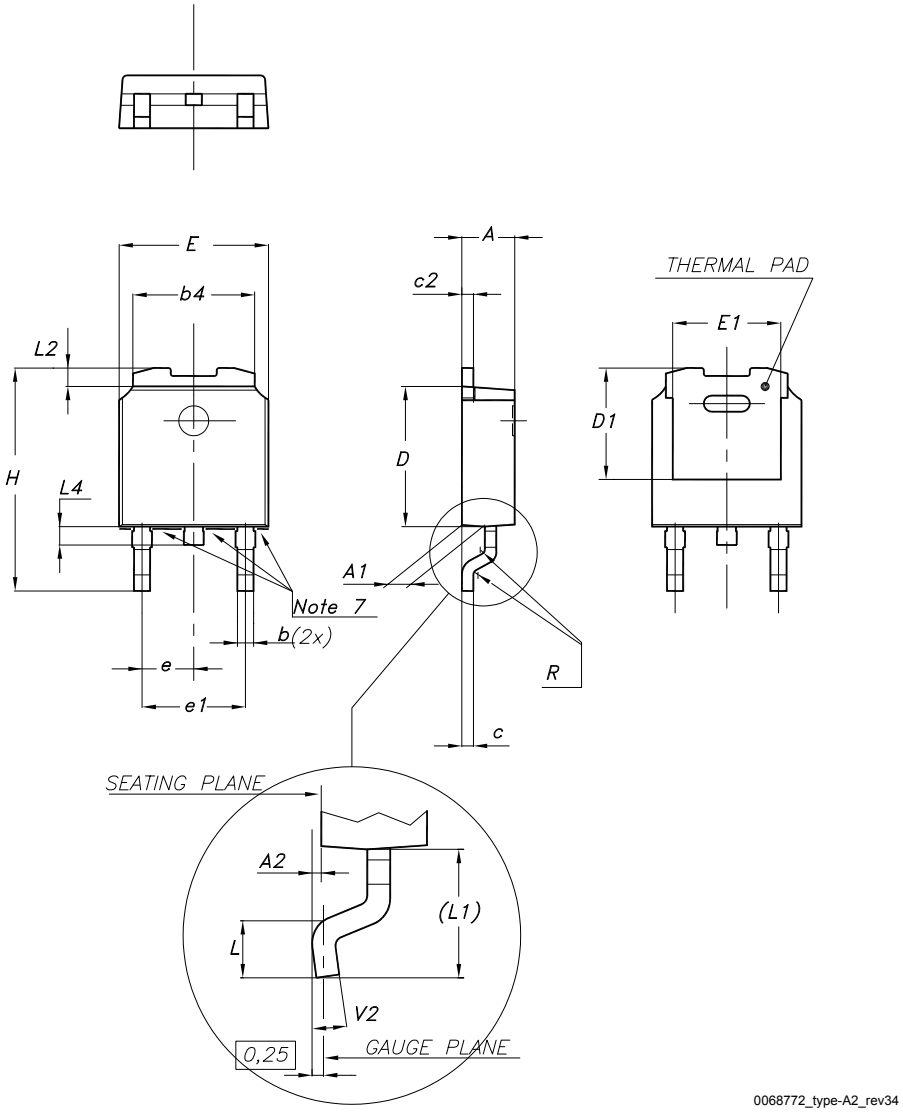
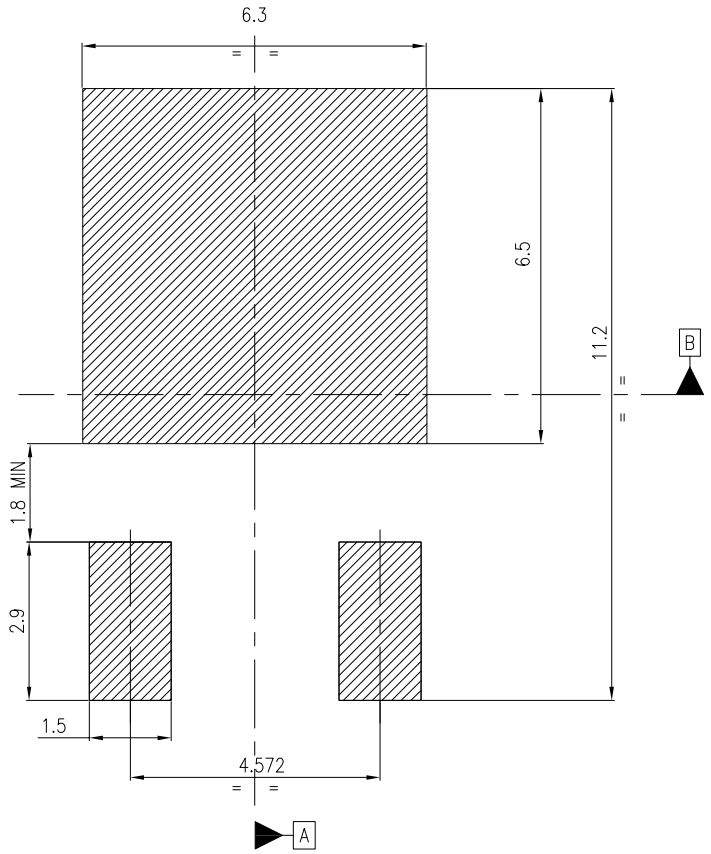


Table 7. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 18. DPAK (TO-252) recommended footprint (dimensions are in mm)



Notes:

1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664–1)

2) The device must be positioned within ⌖ 0.05 A B

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4.2 DPAK (TO-252) packing information

Figure 19. **DPAK (TO-252) tape outline**

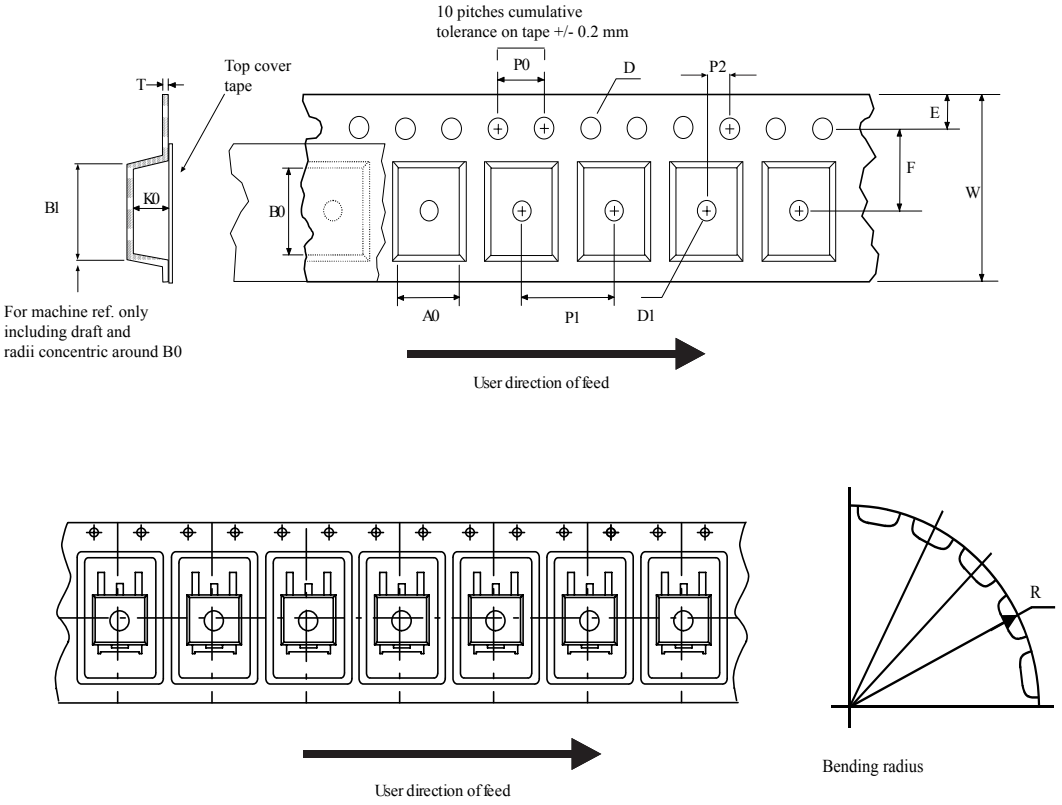

Figure 20. **DPAK (TO-252) reel outline**

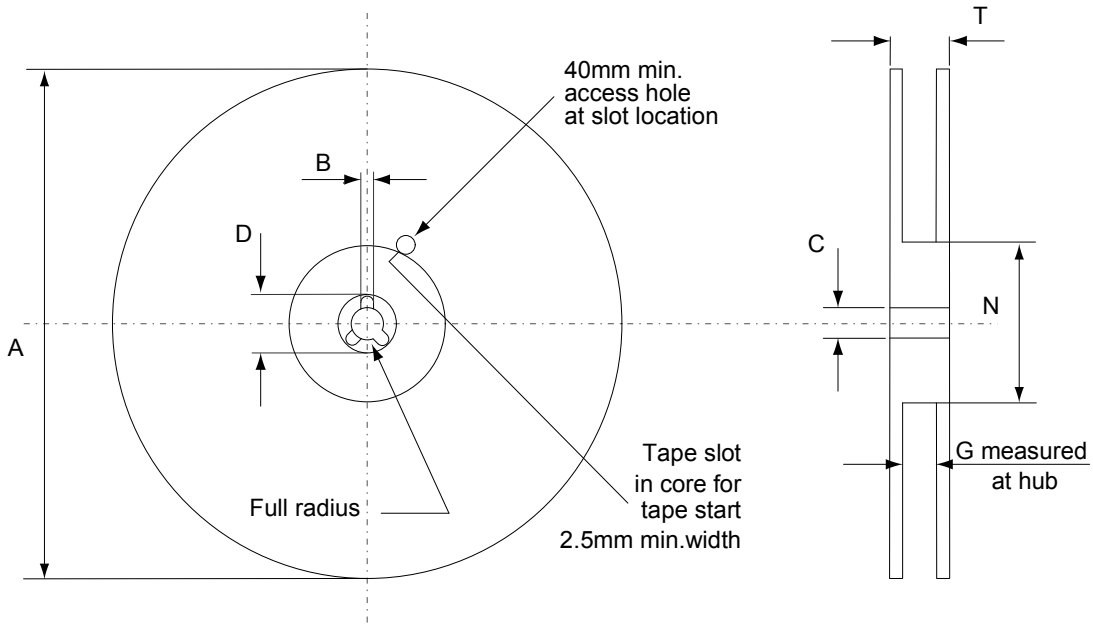

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Table 8. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 9. **Document revision history**

Date	Version	Changes
21-Sep-2011	1	First release.
08-May-2023	2	Updated Section 4.1 DPAK (TO-252) type A2 package information. Minor text changes.

Contents