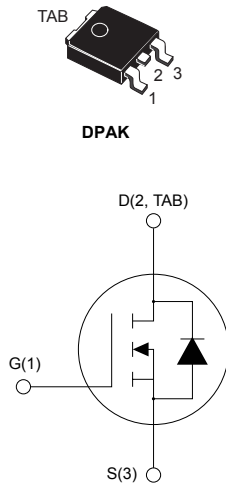


Automotive-grade N-channel 500 V, 730 mΩ typ., 11 A MDmesh II Power MOSFET in a DPAK package




AM01475v1_noZen



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD9NM50N	500 V	790 mΩ	5 A

- AEC-Q101 qualified 
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Product status link

[STD9NM50N](#)

Product summary

Order code	STD9NM50N
Marking	9NM50N
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±25	V
I _D	Drain current (continuous) at T _C = 25 °C	5	A
	Drain current (continuous) at T _C = 100 °C	3	
I _{DM} ⁽¹⁾	Drain current (pulsed)	20	A
P _{TOT}	Total power dissipation at T _C = 25 °C	45	W
I _{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _J max)	2	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	140	mJ
dv/dt ⁽²⁾	Peak diode recovery voltage slope	15	V/ns
T _{stg}	Storage temperature range	-55 to 150	°C
T _J	Operating junction temperature range		°C

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 5 \text{ A}$, $di/dt \leq 400 \text{ A}/\mu\text{s}$, $V_{DS} (\text{peak}) \leq V_{(BR)DSS}$, $V_{DS} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJC}	Thermal resistance, junction-to-case	2.78	°C/W
R _{thJA} ⁽¹⁾	Thermal resistance, junction-to-ambient	50	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	500			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			100	
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 25\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$		730	790	m Ω

1. Specified by design, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	364	-	pF
C_{oss}	Output capacitance		-	33	-	pF
C_{riss}	Reverse transfer capacitance		-	1.2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }50\text{ V}$	-	147.5	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	5.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 12. Test circuit for gate charge behavior)	-	14	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain charge		-	7	-	nC

1. $C_{oss\text{ eq.}}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	7	-	ns
t_r	Rise time		-	4.4	-	ns
$t_{d(off)}$	Turn-off delay time		-	25	-	ns
t_f	Fall time		-	8.8	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5\text{ A}, V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V}$	-	187		ns
Q_{rr}	Reverse recovery charge	(see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	1.3		μC
I_{RRM}	Reverse recovery current		-	14		A
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V},$	-	224		ns
Q_{rr}	Reverse recovery charge	$T_J = 150\text{ }^\circ\text{C}$ (see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	1.5		μC
I_{RRM}	Reverse recovery current		-	13		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

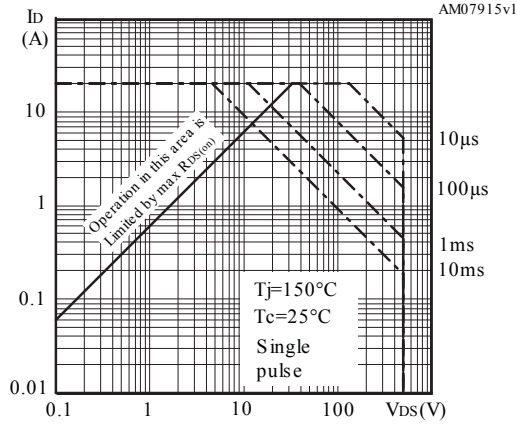


Figure 2. Normalized transient thermal impedance

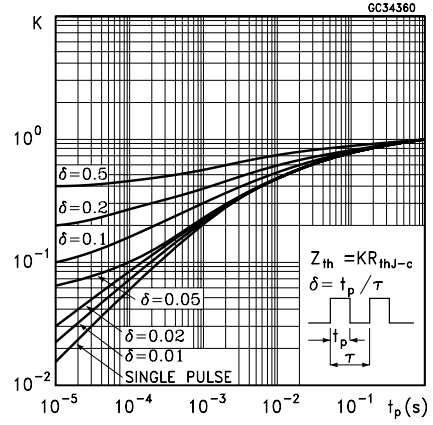


Figure 3. Typical output characteristics

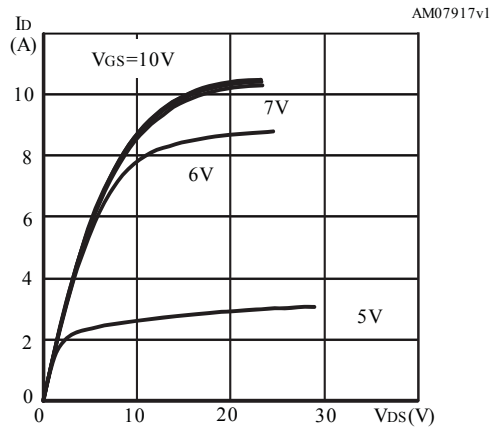


Figure 4. Typical transfer characteristics

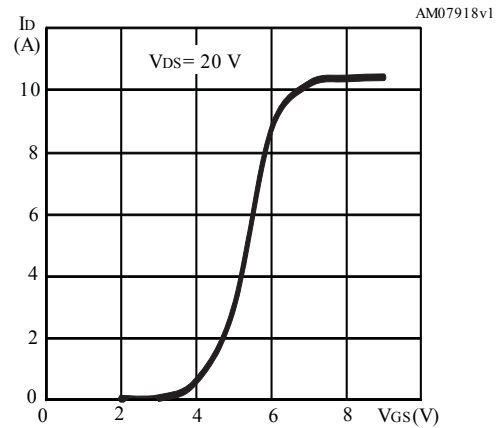


Figure 5. Typical gate charge characteristics

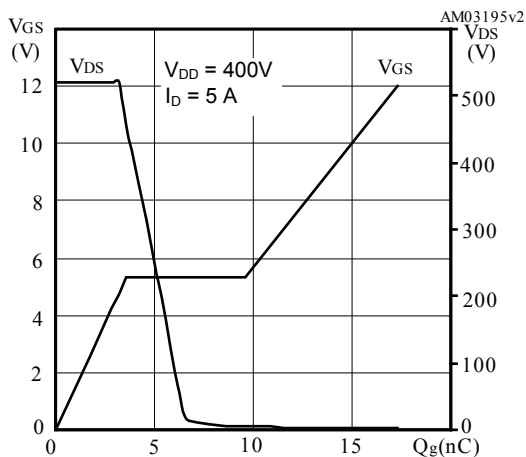


Figure 6. Typical drain-source on-resistance

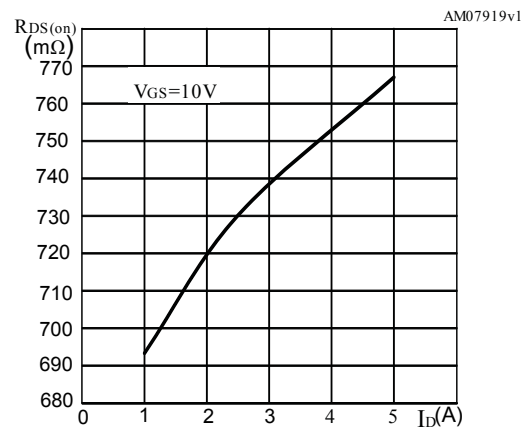


Figure 7. Typical capacitance characteristics

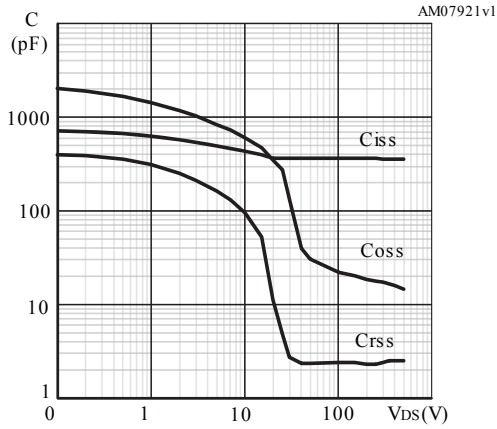


Figure 8. Normalized gate threshold vs temperature

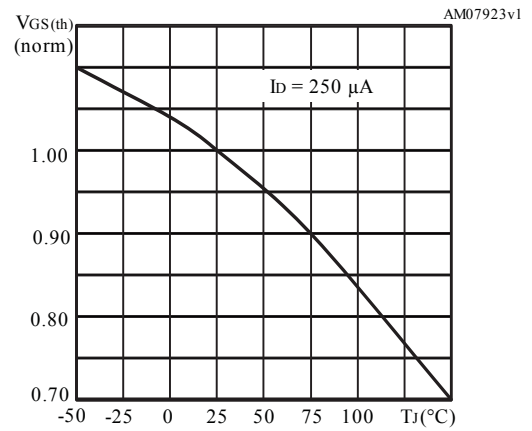


Figure 9. Normalized on-resistance vs temperature

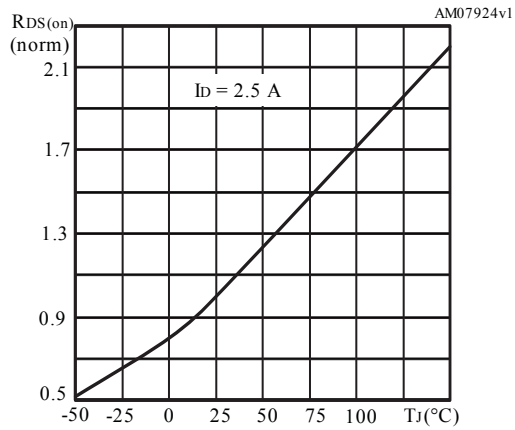
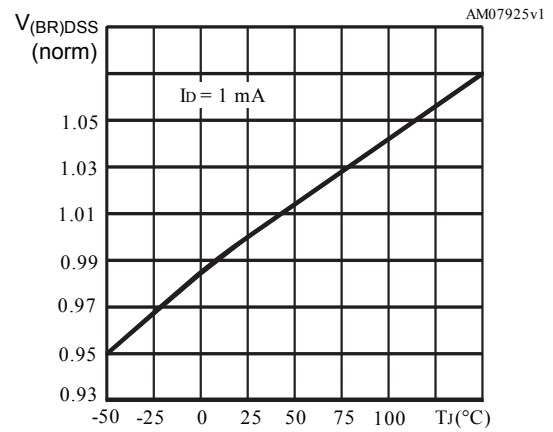
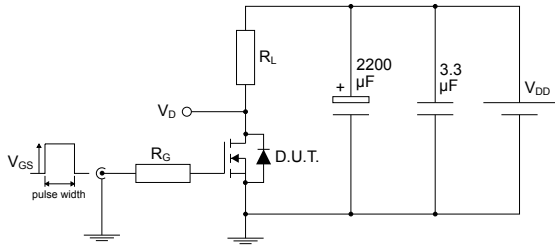


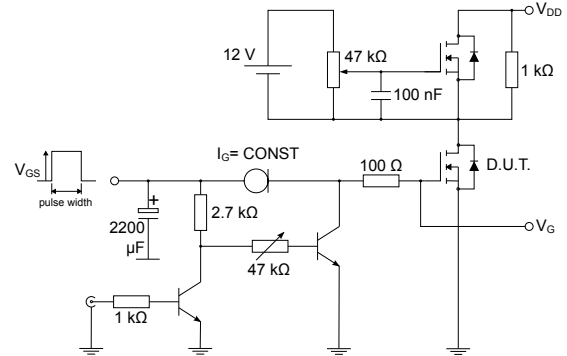
Figure 10. Normalized breakdown voltage vs temperature



3 Test circuits

Figure 11. Test circuit for resistive load switching times


AM01468v1

Figure 12. Test circuit for gate charge behavior


AM01469v1

Figure 13. Test circuit for inductive load switching and diode recovery times


AM01470v1

Figure 14. Unclamped inductive load test circuit


AM01471v1

Figure 15. Unclamped inductive waveform


AM01472v1

Figure 16. Switching time waveform

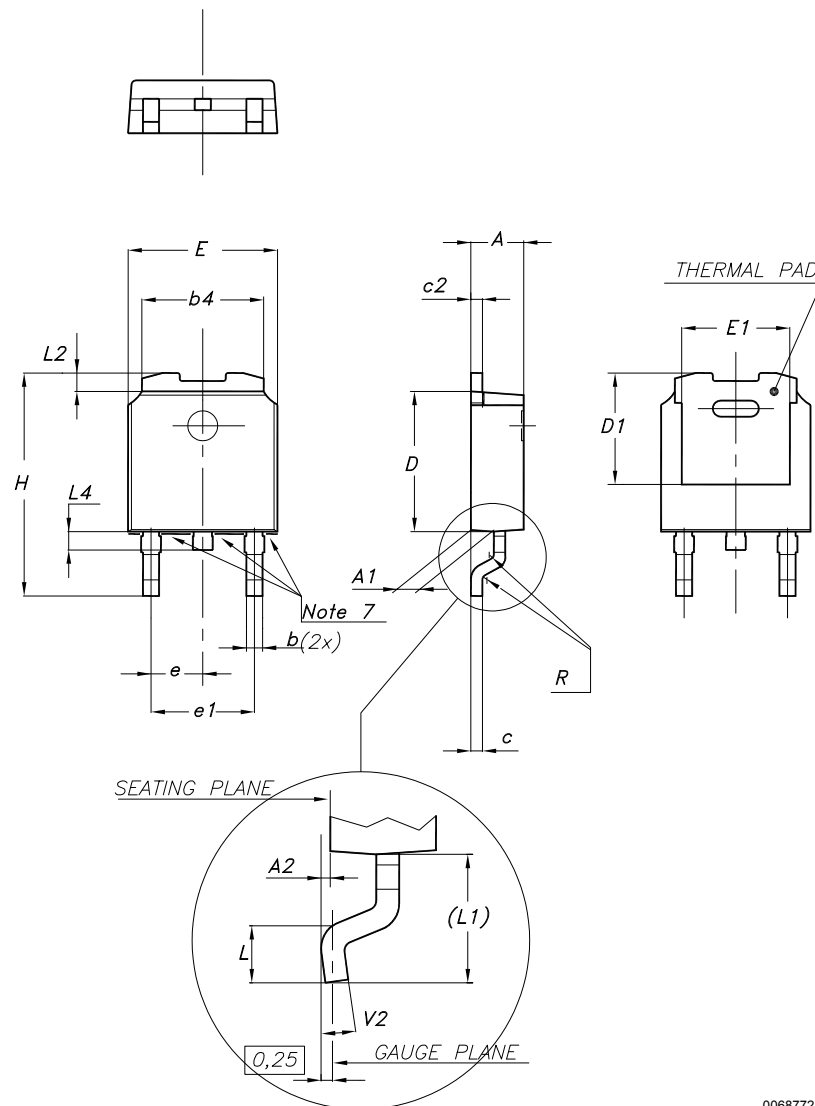

AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 17. DPAK (TO-252) type A2 package outline

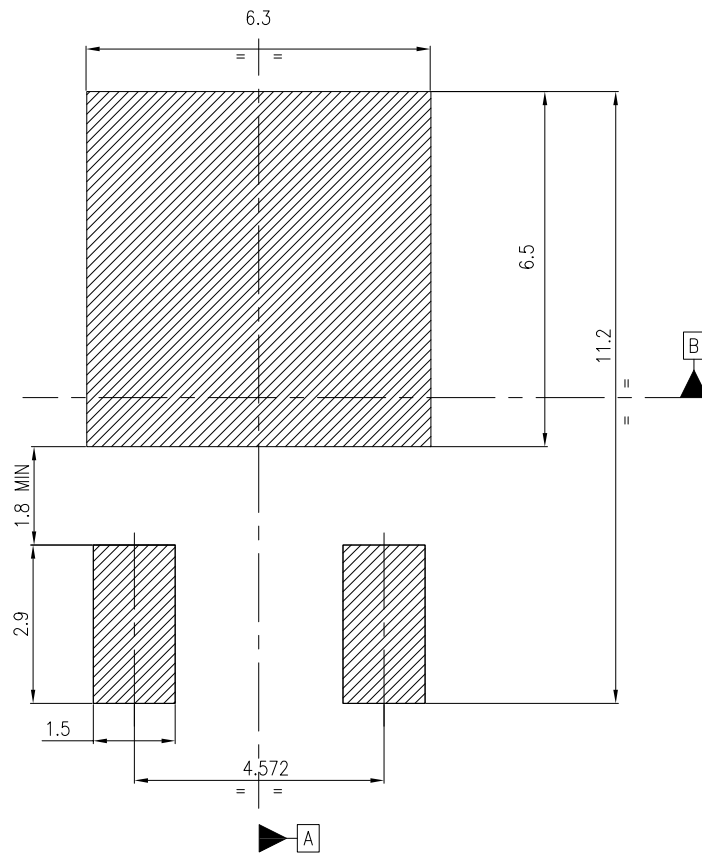


0068772_type-A2_rev34

Table 7. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 18. DPAK (TO-252) recommended footprint (dimensions are in mm)



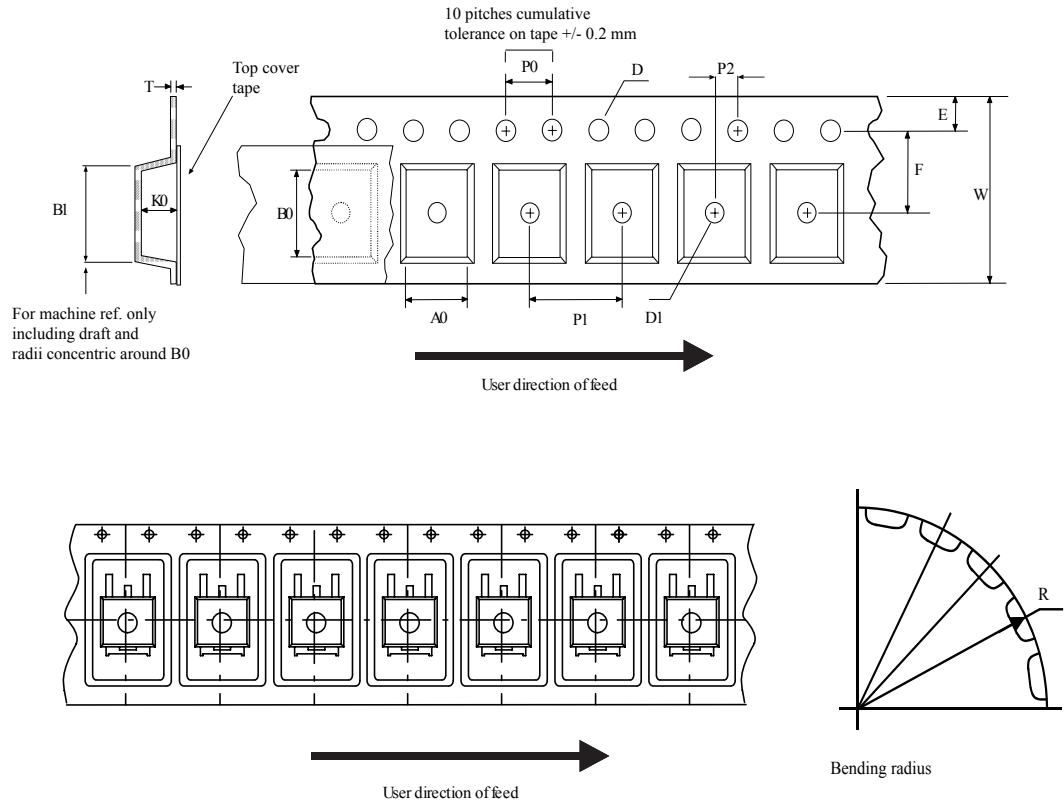
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within $\boxed{\oplus 0.05 \text{ A B}}$

FP_0068772_34

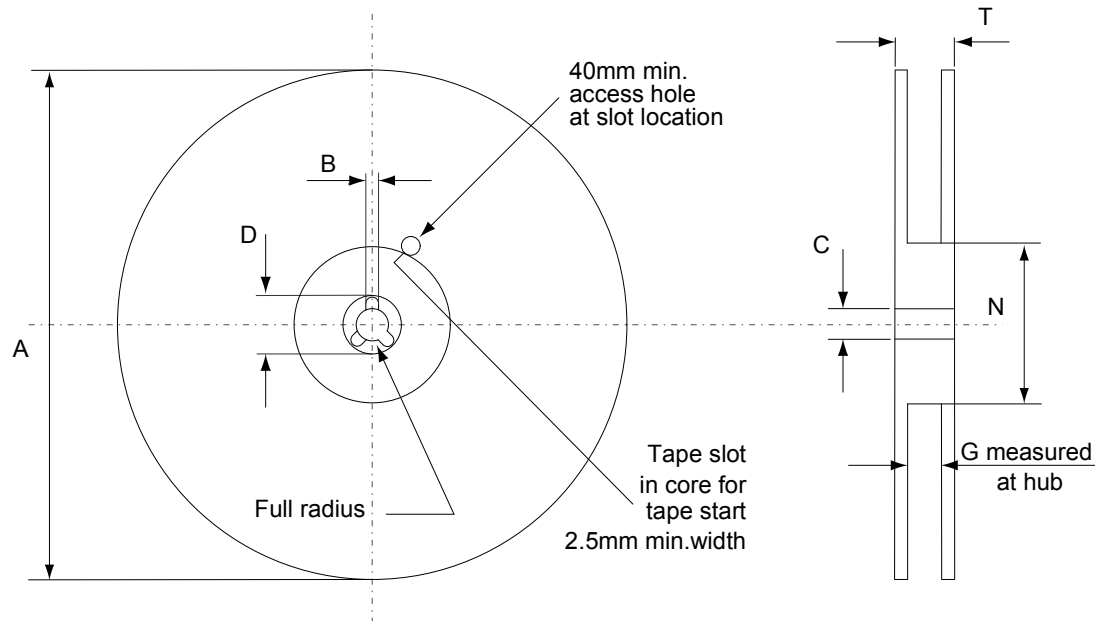
4.2 DPAK (TO-252) packing information

Figure 19. DPAK (TO-252) tape outline



AM08852v1

Figure 20. DPAK (TO-252) reel outline



AM06038v1

Table 8. DPAK (TO-252) tape and reel mechanical data

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 9. Document revision history

Date	Version	Changes
21-Sep-2011	1	First release.
08-May-2023	2	Updated Section 4.1 DPAK (TO-252) type A2 package information. Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	DPAK (TO-252) type A2 package information	8
4.2	DPAK (TO-252) packing information	11
	Revision history	13

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved