PCN Number:		20180425000.2				Ρ	CN Date:	Ap	ril 30 2018	
Title:	Title: Qualification of a new Bump Site plus addition of Polyimide for select devices						vices			
Custon	ner Contact:	PCN M	anager	Dept:	Quality Ser					
Proposed 1 st Ship Date		te:	Cct 30 2018		timated San ailability:	nple	ple		Provided upon Request	
Change										
	embly Site		Assembly			\boxtimes				
	sign		Electrical				Mechanical Specification			
	st Site		Packing/S				Test Process			
	fer Bump Site		Wafer Bur			<u> </u>	Wafer Bun			
Wa	fer Fab Site		Wafer Fab				Wafer Fab Process			
			Part numb							
				PCN D	etails					
Descrip	otion of Chang	e:								
	Texas Instruments is pleased to announce the qualification of a new bump site as well as the introduction of Polyimide: Current New									
Wafer Bump Sit		_	HBUMP							
V	Vafer Bump Si	ite		HBUM					>	
	Vafer Bump S Die Coating	ite		HBUM None	IP			UMI		
	Die Coating	ite			IP		DB	UMI		
Reasor	Die Coating				IP		DB	UMI		
Reason HBUMP	Die Coating for Change: facility has clos	ed	Form, Func	None	IP 2	abi	DB Poly	UMI imi	de	
Reason HBUMP	Die Coating	ed	Form, Func	None	IP 2	abi	DB Poly	UMI imi	de	
Reason HBUMP Anticip None	Die Coating for Change: facility has clos	ed n Fit,		None	IP 2	abi	DB Poly	UMI imi	de	
Reason HBUMP Anticip None Anticip	for Change: facility has clos ated impact o	ed n Fit, n Mat	erial Declar Material I productio release.	None tion, Qu ration Declaration Declaration Upon pro	IP	t Co ilat se	DB Poly	ve /	de ' negative): re driven from production	
Reason HBUMP Anticip None Anticip	Pie Coating for Change: facility has clos ated impact o ated impact o Impact to the	ed n Fit, n Mat	erial Declar Material I productio release. obtained	None tion, Qu ration Declaration Declaration n data an Upon pro from the	IP a ality or Reli ons or Produc nd will be ava oduction relea <u>TI ECO webs</u>	t Co ilat se i <u>ite</u> .	DB Poly	ve /	de ' negative): re driven from production	
Reason HBUMP Anticip None Anticip	Pie Coating for Change: facility has clos ated impact o ated impact o Impact to the cerial Declaratio es to product i	ed n Fit, n Mat	erial Declar Material I productio release. obtained	None tion, Qu ration Declaration Declaration n data an Upon pro from the	IP a ality or Reli ons or Produc nd will be ava oduction relea <u>TI ECO webs</u>	t Co ilat se i <u>ite</u> .	DB Poly	ve /	de ' negative): re driven from production	

Product Affected							
TPS650001TRTERQ1	TPS650002TRTERQ1	TPS65000TRTERQ1					



Automotive New Product Qualification Summary

(As per AEC-Q100 and JEDEC Guidelines)

TPS65000TRTERQ1 Bump site offload from HBUMP to DBUMP Approved 19-Apr-2018

Product Attributes

Product Attributes							
Attributes	Qual Device: TPS65000TRTERQ1	QBS Product and Package References: <u>TPS57114QRTERDN</u>	QBS Process Reference: <u>TPS55340QPWPRQ1</u>	QBS Package Reference: <u>DS90UB921</u>			
Operating Temp Range	-40 to +105 C	-40 to +125 C	-40 to +125 C	105 C			
Automotive Grade Level	Grade 2	Grade 1	Grade 1	- Signal Chain MFAB			
Product Function	Power Management	Power Management	Power Management				
Wafer Fab Supplier	MIHO	MIHO	MIHO				
Die Revision	C (PG1.2)	A3	PG2.0	A			
Assembly Site	TIM	TIM	TITL	TIEM			
Package Type	QFN	QFN	HTSSOP	QFN			
Package Designator	RTE	RTE	PWP	RHS			
Ball/Lead Count	16	16	14	48			

- QBS: Qual By Similarity

- Qual Device TPS65000TRTERQ1 is qualified at LEVEL2-260CG

Qualification Results Data Displayed as: N T-4-1 onlo sizo / Total failed

	Data Displayed as: Number of lots / Total sample size / Total failed										
	Туре	#	Test Spec	Min Lot Qty	SS/ Lot	Test Name / Condition	Duration	Qual Device: TP \$65000TRTERQ1	QBS Product and Package References: <u>TPS57114QRTERDN</u>	QBS Process Reference: <u>TP S55340QPWPRQ1</u>	QBS Package Reference: <u>DS90UB921</u>
Tes	t Group /	A – Ac	celerated Environment Stress	s Tests							
	PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Automotive Preconditioning	Level 2-260C	All pass	-	All pass	All pass
	PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Automotive Preconditioning	Level 3-260C	-	All pass	-	-
	HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 130C/85%RH	96 Hours	-	3/231/0	3/231/0	1/81/0
	AC	A3	JEDEC JESD22-A102	3	77	Autoclave 121C	96 Hours	1/77/0	3/231/0	3/231/0	1/77/0
	тс	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles	1/77/0	3/231/0	3/231/0	1/77/0
	TC-BP	A4	MIL-STD883 Method 2011	1	60	Post Temp. Cycle Bond Pull	per MIL-STD 883 Method 2011	1/5/0	3/15/0	3/15/0	1/5/0
	PTC	A5	JEDEC JESD22-A105	1	45	Power Temperature Cycle, -40/125C	1000 Cycles	-	1/45/0	1/45/0	-
	HTSL	A6	JEDEC JESD22-A103	1	45	High Temp. Storage Bake 175C	500 Hours	1/45/0	1/45/0	-	-
	HTSL	A6	JEDEC JESD22-A103	1	45	High Temp. Storage Bake, 150C	1000 Hours	-	-	1/50/0	1/45/0
Tes	t Group E	B – Ac	celerated Lifetime Simulation	Tests							
	HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 125C	1000 Hours	-	3/231/0	3/231/0	1/77/0
	ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate, 125C	48 Hours	-	-	3/2400/0	-
\vdash						NVM Endurance, Data Retention,					
	EDR	B3	AEC Q100-005	3	77	and Operational Life	-	N/A	-	-	-
Tes	t Group (C – Pa	ckage Assembly Integrity Tes	ts							
	WBS	C1	AEC Q100-001	1	30	Bond Shear (Cpk>1.67)	Wires	1/30/0			
\vdash	WBP	C2	MIL-STD883 Method 2011	1	30	Bond Pull (Cpk>1.67)	Wires	1/30/0		-	-
	SD	СЗ	JEDEC JESD22-B102	1	15	Surface Mount Solderability >95% Lead Coverage, steam aging	-	-	-	-	1/15/0
	PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions (Cpk>1.67)	-	3/30/0	-	-	-
	SBS	C5	AEC Q100-010	3	50	Solder Ball Shear (Cpk>1.67)	Post HTSL/Bump	-			-
	LI	C6	JEDEC JESD22-B105	1	50	Lead Integrity	Leads	-	-	-	-
Tes	t Group I	D – Die	Fabrication Reliability Tests								
			·					Completed Per			
	EM	D1	JESD61	-	-	Electromigration	-	Process Technology Requirements	-	-	-
	TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	Completed Per Process Technology Requirements	-	-	-
	HCI	D3	JESD60 & 28	-	-	Hot Injection Carrier	-	Completed Per Process Technology Requirements	-	-	-
	NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	Completed Per Process Technology Requirements	-	-	-
	SM	D5	-	-	-	Stress Migration	-	Completed Per Process Technology Requirements	-	-	-
Te	st Group	E – El	ectrical Verification Tests								
	HBM	E2	AEC Q100-002	1	3	ESD - HBM	2000 V	1/3/0	1/3/0	-	-
\vdash	CDM	E3	AEC Q100-011	1	3	ESD - CDM	1000 V	1/3/0	1/3/0	-	1/3/0
\vdash	LU	E4	AEC Q100-004	1	6	Latch-up	T max	1/6/0	1/6/0	1/6/0	2/12/0
	ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, Hot, & Cold	3/90/0	3/90/0	3/90/0	-

 ED
 ED
 AEC CITUE-UU9
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 Electronal Distributions

 A1 (PC): Preconditioning:
 Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.
 Ambient Operating Temperature by Automotive Grade Level:
 Grade 0 (or E):
 Or Constraints
 Grade 1 (or Q):
 40°C to +125°C
 Grade 2 (or T):
 40°C to +125°C
 Grade 2 (or T):
 40°C to +105°C
 Grade 3 (or E):
 40°C to +105°C
 60°C
 40°C to +105°C
 40°C to +105°C
 40°C to +105°C
 40°C to +105°C
 40°C to +10°C to +10°C

Green/Pb-free Status: Qualified Pb-Free(SMT) and Green

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com