19-3154; Rev 1; 5/05

EVALUATION KIT AVAILABLE

Low-Cost, Current-Mode PWM Buck Controller with Foldback Current Limit

MAX1954A

General Description

The MAX1954A synchronous current-mode, pulse-width modulation (PWM) buck controller is pin compatible with the popular MAX1954 and is suitable for applications where cost and size are critical.

The MAX1954A operates from an input voltage range of 3.0V to 13.2V, independent of the IC supply. The output voltage is adjustable down to 0.8V. The IC operates at a fixed 300kHz switching frequency and provides up to 25A of output current with efficiency up to 95%. This controller has excellent transient response resulting in smaller output capacitance.

The MAX1954A features foldback current limiting that greatly reduces input current and component power dissipation during output overload or short-circuit conditions.

The compensation and shutdown control (COMP) input, in addition to providing compensation to the error amplifier, can be pulled low to shut down the converter. An input undervoltage lockout is provided to ensure proper operation during power sags to prevent the external power MOSFETs from overheating. Internal digital soft-start is included to reduce inrush current and save an external capacitor.

The MAX1954A is available in a tiny 10-pin µMAX® package to minimize PC board space.

Applications

Printers and Scanners

Graphic Cards and Video Cards

PCs and Servers

Microprocessor Cores

Low-Voltage Distributed Power

Telecom/Networks

µMAX is a registered trademark of Maxim Integrated Products, Inc.

Features

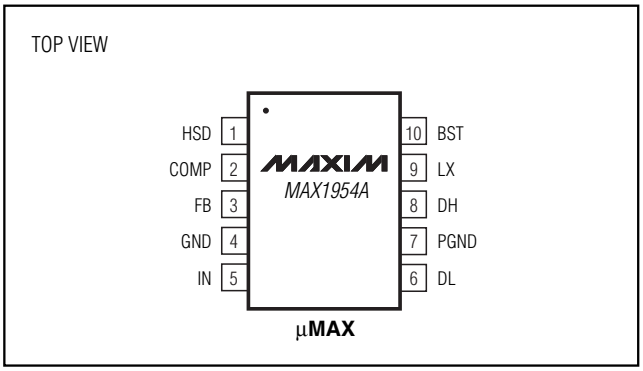
- **Current-Mode Controller**
- **Fixed-Frequency PWM**
- **Foldback Current Limit**
- **Output Down to 0.8V with ±1% FB Accuracy**
- **3.0V to 13.2V Input Voltage**
- **300kHz Switching Frequency**
- **25A Output-Current Capability**
- **93% Efficiency**
- **All-N-Channel-MOSFET Design for Low Cost**
- **No Current-Sense Resistor Needed**
- **Internal Digital Soft-Start**
- **Small 10-Pin µMAX Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1954AEUB	-40°C to +85°C	10 µMAX
MAX1954AEUB+	-40°C to +85°C	10 µMAX

+Denotes lead-free package.

Pin Configuration



Low-Cost, Current-Mode PWM Buck Controller with Foldback Current Limit

ABSOLUTE MAXIMUM RATINGS

IN, FB to GND .....-0.3V to +6V
LX to BST .....-6V to +0.3V
BST to GND .....-0.3V to +20V
DH to LX ..... -0.3V to (V_{BST} + 0.3V)
DL, COMP to GND .....-0.3V to (V_{IN} + 0.3V)
HSD to GND .....-0.3V to 14V
PGND to GND .....-0.3V to +0.3V

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....+65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V, V_{BST} - V_{LX} = 5V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
Operating Input Voltage Range			3.0		5.5	V
HSD Voltage Range	(Note 1)		3.0		13.2	V
Quiescent Supply Current	V_{FB} = 1.5V			1	2	mA
Standby Supply Current	V_{IN} = V_{BST} = 5.5V, V_{HSD} = 13.2V, LX = unconnected, COMP = GND				2	mA
Undervoltage-Lockout Trip Level	Falling V_{IN}, 50mV (typ) hysteresis		2.5	2.7	2.9	V
DC-DC CONTROLLER						
Output-Voltage Adjust Range (V_{OUT})	Maximum output voltage depends on external components and maximum duty cycle		0.8			V
ERROR AMPLIFIER						
FB Regulation Voltage			-1.0	+0.8	+1.0	%
Transconductance			70	110	160	µS
Voltage Gain				200		V/V
FB Input Leakage Current	V_{FB} = 0.9V			50	500	NA
FB Input Common-Mode Range			-0.1		+1.5	V
COMP Output-Voltage Swing			0.80		2.36	V
Current-Sense Amplifier Voltage Gain			3.15	3.5	3.85	V/V
Current-Limit Threshold	V_{PGND} - V_{LX}	V_{FB} = 0.8V	110	135	145	mV
		V_{FB} = 0V	21	36	51	
OSCILLATOR						
Switching Frequency	MAX1954A		240	300	360	kHz
Maximum Duty Cycle	Measured at DH		89	91	93	%
Minimum Duty Cycle	V_{COMP} = 1.25V, LX = GND, V_{BST} = V_{IN} = 3.3V			2.5	3	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, V_{BST} - V_{LX} = 5V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START					
Soft-Start Period			3.4		ms
Soft-Start Levels			12.5		mV
FET DRIVERS					
DH, DL Output Low Voltage	I_{SINK} = 10mA			0.1	V
DH, DL Output High Voltage	I_{SOURCE} = 10mA	V_{IN} - 0.1V or V_{BST} - 0.1V			V
DH Pullup/Pulldown, DL Pullup On-Resistance			1.5	3	Ω
DL Pulldown On-Resistance			1	2	Ω
LX, BST, HSD Leakage Current	V_{BST} = 18.7V, V_{LX} = 13.2V, V_{IN} = 5.5V, V_{HSD} = 13.2V			30	µA
THERMAL PROTECTION					
Thermal Shutdown	Rising temperature, 15°C hysteresis		+160		°C
SHUTDOWN CONTROL					
COMP Logic-Level Low	3V < V_{IN} < 5.5V			0.25	V
COMP Logic-Level High	3V < V_{IN} < 5.5V	0.8			V
COMP Pullup Current				100	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V, V_{BST} - V_{LX} = 5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
GENERAL				
Operating Input Voltage Range		3.0	5.5	V
HSD Voltage Range	(Note 1)	3.0	13.2	V
Quiescent Supply Current	V_{FB} = 1.5V		2	mA
Standby Supply Current	V_{IN} = V_{BST} = 5.5V, V_{HSD} = 13.2V, LX = unconnected, COMP = GND		2	mA
Undervoltage Lockout Trip Level	Rising V_{IN} 3% (typ) hysteresis	2.50	2.93	V
DC-DC CONTROLLER				
Output-Voltage Adjust Range (V_{OUT})		0.8	0.9 x V_{IN}	V
ERROR AMPLIFIER				
FB Regulation Voltage		-2.5	+1.0	%
Transconductance		70	160	µS
FB Input Leakage Current	V_{FB} = 0.9V		500	NA
FB Input Common-Mode Range		-0.1	+1.5	V
COMP Output-Voltage Swing		0.8	2.2	V

Low-Cost, Current-Mode PWM Buck Controller with Foldback Current Limit

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, V_{BST} - V_{LX} = 5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

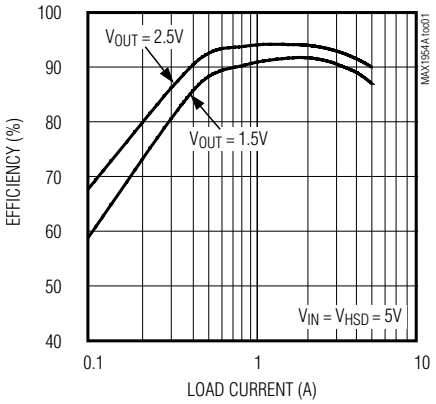
PARAMETER	CONDITIONS		MIN	MAX	UNITS
Current-Sense Amplifier Voltage Gain			3.15	3.85	V/V
Current-Limit Threshold	V_{PGND} - V_{LX}, MAX1954A	V_{FB} = 0.8V	110	145	mV
		V_{FB} = 0V	21	51	
OSCILLATOR					
Switching Frequency			240	360	kHz
Maximum Duty Cycle	Measured at DH		89	93	%
Minimum Duty Cycle	V_{COMP} = 1.25V, LX = GND, V_{BST} = V_{IN} = 3.3V			3	%
FET DRIVERS					
DH, DL Output Low Voltage	I_{SINK} = 10mA			0.1	V
DH, DL Output High Voltage	I_{SOURCE} = 10mA		V_{IN} - 0.1V or V_{BST} - 0.1V		V
DH Pullup/Pulldown, DL Pullup On-Resistance				3	Ω
DL Pulldown On-Resistance				2	Ω
LX, BST, HSD Leakage Current	V_{BST} = 18.7V, V_{LX} = 13.2V, V_{IN} = 5.5V, V_{HSD} = 13.2V			30	µA
SHUTDOWN CONTROL					
COMP Logic-Level Low	3V < V_{IN} < 5.5V			0.25	V
COMP Logic-Level High	3V < V_{IN} < 5.5V		0.8		V
COMP Pullup Current				100	µA

Note 1: HSD and IN are externally connected for applications where HSD < 5.5V.
Note 2: Specifications to -40°C are guaranteed by design and not production tested.

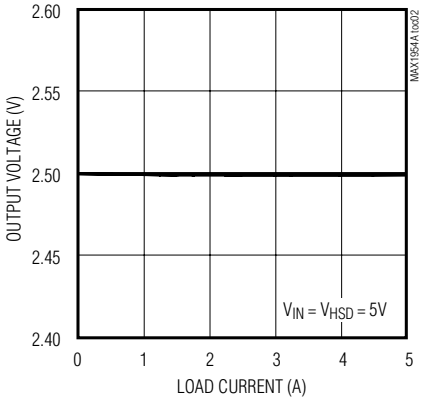
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

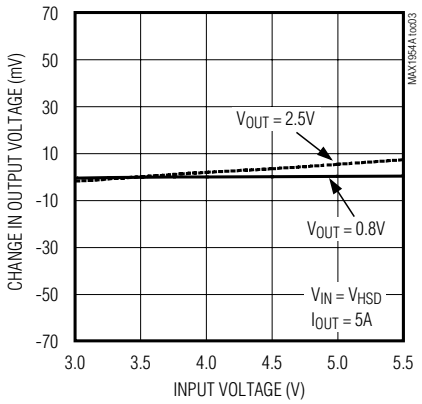
EFFICIENCY vs. LOAD CURRENT



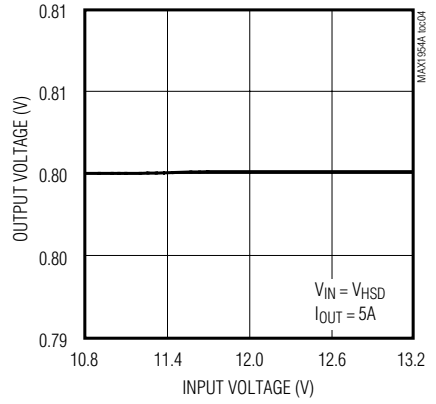
OUTPUT VOLTAGE vs. LOAD CURRENT



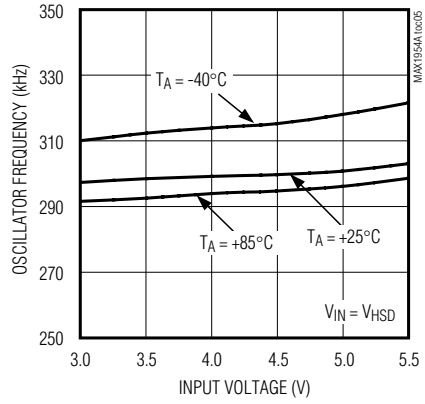
OUTPUT VOLTAGE CHANGE vs. INPUT VOLTAGE



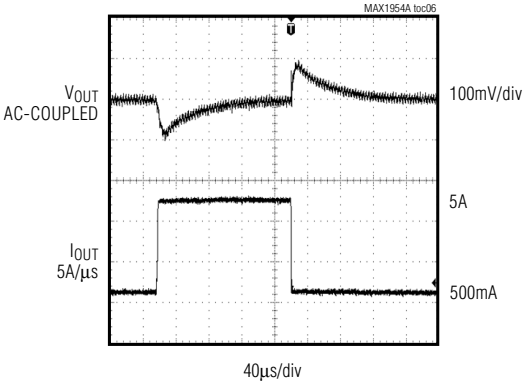
OUTPUT VOLTAGE vs. INPUT VOLTAGE



OSCILLATOR FREQUENCY vs. INPUT VOLTAGE



LOAD TRANSIENT

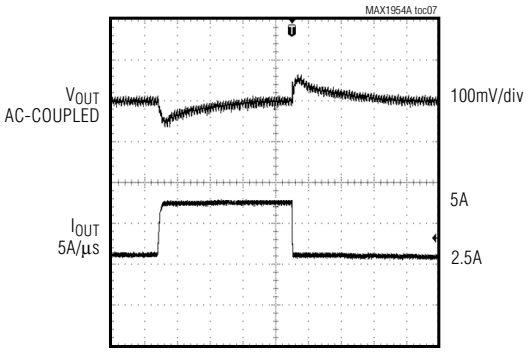


Low-Cost, Current-Mode PWM Buck Controller with Foldback Current Limit

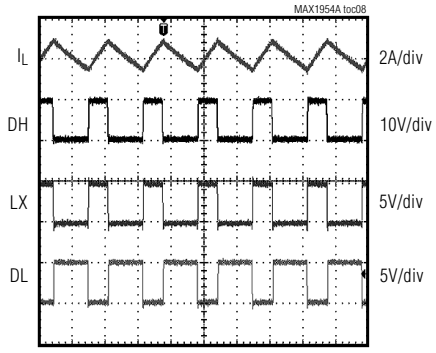
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

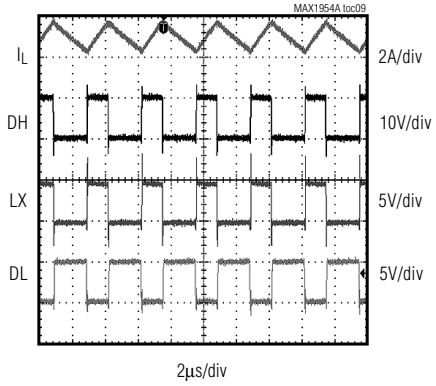
LOAD TRANSIENT



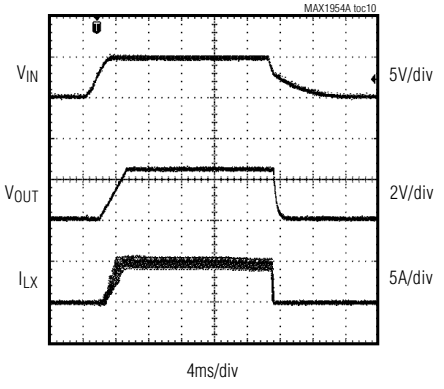
NO-LOAD SWITCHING WAVEFORMS



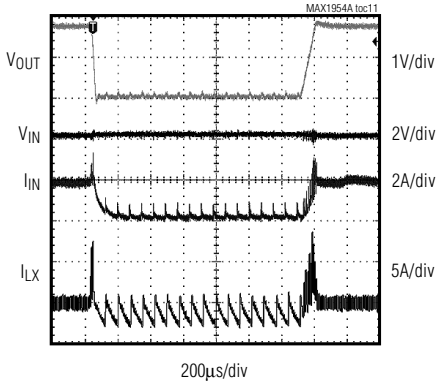
HEAVY-LOAD SWITCHING WAVEFORMS
I_{LOAD} = 5A



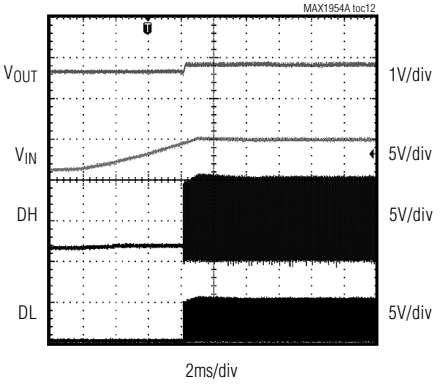
POWER-UP/POWER-DOWN WAVEFORMS



SHORT CIRCUIT AND RECOVERY



STARTUP INTO PREBIASED OUTPUT
(OUTPUT PREBIASED AT ~1.7V)



Pin Description

PIN	NAME	FUNCTION
1	HSD	High-Side Drain Current-Sense Input. HSD senses the voltage at the drain of the high-side, N-channel MOSFET. Connect to the high-side MOSFET drain using a Kelvin connection.
2	COMP	Compensation and Shutdown Control Pin. Connect appropriate RC networks to compensate the control loop. Pull to GND to shut down the IC. See the *Compensation Design* section for instructions on calculating the RC values.
3	FB	Feedback Input. Regulates at V_{FB} = 0.8V. Connect FB to the center tap of a resistor-divider from the output to GND to set the output voltage.
4	GND	Ground
5	IN	IC Supply Voltage. Provides power for the IC. Connect to a 3V to 5.5V power supply. Bypass to GND with a 0.22µF ceramic capacitor and to PGND with a 1µF ceramic capacitor.
6	DL	Low-Side Gate-Drive Output. Drives the synchronous-rectifier MOSFET. Swings from 0 to V_{IN}. DL is low in shutdown and UVLO.
7	PGND	Power Ground
8	DH	High-Side Gate-Drive Output. Drives the high-side N-channel MOSFET. DH is a floating driver output that swings from V_{LX} to V_{BST}. DH is low in shutdown and UVLO.
9	LX	Controller Current-Sense Input. Connect LX to the junction of the MOSFETs and inductor. LX is the reference point for the current limit.
10	BST	High-Side MOSFET Supply Input. Connect a 0.1µF ceramic capacitor from BST to LX to supply the necessary gate drive for the high-side N-channel MOSFET.

Detailed Description

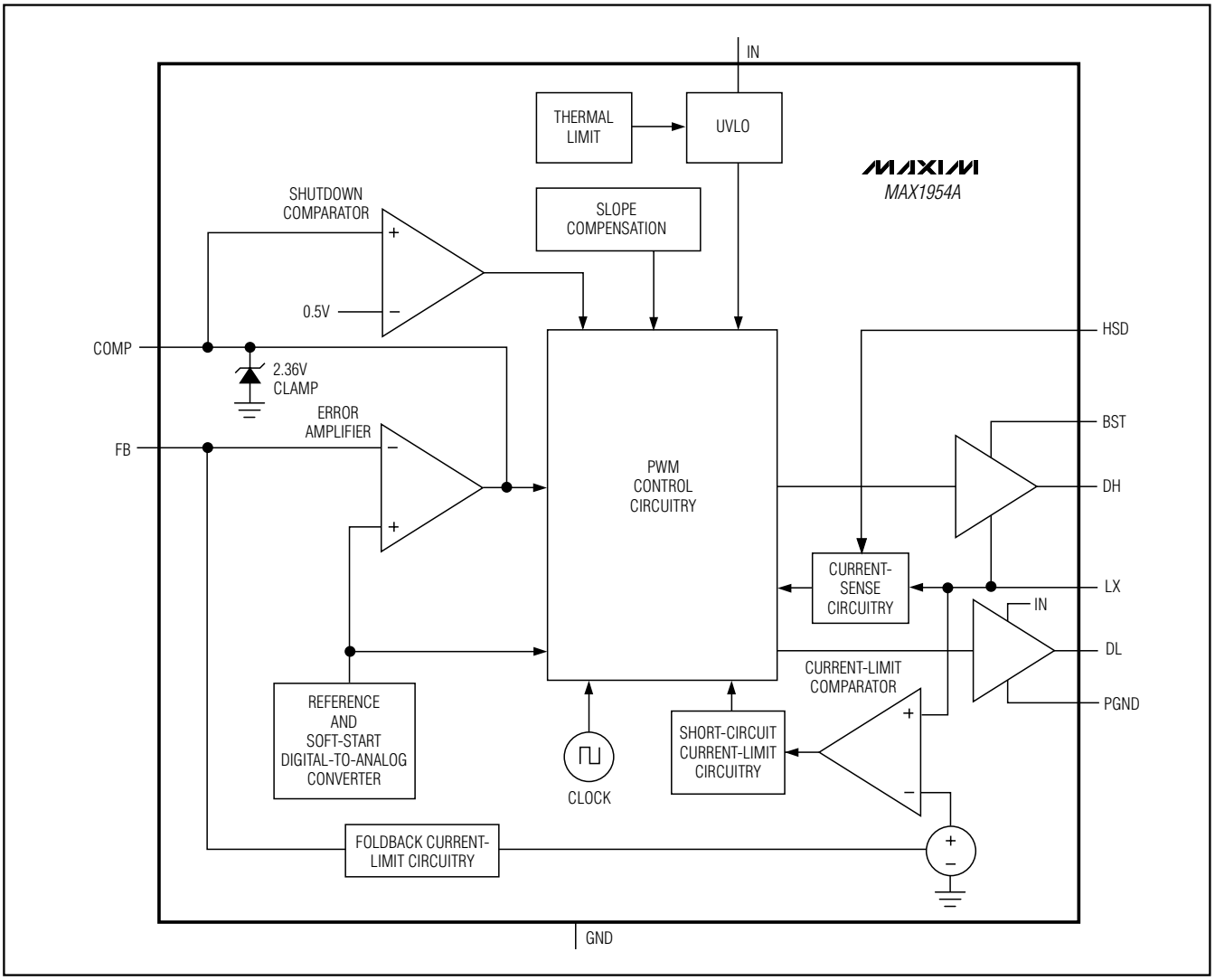
The MAX1954A single-output, current-mode, PWM, step-down DC-DC controller features foldback current limit and switches at 300kHz for high efficiency. The MAX1954A is designed to drive a pair of external N-channel power MOSFETs in a synchronous buck topology to improve efficiency and cost compared with a P-channel power-MOSFET topology. The on-resistance of the low-side MOSFET is used for short-circuit current-limit sensing, while the high-side MOSFET's on-resistance is used for current-mode feedback, thus eliminating the need for current-sense resistors. The short-circuit current limit is fixed at 135mV. The foldback current scheme reduces the input current during short-circuit and severe-overload conditions. The MAX1954A is configured with a high-side drain input (HSD) allowing an extended input voltage range of 3V to 13.2V that is independent of the IC input supply (Figure 1).

DC-DC Converter Control Architecture

The MAX1954A step-down converter uses a PWM, current-mode control scheme. An internal transconductance amplifier establishes an integrated error voltage. An open-loop comparator compares the integrated voltage-feedback signal against the amplified current-sense signal plus the slope compensation ramp, which is summed into the main PWM comparator to preserve inner-loop stability and eliminate inductor staircasing. At each rising edge of the internal clock, the high-side MOSFET turns on until the PWM comparator trips or the maximum duty cycle is reached. During this on-time, current ramps up through the inductor, storing energy in a magnetic field and sourcing current to the output. The current-mode feedback system regulates the peak inductor current as a function of the output-voltage error signal. The circuit acts as a switch-mode transconductance amplifier because the average inductor current is close to the peak inductor current (assuming the inductor is large enough to provide a reasonably small ripple current). This pushes the output inductance-capacitance filter pole normally found in a voltage-mode PWM to a higher frequency.

Low-Cost, Current-Mode PWM Buck Controller with Foldback Current Limit

Functional Diagram



During the second half of the cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as the current ramps down, providing current to the output. The output capacitor stores charge when the inductor current exceeds the required load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions, when the inductor current exceeds the current limit (see the *Current-Limit Circuit* section), the high-side MOSFET is not turned on at the rising clock edge and the low-side MOSFET remains on to let the inductor current ramp down.

The MAX1954A operates in a forced-PWM mode; therefore, the controller maintains a constant switching frequency, regardless of load, to allow for easier post-filtering of the switching noise.

Current-Sense Amplifier

The current-sense circuit amplifies the current-sense voltage (the high-side MOSFET's on-resistance ($R_{DS(ON)}$) multiplied by the inductor current). This amplified current-sense signal and the internal slope-compensation signal are summed (V_{SUM}) together and fed into the PWM comparator's inverting input. The PWM comparator shuts off the high-side MOSFET when V_{SUM} exceeds the integrated feedback voltage (V_{COMP}).

Typical Application Circuits

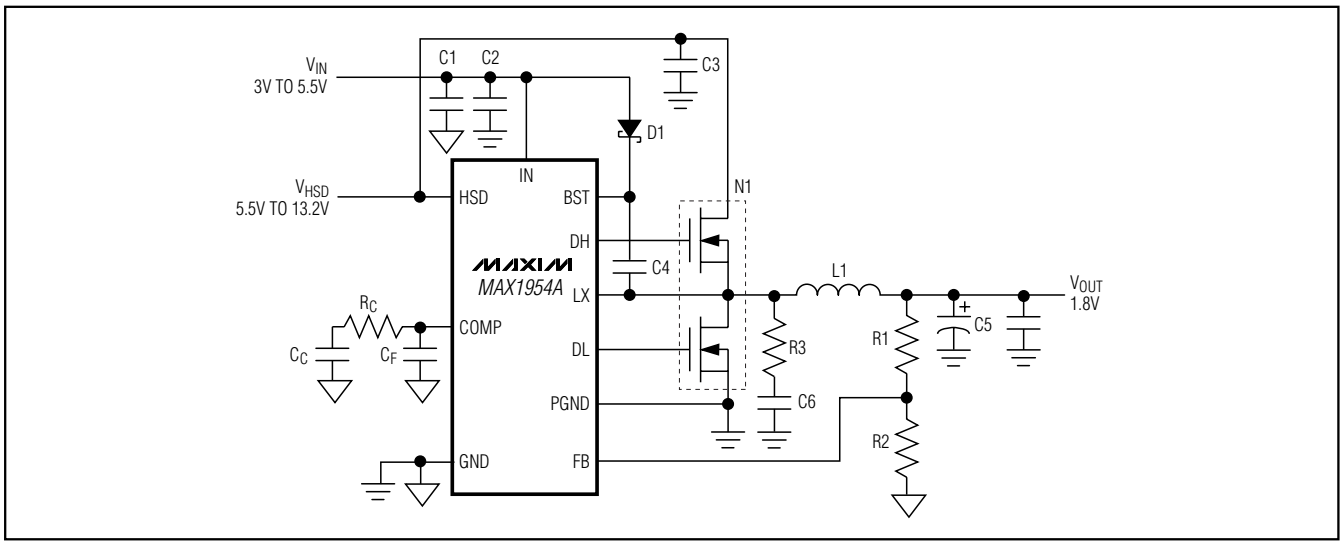


Figure 1. MAX1954A Typical Application Circuit

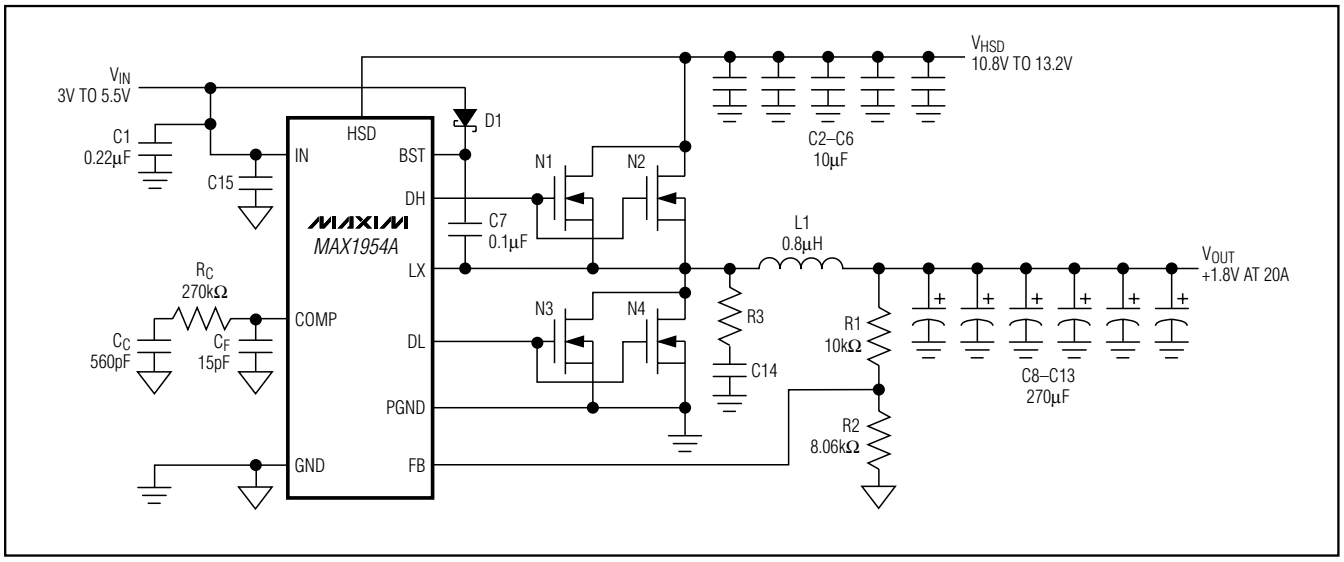


Figure 2. MAX1954A Circuit Capable of 20A Output

Place the high-side MOSFET as close as possible to the controller and connect HSD and LX to the MOSFET using Kelvin-sense connections to guarantee current-sense accuracy and improve stability.

Current-Limit Circuit

The current-limit circuit employs a lossless, foldback, valley current-limiting algorithm that uses the low-side MOSFET's on-resistance as the sensing element. Once the high-side MOSFET turns off, the voltage across the low-side MOSFET is monitored. If the voltage across the low-side MOSFET ($R_{DS(ON)}$ x $I_{INDUCTOR}$) does not exceed the current limit, the high-side MOSFET turns on normally. In this condition, the output drops smoothly out of regulation. If the voltage across the low-side MOSFET exceeds the current-limit threshold at the beginning of a new oscillator cycle, the low-side MOSFET remains on and the high-side MOSFET remains off.

Low-Cost, Current-Mode PWM Buck Controller with Foldback Current Limit

When the output is shorted, the foldback current limit reduces the current-limit threshold linearly to 20% of the nominal value to reduce the power dissipation of components and the input current. Once the voltage across the low-side MOSFET drops below the current-limit threshold, the high-side MOSFET is turned on at the next clock cycle. During severe-overload and short-circuit conditions, the frequency of the MAX1954A appears to decrease because the on-time of the low-side MOSFET extends beyond a clock cycle. The current-limit threshold is preset to 135mV.

In addition to the valley current limit, the MAX1954A also features a cycle-by-cycle peak-current clamp that limits the voltage across the high-side MOSFET by terminating its on-time. This, together with the valley foldback current limit, provides a very robust overload and short-circuit protection.

Synchronous-Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by replacing the normal Schottky catch diode with a low-resistance MOSFET switch. The MAX1954A also uses the synchronous rectifier to ensure proper startup of the boost gate-driver circuit and to provide the current-limit signal. The DL low-side waveform is always the complement of the DH high-side drive waveform (with controlled dead time to prevent crossconduction or shoot-through). A dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off. For the dead-time circuit to work properly, there must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate. Otherwise, the sense circuitry in the MAX1954A interprets the MOSFET gate as off although gate charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the device). The dead time at the other edge (DH turning off) is also determined through gate sensing.

High-Side Gate-Drive Supply (BST)

Gate-drive voltage for the high-side, N-channel switch is generated by a flying-capacitor boost circuit (Figure 3). The capacitor between BST and LX is charged from the V_{IN} supply up to V_{IN} minus the diode drop while the low-side MOSFET is on. When the low-side MOSFET is switched off, the stored voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage (V_{GS}) for the high-side MOSFET. The controller then closes an internal switch between BST and DH to turn the high-side MOSFET on.

Undervoltage Lockout (UVLO)

If V_{IN} drops below 2.7V, the MAX1954A assumes that the supply voltage is too low for proper circuit operation, so the UVLO circuitry inhibits switching and forces the DL and DH gate drivers low. After V_{IN} rises above 2.7V, the controller goes into the startup sequence and resumes normal operation.

Startup

The MAX1954A begins switching when V_{IN} rises above the UVLO threshold. However, the controller is not enabled unless five conditions are met:

1) V_{IN} exceeds the 2.7V UVLO threshold.
2) The internal reference exceeds 92% of its nominal value (V_{REF} > 1V).
3) The internal bias circuitry powers up.
4) The thermal-overload limit is not exceeded.
5) The feedback voltage is below the regulation threshold.

If these conditions are met, the step-down controller enables soft-start and begins switching. The soft-start circuitry gradually ramps up the output voltage until the voltage at FB is equal to the reference voltage. This controls the rate of rise of the output voltage and reduces input surge currents during startup. The soft-start period is 1024 clock cycles (1024 / f_S). The output voltage is incremented through 64 equal steps. The output reaches regulation when soft-start is completed, regardless of output capacitance and load.

The MAX1954A also has internal circuitry to prevent discharging of a precharged output capacitor during soft-start or in UVLO. This feature (monotonic startup) is needed in applications where the MAX1954A output is connected in parallel with another power-supply output, such as redundant-power or standby-power applications.

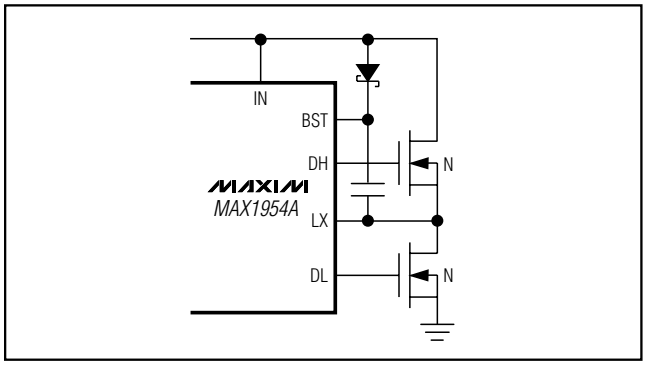


Figure 3. DH Boost Circuit

Table 1. Suggested Components

PART DESIGNATOR	MAX1954A (FIGURE 1)	20A CIRCUIT (FIGURE 2)
C1	0.22µF, 10V X7R ceramic capacitor Kemet C0603C224M8RAC	0.22µF, 10V X7R ceramic capacitor Kemet C0603C224M8RAC
C2	1µF, 6.3V X5R ceramic capacitor Taiyo Yuden JMK212BJ106MG	10µF, 16V X5R ceramic capacitor Taiyo Yuden EMK325BJ106MN
C3	10µF, 16V X5R ceramic capacitor Taiyo Yuden EMK325BJ106MN	10µF, 16V X5R ceramic capacitor Taiyo Yuden EMK325BJ106MN
C4	0.1µF, 6.3V X7R ceramic capacitor	10µF, 16V X5R ceramic capacitor Taiyo Yuden EMK325BJ106MN
C5	180µF, 4V SP polymer capacitor Panasonic EEFUEOG181R	10µF, 16V X5R ceramic capacitor Taiyo Yuden EMK325BJ106MN
C6	1500pF, 50V X7R ceramic capacitor TDK C1608X7R1H152K	10µF, 16V X5R ceramic capacitor Taiyo Yuden EMK325BJ106MN
C7	—	0.1µF, 50V X7R ceramic capacitor Taiyo Yuden UMK107BJ104KA
C8	—	270µF, 2V SP polymer capacitor Panasonic EEFUEOD271R
C9–C13	—	270µF, 2V SP polymer capacitors Panasonic EEFUEOD271R
C_C	680pF, 10V X7R ceramic capacitor Kemet C0402C681M8RAC	560pF, 10V X7R ceramic capacitor Kemet C0402C561M8RAC
C_F	—	15pF, 10V C0G ceramic capacitor Kemet C0402C150K8GAC
R1	16.9kΩ ±1% resistor	10kΩ ±1% resistor
R2	8.06kΩ ±1% resistor	8.06kΩ ±1% resistor
R3	2Ω ±5% resistor	—
R_C	62kΩ ±5% resistor	270kΩ ±5% resistor
D1	Schottky diode Central Semiconductor CMPSH1-4	Schottky diode Central Semiconductor CMPSH1-4
N1, N2	20V, 5A dual MOSFETs Fairchild FDS6898A	30V N-channel MOSFETs International Rectifier IRF7811
N3, N4	—	30V N-channel MOSFETs Siliconix Si4842DY
L1	1µH, 3.6A inductor TOKO 817FY-1R0M	0.8µH, 27.5A inductor Sumida CEP125U-0R8

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Shutdown

The MAX1954A features a low-power shutdown mode. Use an open-collector, NPN transistor to pull COMP low and shut down the IC. COMP must be pulled below 0.25V to shut down the MAX1954A. Choose a transistor with a $V_{CE(SAT)}$ below 0.25V. During shutdown, the output is high impedance. Shutdown reduces the quiescent current (I_Q) to 220µA (typ). Note that implementing shutdown in this fashion discharges the output only until the inductor runs out of energy. Upon recovery, soft-start is not available. Only the foldback current limit results in pseudo-soft-start mode.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX1954A. When the junction temperature exceeds T_J = +160°C, an internal thermal sensor shuts down the IC, allowing the IC to cool. The thermal sensor turns the IC on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

Design Procedures

Setting the Output Voltage

To set the output voltage for the MAX1954A, connect FB to the center of an external resistor-divider from the output to GND (Figures 1 and 2). Select R2 between 8kΩ and 24kΩ, and calculate R1 by:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 0.8V. R1 and R2 should be placed as close as possible to the IC.

Inductor Value

There are several parameters that must be examined when determining which inductor to use. Input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of inductor current ripple to DC load current. A higher LIR value allows for a smaller inductor, but results in higher losses and higher output ripple. A good compromise between size and efficiency is an LIR of 30%. Once all of the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR}$$

where f_S is the switching frequency. Choose a standard value close to the calculated value. The exact inductor value is not critical and can be adjusted to make tradeoffs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but eventually resistive losses, due to extra turns of wire, exceed the benefit gained from lower AC levels. Find a low-loss inductor with the lowest possible DC resistance that fits the allotted dimensions. Ferrite cores are often the best choice. However, powdered iron is inexpensive and can work well at 300kHz. The chosen inductor's saturation current rating must exceed the peak inductor current determined as:

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \right) \times I_{LOAD(MAX)}$$

Setting the Current Limit

The MAX1954A uses a valley current-sense method for current limiting. The voltage drop across the low-side MOSFET due to its on-resistance is used to sense the inductor current. The voltage drop across the low-side MOSFET at the valley point and at $I_{LOAD(MAX)}$ is:

$$V_{VALLEY} = R_{DS(ON)} \times \left(I_{LOAD(MAX)} - \left(\frac{LIR}{2} \right) \times I_{LOAD(MAX)} \right)$$

The calculated V_{VALLEY} must be less than the minimum current-limit threshold specified.

Additionally, the high-side MOSFET $R_{DS(ON)}$ must meet the following equation to avoid tripping the internal peak-current clamp circuit prematurely:

$$R_{DS(ON)} < 0.8V / (3.65 \times (I_{LOAD(MAX)} \times (1 + LIR / 2)))$$

Use the maximum $R_{DS(ON)}$ value at the desired maximum operating junction temperature of the MOSFET. A good general rule is to allow 0.5% additional resistance for each °C of MOSFET junction-temperature rise.

MOSFET Selection

The MAX1954A drives two external, logic-level, N-channel MOSFETs as the circuit-switch elements. The key selection parameters are:

1) On-resistance ($R_{DS(ON)}$): the lower, the better. However, the current-sense signal ($R_{DS} \times I_{PEAK}$) must be greater than 16mV at maximum load.
2) Maximum drain-to-source voltage (V_{DSS}): it should be at least 20% higher than the input supply rail at the high-side MOSFET's drain.
3) Gate charges (Q_g, Q_{gd}, Q_{gs}): the lower, the better.

For a 3.3V input application, choose a MOSFET with a rated $R_{DS(ON)}$ at V_{GS} = 2.5V. For a 5V input application, choose the MOSFETs with rated $R_{DS(ON)}$ at $V_{GS} \le 4.5V$. For a good compromise between efficiency and cost,

choose the high-side MOSFET (N1) that has conduction losses equal to switching loss at nominal input voltage and output current. The selected MOSFETs must have an $R_{DS(ON)}$ that satisfies the current-limit setting condition above. For N2, ensure that it does not spuriously turn on due to dV/dt caused by N1 turning on, as this would result in shoot-through current degrading the efficiency. MOSFETs with a lower Q_{gd}/Q_{gs} ratio have higher immunity to dV/dt.

For proper thermal-management design, the power dissipation must be calculated at the desired maximum operating junction temperature, $T_{J(MAX)}$. N1 and N2 have different loss components due to the circuit operation. N2 operates as a zero-voltage switch; therefore, major losses are the channel-conduction loss (P_{N2CC}) and the body-diode conduction loss (P_{N2DC}).

$$V_{VALLEY} = R_{DS(ON)} \times \left(I_{LOAD(MAX)} - \left(\frac{LIR}{2}\right) \times I_{LOAD(MAX)}\right)$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$.

$$P_{N2DC} = 2 \times I_{LOAD} \times V_F \times t_{dt} \times f_S$$

where V_F is the body-diode forward-voltage drop, t_{dt} is the dead time between N1 and N2 switching transitions, f_S is the switching frequency, and t_{dt} is 20ns (typ).

N1 operates as a duty-cycle control switch and has the following major losses: the channel-conduction loss (P_{N1CC}), the VL overlapping switching loss (P_{N1SW}), and the drive loss (P_{N1DR}). N1 does not have body-diode conduction loss, because the diode never conducts current.

$$P_{N1CC} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I^2_{LOAD} \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$.

$$P_{N1SW} = V_{IN} \times I_{LOAD} \times \left(\frac{Q_{gs} + Q_{gd}}{I_{GATE}}\right) \times f_S$$

where I_{GATE} is the average DH-driver output current capability determined by:

$$I_{GATE} \cong 0.5 \times \frac{V_{IN}}{R_{DS(ON)(N2)} + R_{GATE}}$$

where $R_{DS(ON)(N2)}$ is the high-side MOSFET driver's on-resistance (1.5Ω typ) and R_{GATE} is the internal gate resistance of the MOSFET (~2Ω).

$$P_{N1DR} = Q_g \times V_{GS} \times f_S \times \frac{R_{GATE}}{R_{GATE} + R_{DS(ON)(N2)}}$$

where $V_{GS} \sim V_{IN}$.

In addition to the losses above, allow approximately 20% for additional losses due to MOSFET output capacitances and N2 body-diode reverse-recovery charge dissipated in N1 that exists, but is not well defined, in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal-resistance specification to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above calculated power dissipations.

To reduce electromagnetic interference (EMI) caused by switching noise, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source or add resistors in series with DH and DL to slow down the switching transitions. However, adding series resistors increases the power dissipation of the MOSFET, so be sure this does not overheat the MOSFET.

The minimum load current must exceed the high-side MOSFET's maximum leakage-current overtemperature if fault conditions are expected.

MOSFET Snubber Circuit

Fast-switching transitions cause ringing because of resonating circuit parasitic inductance and capacitance at the switching nodes. This high-frequency ringing occurs at LX's rising and falling transitions and can interfere with circuit performance and generate EMI. To dampen this ringing, a series RC snubber circuit is added across each switch. Below is the procedure for selecting the value of the series RC circuit:

1) Connect a scope probe to measure the voltage from LX to GND, and observe the ringing frequency, f_R.
2) Find the capacitor value (connected from LX to GND) that reduces the ringing frequency by half.

The circuit parasitic capacitance (C_{PAR}) at LX is then equal to 1/3rd of the value of the added capacitance above. The circuit parasitic inductance (L_{PAR}) is calculated by:

$$L_{PAR} = \frac{1}{(2\pi f_R)^2 \times C_{PAR}}$$

The resistor for critical dampening (R_{SNUB}) is equal to $2\pi \times f_R \times L_{PAR}$. Adjust the resistor value up or down to tailor the desired damping and the peak voltage excursion. The capacitor (C_{SNUB}) should be at least two to four times the value of the C_{PAR} to be effective. The power loss of the snubber circuit (P_{RSNUB}) is dissipated in the resistor R_{SNUB} and can be calculated as:

$$P_{RSNUB} = C_{SNUB} \times (V_{IN})^2 \times f_S$$

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where V_{IN} is the input voltage and f_S is the switching frequency. Choose a R_{SNUB} power rating that meets the specific application's derating rule for the power dissipation calculated.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{IN} = 2 \times V_{OUT}$); therefore, $I_{RMS(MAX)} = I_{LOAD} / 2$. Ceramic capacitors are recommended due to their low equivalent series resistance (ESR) and equivalent series inductance (ESL) at high frequencies, and their relatively low cost. Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating root-mean-square (RMS) current for optimum long-term reliability.

Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, ESR, ESL, and the voltage-rating requirements. These parameters affect the overall stability, output voltage ripple, and transient response. The output ripple has three components: variations in the charge stored in the output capacitor, and the voltage drop across the capacitor's ESR and ESL caused by the current into and out of the capacitor. The equation below estimates the maximum ripple voltage:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

The output voltage ripple as a consequence of the ESR, output capacitance, and ESL are as follows:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESL)} = \left(\frac{V_{IN}}{L}\right) \times ESL$$

$$I_{P-P} = \left(\frac{V_{IN} - V_{OUT}}{f_S \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right)$$

where I_{P-P} is the peak-to-peak inductor current (see the *Inductor Value* section). These equations are suitable for initial capacitor selection, but final values should be chosen based on a prototype or evaluation circuit. As a general rule, a smaller current ripple results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value and input voltage, the output voltage ripple decreases with larger inductance, and increases with higher input voltages. For the MAX1954A polymer, tantalum, or aluminum electrolytic capacitors are recommended. Lower-cost aluminum electrolytic capacitors with relatively low ESR are available and can be used for the MAX1954A, if the larger physical size is acceptable. For reliable and safe operation, ensure that the capacitor's voltage and ripple-current ratings exceed the calculated values.

The devices' response to a load transient depends on the selected output capacitors. After a load transient, the output voltage instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output voltage deviates further depending on the inductor and output capacitor values. After a short period of time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on its closed-loop bandwidth. With a higher bandwidth, the response time is faster, thus preventing the output voltage from deviating further from its regulation value.

Compensation Design

The MAX1954A uses an internal transconductance error amplifier whose output compensates the control loop. The external inductor, high-side MOSFET, output capacitor, compensation resistor, and compensation capacitors determine the loop stability. The inductor and output capacitors are chosen based on performance, size, and cost. Additionally, the compensation resistor and capacitors are selected to optimize control-loop stability. The component values in Figures 1 and 2 yield stable operation over the given range of input-to-output voltages and load currents. The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The MAX1954A uses the voltage across the high-side MOSFET's on-resistance ($R_{DS(ON)}$) to sense the inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation. A single-series compensation resistor (R_C) and compensation capacitor (C_C) is all that is needed to have a stable high-bandwidth loop in applications where ceramic capacitors are used for

output filtering. For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. Another compensation capacitor should be added to cancel this zero.

The basic regulator loop can be thought of as a power modulator, output feedback divider, and an error amplifier. The power modulator has DC gain set by $g_{mc} \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}) and its equivalent series resistance (R_{ESR}). Below are equations that define the power modulator:

$$G_{MOD} = g_{mc} \times \frac{R_{LOAD} \times f_S \times L}{R_{LOAD} + f_S \times L}$$

where $R_{LOAD} = V_{OUT} / I_{OUT(MAX)}$, and $g_{mc} = 1 / (A_{CS} \times R_{DS(ON)})$, where A_{CS} is the gain of the current-sense amplifier and $R_{DS(ON)}$ is the on-resistance of the high-side power MOSFET. A_{CS} is 3.5. The frequencies at which the pole and zero due to the power modulator occur are determined as follows:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times \left(\frac{R_{LOAD} \times f_S \times L}{R_{LOAD} + f_S \times L} + R_{ESR} \right)}$$

$$f_{zMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$$

The feedback voltage-divider used has a gain of $G_{FB} = V_{FB} / V_{OUT}$, where V_{FB} is equal to 0.8V. The transconductance error amplifier has DC gain, $G_{EA(DC)} = g_m \times R_O$. The amplifier output resistance (R_O) is typically 10MΩ. The C_C, R_O, and the R_C set a dominant pole. The R_C and the C_C set a zero. There is an optional pole set by C_F and R_C to cancel the output-capacitor ESR zero if it occurs before crossover frequency (f_C):

$$f_{pdEA} = \frac{1}{2\pi \times C_C \times (R_O + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The f_C should be much higher than the power modulator pole f_{PMOD}. Also, the crossover frequency should be less than 1/8th of the switching frequency:

$$f_{pMOD} << f_C < \frac{f_S}{8}$$

Therefore, the loop-gain equation at the crossover frequency is:

$$G_{EA(fC)} \times G_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} = 1$$

When f_{zMOD} is greater than f_C:

$$G_{EA(fC)} = g_{mEA} \times R_C \text{ and } G_{MOD(fC)} = g_{mc} \times R_{LOAD} \times \frac{f_{pMOD}}{f_C}$$

then R_C is calculated as:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times G_{MOD(fC)}}$$

where g_{mEA} = 110µs.

The error-amplifier compensation zero formed by R_C and C_C should be set at the modulator pole f_{pMOD}. C_C is calculated by:

$$C_C = \frac{R_{LOAD} \times f_S \times L \times C_{OUT}}{(R_{LOAD} + (f_S \times L)) \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second compensation capacitor, C_f, from COMP to GND to cancel the ESR zero. C_f is calculated by:

$$C_f = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

As the load current decreases, the modulator pole also decreases. However, the modulator gain increases accordingly and the crossover frequency remains the same.

When f_{zMOD} is less than f_C, the power-modulator gain at f_C is:

$$G_{MOD(fC)} = G_{MOD(DC)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

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The error-amplifier gain at f_C is:

$$G_{EA(fC)} = g_{mEA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

R_C is then calculated as:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{f_C}{g_{mEA} \times f_{zMOD} \times G_{MOD(fC)}}$$

C_C and C_f can then be calculated as:

$$C_C = \frac{R_{LOAD} \times f_S \times L \times C_{OUT}}{(R_{LOAD} + f_S \times L) \times R_C}$$

$$C_f = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

Applications Information

See Table 2 for suggested manufacturers of the components used with the MAX1954A.

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place IC decoupling capacitors as close as possible to IC pins. Keep separate the power-ground plane (connected to pin 7) and the signal-ground plane (connected to pin 4). The IN pin has two decoupling capacitors. One connects to pin 7 and one connects to pin 4.
2) Place the MOSFETs' decoupling capacitors as close as possible and place them directly across from the high-side MOSFET drain and the low-side MOSFET source.
3) Input and output capacitors are connected to the power-ground plane; all other capacitors are connected to the signal-ground plane.
4) Keep the high-current paths as short as possible.
5) Connect the drain leads of the power MOSFET to a large copper area to help cool the device. Refer to the power MOSFET data sheet for recommended copper area.
6) Connect HSD directly to the drain leads of the high-side MOSFET.
7) Connect LX directly to the drain of the low-side MOSFET.
8) Place the low-side MOSFET so that its source is as close as possible to pin 7.
9) Ensure all feedback connections are short and direct. Place the feedback resistors as close as possible to the IC.
10) Route high-speed switching nodes away from sensitive analog areas (FB, COMP).
11) The trace length from the gates of the low-side and high-side MOSFETs to DH and DL should be no longer than 700 mils.

To aid design, a sample layout is available in the MAX1954A evaluation kit.

Table 2. Suggested Manufacturers

MANUFACTURER	COMPONENT	PHONE	WEBSITE
Central Semiconductor	Diodes	631-435-1110	www.centralsemi.com
Coilcraft	Inductors	800-322-2645	www.coilcraft.com
Fairchild	MOSFETs	800-341-0392	www.fairchildsemi.com
Kemet	Capacitors	864-963-6300	www.kemet.com
Panasonic	Capacitors	714-373-7366	www.panasonic.com
Taiyo Yuden	Capacitors	408-573-4150	www.t-yuden.com
TOKO	Inductors	800-745-8656	www.toko.com

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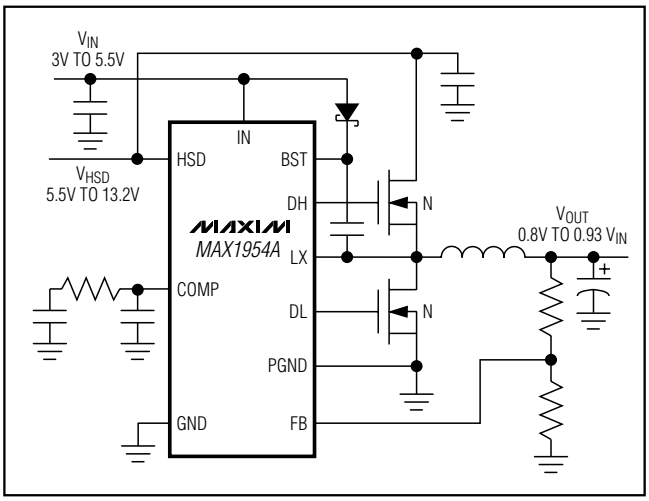
Typical Operating Circuit



Chip Information

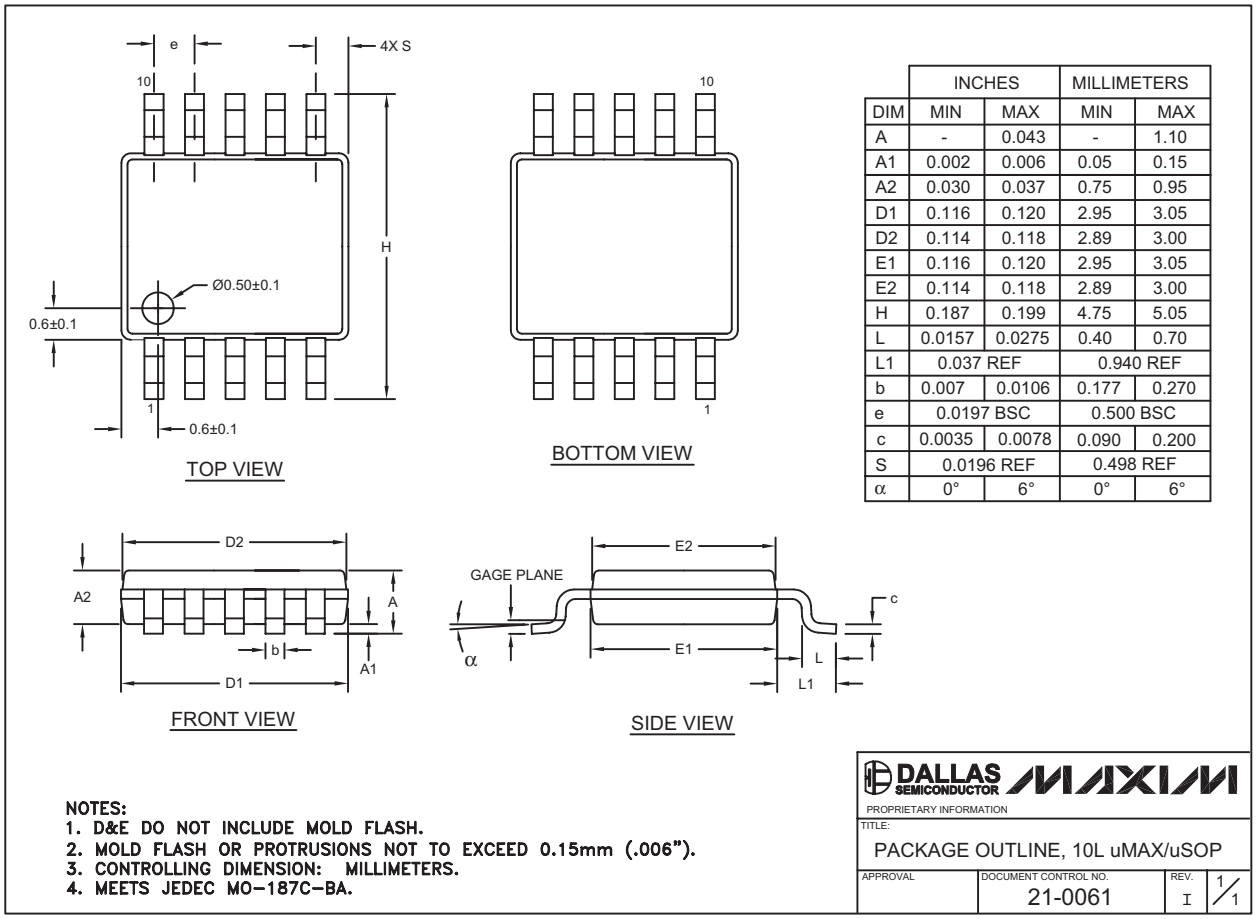
TRANSISTOR COUNT: 2963

PROCESS: BiCMOS

Low-Cost, Current-Mode PWM Buck Controller with Foldback Current Limit

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

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