Phase-Shifted Full-Bridge Controller With Synchronous Rectification

Check for Samples: UCC28950-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40ºC to 125ºC Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **Enhanced Wide-Range Resonant Zero-Voltage Switching (ZVS) Capability**
- **Direct Synchronous Rectifier (SR) Control**
- **Light-Load Efficiency Management Including**
  - **Burst Mode Operation**
  - **Discontinuous Conduction Mode (DCM), Dynamic SR On/Off Control With Programmable Threshold**
  - **Programmable Adaptive Delay**
- **Average- or Peak-Current Mode Control With Programmable Slope Compensation and Voltage-Mode Control**
- **Closed-Loop Soft-Start and Enable Function**
- **Programmable Switching Frequency up to 1 MHz with Bidirectional Synchronization**
- **(±3%) Cycle-by-Cycle Current Limit Protection With Hiccup Mode Support**
- **150-µA Start-Up Current**
- **V_{DD} Undervoltage Lockout**
- **Wide Temperature Range, –40°C to 125°C**

APPLICATIONS

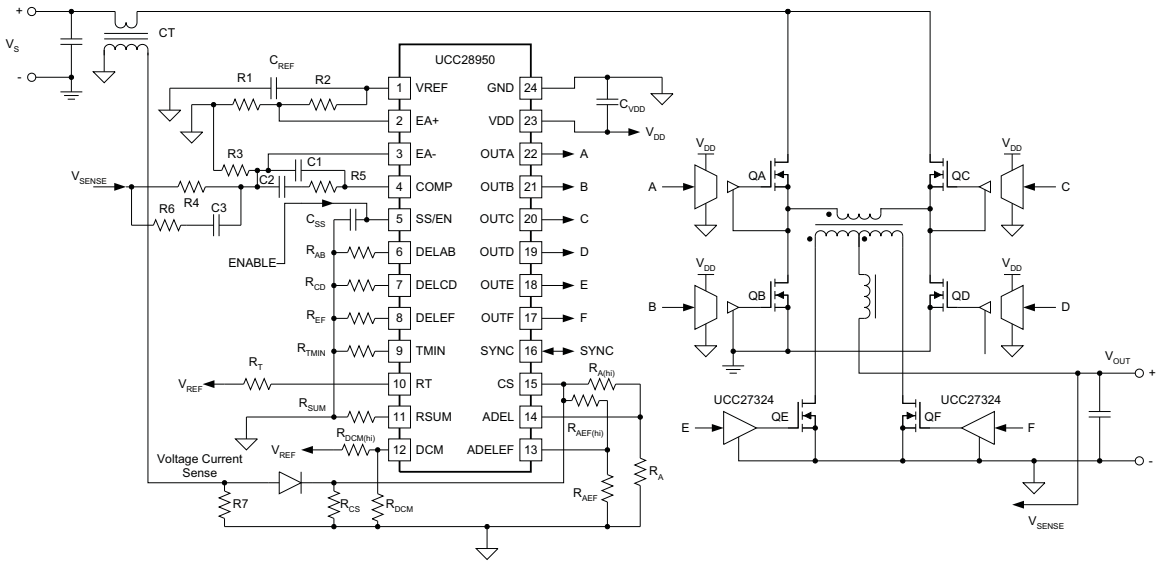
- **Phase-Shifted Full-Bridge Converters**
- **Industrial Power Systems**
- **High-Density Power Architectures**
- **Solar Inverters and Electric Vehicles**

DESCRIPTION

The UCC28950-Q1 enhanced phase-shifted controller builds upon Texas Instruments' industry-standard UCCx895 phase-shifted controller family with enhancements that offer best-in-class efficiency in today's high-performance power systems. The UCC28950-Q1 implements advanced control of the full bridge along with active control of the synchronous-rectifier output stage.

The primary-side signals allow programmable delays to ensure ZVS operation over wide load-current and input-voltage ranges, while the load current naturally tunes the secondary-side switching delays of the synchronous rectifiers, maximizing overall system efficiency.

UCC28950-Q1 Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONT.)

The UCC28950-Q1 also offers multiple light-load management features, including burst mode and dynamic SR on/off control when transitioning in and out of discontinuous-current-mode (DCM) operation, ensuring ZVS operation is extended down to much lighter loads.

In addition, the UCC28950-Q1 includes support for peak current along with voltage-mode control, programmable switching frequency up to 1 MHz, and a wide set of protection features including cycle-by-cycle current limit, UVLO, and thermal shutdown. It is easy to arrange 90-degree phase-shifted interleaved synchronized operation between two converters.

The UCC28950-Q1 is available in a TSSOP-24 package.

ORDERING INFORMATION

T_A	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	UCC28950QPWRQ1	UCC28950Q

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)

PARAMETER	VALUE	UNIT
Input supply voltage range, V_{DD} (3)	–0.4 to 20	V
OUTA, OUTB, OUTC, OUTD, OUTE, OUTF	–0.4 to V_{DD} + 0.4	
Inputs voltages on DELAB, DELCD, DELEF, SS/EN, DCM, TMIN, RT, SYNC, RSUM, EA+, EA–, COMP, CS, ADEL, ADELEF	–0.4 to V_{REF} + 0.4	
Output voltage on VREF	–0.4 to 5.6	
Continuous total power dissipation	See dissipation rating table	
Operating virtual junction temperature range, T_J	–40 to 150	°C
Storage temperature, T_{stg}	–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(3) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See the *Package Options Addendum* of the data sheet for thermal limitations and considerations of packages.

THERMAL INFORMATION

THERMAL METRIC(1)		UCC28950-Q1 PW 24 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	93.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	24.2	°C/W
θ_{JB}	Junction-to-board thermal resistance	47.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, V_{DD}	8	12	17	V
Operating ambient temperature range	-40		125	°C
Converter switching frequency setting range, $f_{SW(nom)}$	50		1000	kHz
Programmable delay range between OUTA, OUTB and OUTC, OUTD set by resistors DELAB and DELCD and parameter K_A (1)	30		1000	ns
Programmable delay range between OUTA, OUTF and OUTB, OUTE set by resistor DELEF, and parameter K_{EF} (1)	30		1400	
Programmable DCM range as percentage of voltage at CS (1)	5%		30%	
Programmable t_{MIN} range	100		800	ns

(1) Verified during characterization only.

ELECTRICAL CHARACTERISTICS (1)

V_{DD} = 12 V, T_A = –40°C to 125°C, C_{VDD} = 1 µF, C_{REF} = 1 µF, R_{AB} = 22.6 kΩ, R_{CD} = 22.6 kΩ , R_{EF} = 13.3 kΩ, R_{SUM} = 124 kΩ, RMIN = 88.7 kΩ, R_T = 59 kΩ connected between RT pin and 5-V voltage supply to set f_{SW} = 100 kHz (f_{OSC} = 200 kHz) (unless otherwise noted). All component designations are from the Typical Application Diagram, Figure 2.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Under Voltage Lockout (UVLO)						
UVLO_RTH	Start threshold		6.75	7.3	7.9	V
UVLO_FTH	Minimum operating voltage after start		6.15	6.7	7.2	
UVLO_HYST	Hysteresis		0.53	0.6	0.75	
Supply Currents						
$I_{DD(off)}$	Startup current	V_{DD} is 5.2 V		150	270	µA
I_{DD}	Operating supply current			5	10	mA
VREF Output Voltage						
V_{REF}	VREF total output range	0 ≤ IR ≤ 20 mA; V_{DD} = from 8 V to 17 V	4.925	5	5.075	V
I_{SCC}	Short-circuit current	VREF = 0 V	–53		–23	mA
Switching Frequency (½ of internal oscillator frequency f_{OSC})						
$f_{SW(nom)}$	Total range		92	100	108	KHz
D_{MAX}	Maximum duty cycle			95%	97%	
Synchronization						
PH_{SYNC}	Total range	R_T = 59 kΩ between RT and GND; Input pulses 200 kHz, D = 0.5 at SYNC	85	90	95	°PH
f_{SYNC}	Total range	R_T = 59 kΩ between RT and 5 V; –40 °C ≤ T_A ≤ 125°C	180	200	220	kHz
t_{PW}	Pulse duration		2.2	2.5	2.8	µs

(1) Typical values for T_A = 25°C

ELECTRICAL CHARACTERISTICS(1) (continued)

V_{DD} = 12 V, T_A = –40°C to 125°C, C_{VDD} = 1 µF, C_{REF} = 1 µF, R_{AB} = 22.6 kΩ, R_{CD} = 22.6 kΩ , R_{EF} = 13.3 kΩ, R_{SUM} = 124 kΩ, RMIN = 88.7 kΩ, R_T = 59 kΩ connected between RT pin and 5-V voltage supply to set f_{SW} = 100 kHz (f_{OSC} = 200 kHz) (unless otherwise noted). All component designations are from the Typical Application Diagram, Figure 2.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amplifier						
V_{ICM}	Common mode input voltage range	V_{ICM} range ensures parameters, the functionality ensured for 3.6 V < V_{ICM} < V_{REF} + 0.4 V, and –0.4 V < V_{ICM} < 0.5 V	0.5		3.6	V
V_{IO}	Offset voltage		–7		7	mV
I_{BIAS}	Input bias current		–1		1	µA
EA_{HIGH}	High-level output voltage	(EA+) – (EA–) = 500 mV, I_{EAOUT} = –0.5 mA	3.9	4.25		V
EA_{LOW}	Low-level output voltage	(EA+) – (EA–) = –500 mV, I_{EAOUT} = 0.5 mA		0.25	0.35	
I_{SOURCE}	Error-amplifier source current		–8	–3.75	–0.5	mA
I_{SINK}	Error-amplifier sink current		2.7	4.6	5.75	
I_{VOL}	Open-loop dc gain			100		dB
GBW	Unity gain bandwidth(2)			3		MHz
Cycle-by-Cycle Current Limit						
V_{CS_LIM}	CS pin cycle-by-cycle threshold		1.94	2	2.06	V
T_{CS}	Propagation delay from CS to OUTC and OUTD outputs	Input pulse between CS and GND from zero to 2.5 V		100		ns
Internal Hiccup Mode Settings						
I_{DS}	Discharge current to set cycle-by-cycle current limit duration	CS = 2.5 V, VSS = 4 V	15	20	25	µA
V_{HCC}	Hiccup off-time threshold		3.2	3.6	4.2	V
I_{HCC}	Discharge current to set hiccup-mode off-time		1.9	2.55	3.2	µA
Soft Start/Enable						
I_{SS}	Charge current	V_{SS} = 0 V	20	25	30	µA
V_{SS_STD}	Shutdown/restart/reset threshold		0.25	0.5	0.7	V
V_{SS_PU}	Pullup threshold		3.3	3.7	4.3	
V_{SS_CL}	Clamp voltage		4.2	4.65	4.95	

(2) Verified during characterization only.

ELECTRICAL CHARACTERISTICS(1) (continued)

V_{DD} = 12 V, T_A = –40°C to 125°C, C_{VDD} = 1 µF, C_{REF} = 1 µF, R_{AB} = 22.6 kΩ, R_{CD} = 22.6 kΩ , R_{EF} = 13.3 kΩ, R_{SUM} = 124 kΩ, RMIN = 88.7 kΩ, R_T = 59 kΩ connected between RT pin and 5-V voltage supply to set f_{SW} = 100 kHz (f_{OSC} = 200 kHz) (unless otherwise noted). All component designations are from the Typical Application Diagram, Figure 2.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Programmable Delay Time Set Accuracy and Range(3)(4)(5)(6)(7)						
t_{ABSET1}	Short delay time set accuracy between OUTA and OUTB	CS = ADEL = ADELEF = 1.8 V	32	45	56	ns
t_{ABSET2}	Long delay time set accuracy between OUTA and OUTB	CS = ADEL = ADELEF = 0.2 V	216	270	325	ns
t_{CDSET1}	Short delay time set accuracy between OUTC and OUTD	CS = ADEL = ADELEF = 1.8 V	32	45	56	ns
t_{CDSET2}	Long delay time set accuracy between OUTC and OUTD	CS = ADEL = ADELEF = 0.2 V	216	270	325	ns
t_{AFSET1}	Short delay time set accuracy between falling OUTA, OUTF	CS = ADEL = ADELEF = 0.2 V	22	35	48	ns
t_{AFSET2}	Long delay time set accuracy between falling OUTA, OUTF	CS = ADEL = ADELEF = 1.8 V	190	240	290	ns
t_{BESET1}	Short delay time set accuracy between falling OUTB, OUTE	CS = ADEL = ADELEF = 0.2 V	22	35	48	ns
t_{BESET2}	Long delay time set accuracy between falling OUTB, OUTE	CS = ADEL = ADELEF = 1.8 V	190	240	290	ns
Δt_{ADBC}	Pulse matching between OUTA rise, OUTD fall and OUTB rise, OUTC fall	CS = ADEL = ADELEF = 1.8 V, COMP = 2 V	-50	0	50	ns
Δt_{ABBA}	Half cycle matching between OUTA rise, OUTB rise and OUTB rise, OUTA rise	CS = ADEL = ADELEF = 1.8 V, COMP = 2 V	-50	0	50	ns
Δt_{EEFF}	Pulse matching between OUTE fall, OUTE rise and OUTF fall, OUTF rise	CS = ADEL = ADELEF = 0.2 V, COMP = 2 V	-60	0	60	ns
Δt_{EFFE}	Pulse matching between OUTE fall, OUTF rise and OUTF fall, OUTE rise	CS = ADEL = ADELEF = 0.2 V, COMP = 2 V	-60	0	60	ns

(3) See Figure 6 for timing diagram and t_{ABSET1}, t_{ABSET2}, t_{CDSET1}, t_{CDSET2} definitions.
(4) See Figure 9 for timing diagram and t_{AFSET1}, t_{AFSET2}, t_{BESET1}, t_{BESET2} definitions.
(5) Pair of outputs OUTC, OUTE and OUTD, OUTF always going high simultaneously.
(6) Outputs A or B are never allowed to go high if both outputs OUTE and OUTF are high.
(7) All delay settings are measured relatively 50% of pulse amplitude.

ELECTRICAL CHARACTERISTICS(1) (continued)

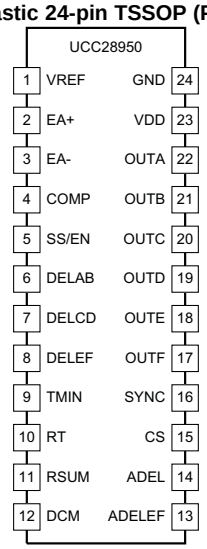
V_{DD} = 12 V, T_A = –40°C to 125°C, C_{VDD} = 1 µF, C_{REF} = 1 µF, R_{AB} = 22.6 kΩ, R_{CD} = 22.6 kΩ , R_{EF} = 13.3 kΩ, R_{SUM} = 124 kΩ, RMIN = 88.7 kΩ, R_T = 59 kΩ connected between RT pin and 5-V voltage supply to set f_{SW} = 100 kHz (f_{OSC} = 200 kHz) (unless otherwise noted). All component designations are from the Typical Application Diagram, Figure 2.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Light-Load Efficiency Circuit						
V_{DCM}	DCM threshold, T = 25°C	V_{DCM} = 0.4 V, Sweep CS confirm there are OUTE and OUTF pulses	0.37	0.39	0.41	V
	DCM threshold, T = 0°C to 85°C (8)	V_{DCM} = 0.4 V, Sweep CS, confirm there are OUTE and OUTF pulses	0.364	0.390	0.416	
	DCM threshold, T= –40°C to 125°C (8)	V_{DCM} = 0.4 V, Sweep CS, confirm there are OUTE and OUTF pulses	0.35	0.39	0.43	
$I_{DCM,SRC}$	DCM sourcing current	CS < DCM threshold	14	20	26	µA
t_{MIN}	Total range	R_{TMIN} = 88.7 kΩ	425	525	625	ns
OUTPUTS OUTA, OUTB, OUTC, OUTD, OUTE, OUTF						
$I_{SINK/SRC}$	Sink/Source peak current(8)			0.2		A
t_r	Rise time	C_{LOAD} = 100 pF		9	25	ns
t_f	Fall time	C_{LOAD} = 100 pF		7	25	ns
R_{SRC}	Output source resistance	I_{OUT} = 20 mA	10	20	35	Ω
R_{SINK}	Output sink resistance	I_{OUT} = 20 mA	5	10	30	Ω
THERMAL SHUTDOWN						
	Rising threshold(8)			160		°C
	Falling threshold(8)			140		°C
	Hysteresis			20		°C

(8) Verified during characterization only

DEVICE INFORMATION

Plastic 24-pin TSSOP (PW)



PIN FUNCTIONS

PIN		I/O	FUNCTION
NUMBER	NAME		
1	VREF	O	5-V, ±1.5%, 20-mA reference voltage output
2	EA+	I	Error amplifier non-inverting input
3	EA–	I	Error amplifier inverting input
4	COMP	I/O	Error amplifier output and input to the PWM comparator
5	SS/EN	I	Soft-start programming, device enable and hiccup-mode protection circuit
6	DELAB	I	Dead-time delay programming between OUTA and OUTB
7	DELCD	I	Dead-time delay programming between OUTC and OUTD
8	DELEF	I	Delay-time programming between OUTA to OUTF, and OUTB to OUTE
9	TMIN	I	Minimum duty-cycle programming in burst mode
10	RT	I	Oscillator frequency set. Master- or slave-mode setting
11	RSUM	I	Slope compensation programming. Voltage-mode or peak-current-mode setting
12	DCM	I	DCM threshold setting
13	ADELEF	I	Delay-time programming between primary-side and secondary-side switches, t_{AFSET} and t_{BESET}.
14	ADEL	I	Dead-time programming for the primary switches over CS voltage range, t_{ABSET} and t_{CDSET}.
15	CS	I	Current sense for cycle-by-cycle overcurrent protection and adaptive delay functions
16	SYNC	I/O	Synchronization out from master controller to input of slave controller
17	OUTF	O	0.2-A sink/source synchronous switching output
18	OUTE	O	0.2-A sink/source synchronous switching output
19	OUTD	O	0.2-A sink/source primary switching output
20	OUTC	O	0.2-A sink/source primary switching output
21	OUTB	O	0.2-A sink/source primary switching output
22	OUTA	O	0.2-A sink/source primary switching output
23	VDD	I	Bias supply input
24	GND		Ground. All signals are referenced to this node.

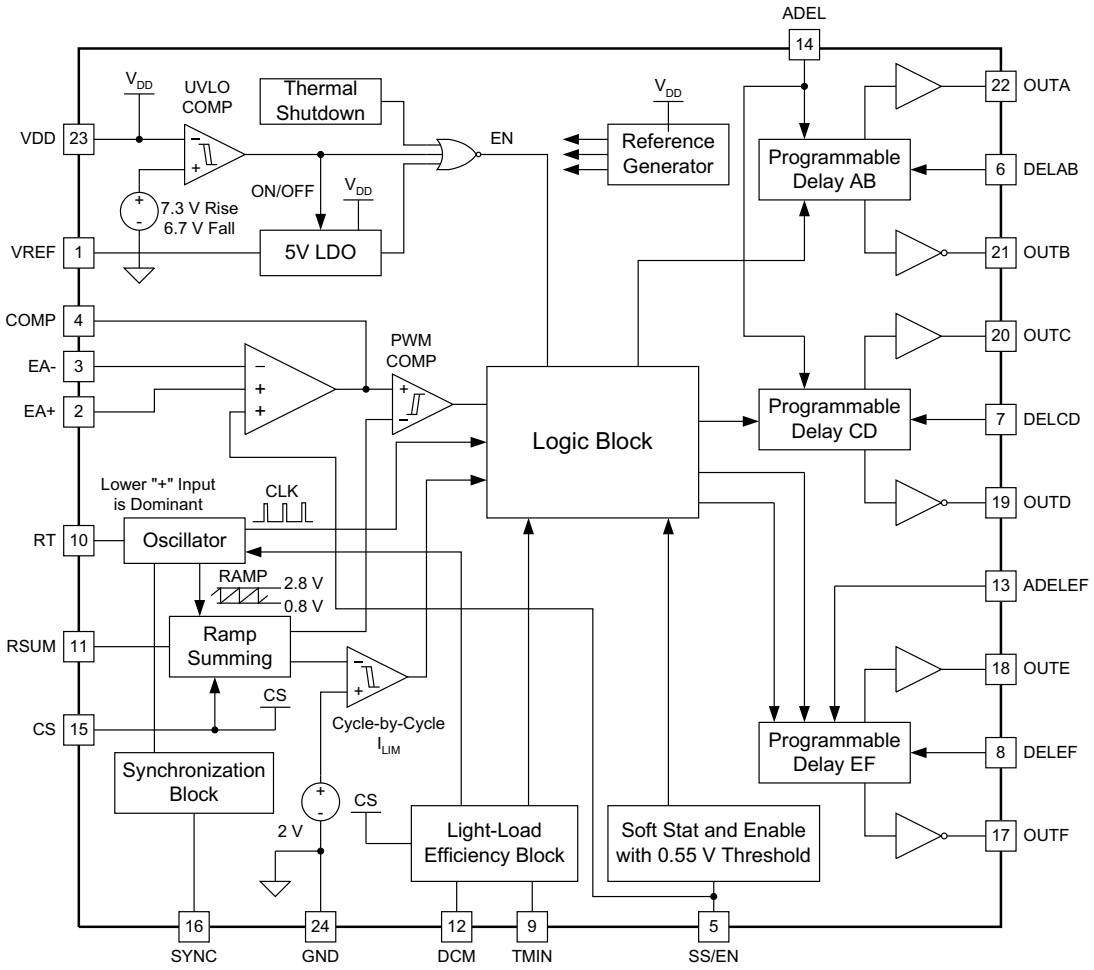


Figure 1. Functional Block Diagram

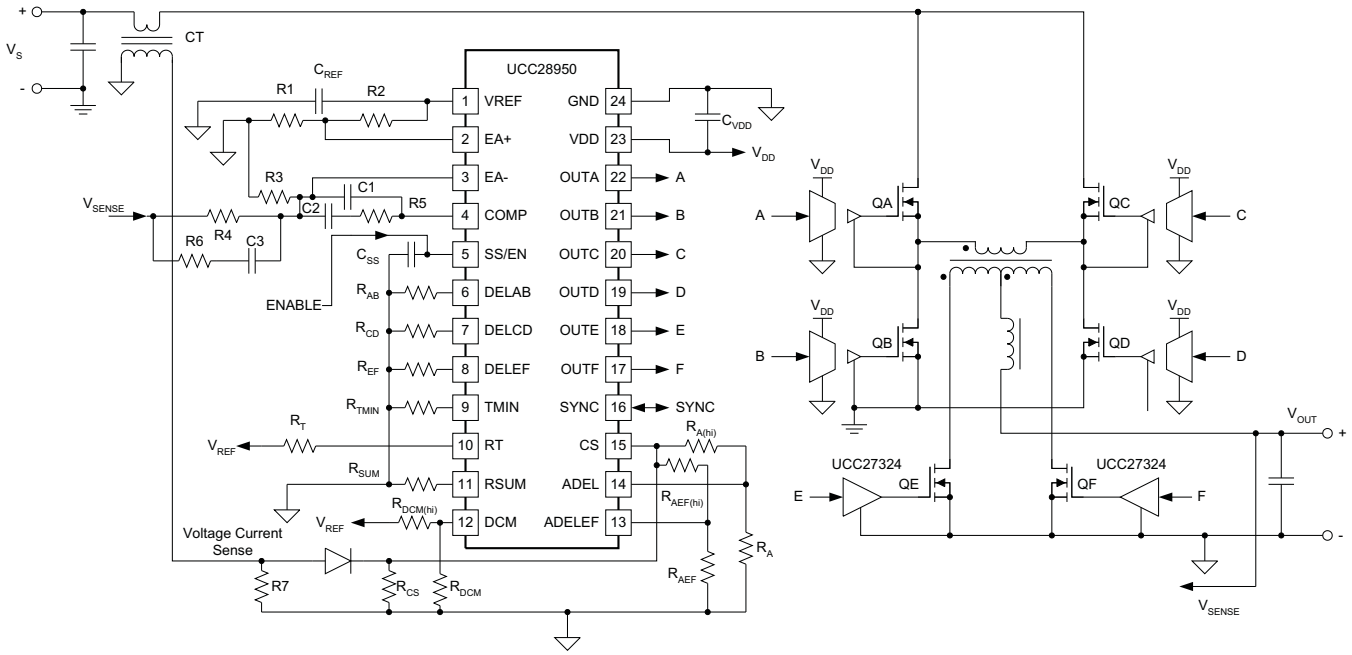


Figure 2. Typical Application Diagram

Start-Up Timing Diagram

No output delay shown, COMP-to-RAMP offset not included

Figure 3.

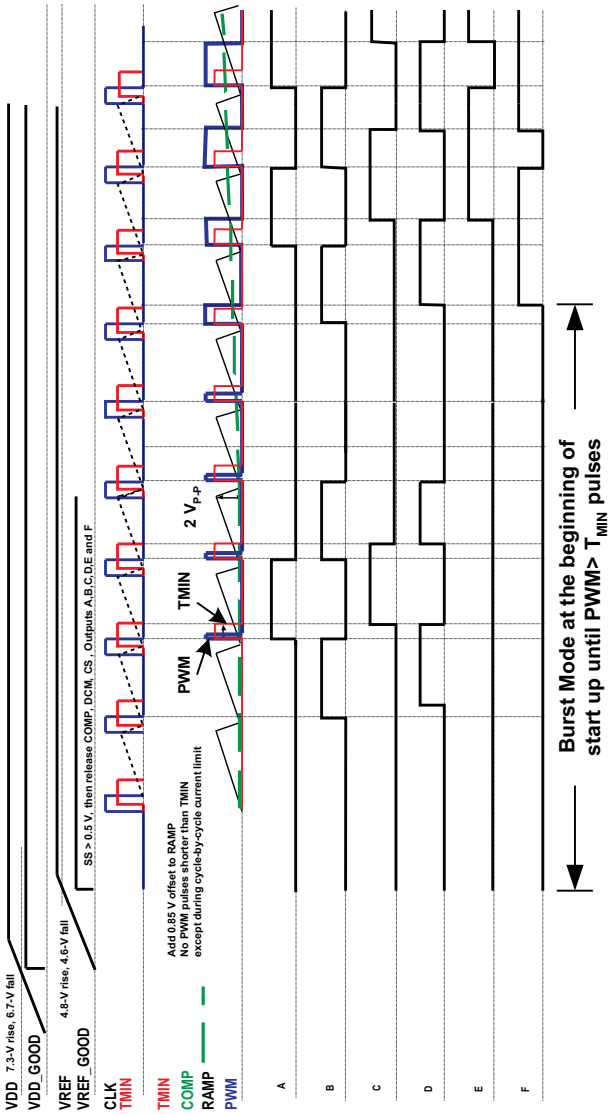


Figure 4. UCC28950-Q1 Timing Diagram

NOTE

There is no pulse on OUTE during burst mode at start-up. Enabling the synchronous rectifier outputs requires two preceding falling-edge PWM pulses.

Steady State/Shutdown Timing Diagram

No output delay shown, COMP-to-RAMP offset not included

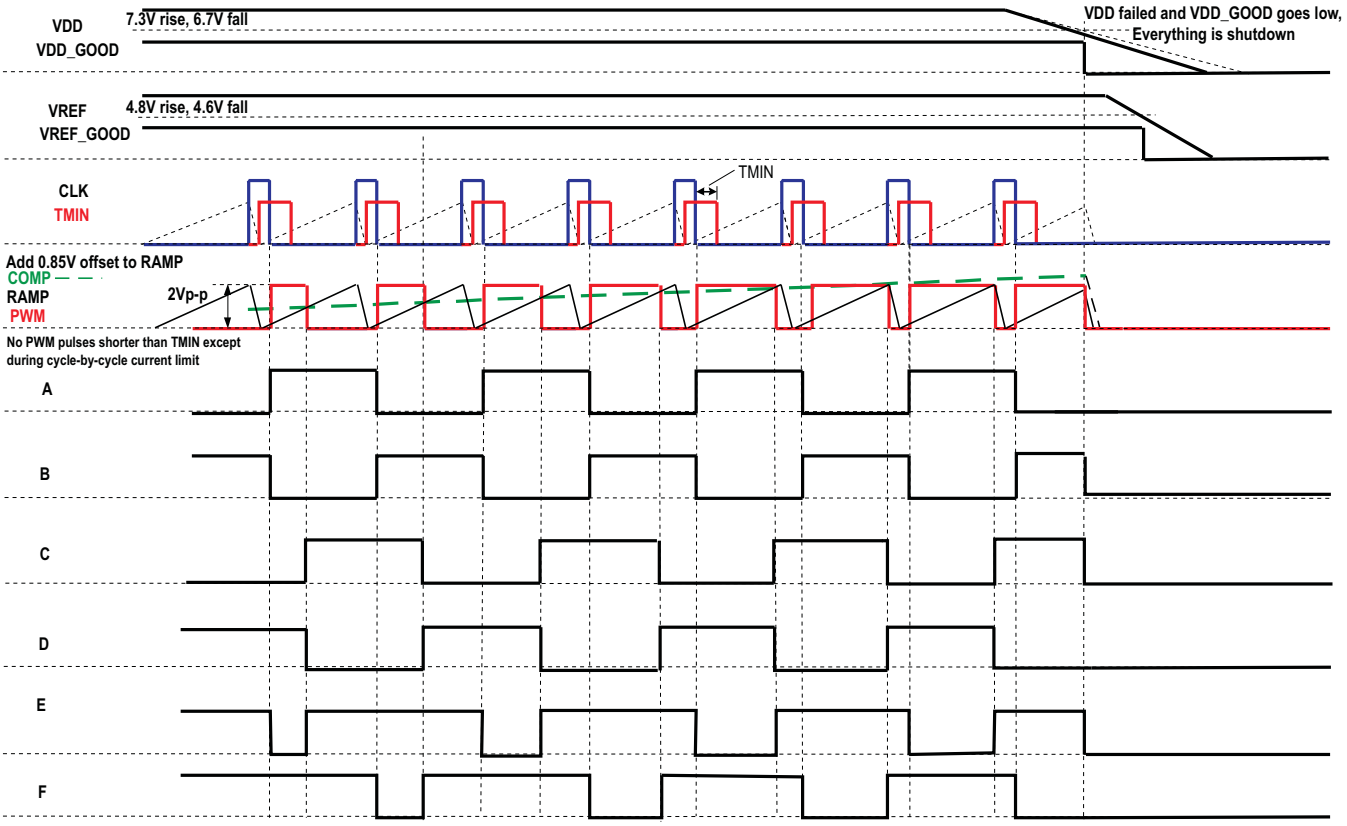


Figure 5. UCC28950-Q1 Timing Diagram

DETAILED PIN DESCRIPTION AND PARAMETER SETTINGS

Start-Up Protection Logic

Before the UCC28950-Q1 controller starts up, there is a requirement to meet the following conditions:

- VDD voltage exceeds rising UVLO threshold, 7.3 V typical.
- The 5-V reference voltage is available.
- Junction temperature is below the thermal shutdown threshold of 140°C.
- The voltage on the soft-start capacitor is not below 0.55 V typical.

Meeting all those conditions causes the generation of an internal enable signal EN that initiates the soft-start process. The voltage at the SS pin defines the duty cycle during the soft start, and cannot be lower than the duty cycle set by TMIN, or by the cycle-by-cycle current-limit circuit, depending on load conditions.

Voltage Reference (VREF)

The accurate (±1.5%) 5-V reference voltage regulator with the short-circuit protection circuit supplies internal circuitry and provides up to a 20-mA external output current for setting dc-dc converter parameters. Place a low-ESR and -ESL decoupling capacitor C_{REF} in the 1-µF to 2.2-µF range, preferably ceramic, from this pin to GND, as close to the related pins as possible for best performance. The only condition where the reference regulator is shut down internally is during undervoltage lockout.

Error Amplifier (EA+, EA–, COMP)

The error amplifier has two uncommitted inputs, EA+ and EA–, with a 3-MHz unity bandwidth, which allows flexibility in closing the feedback loop. EA+ is a non-inverting input, EA– is an inverting input, and COMP is the output of the error amplifier. The input-voltage common-mode range within which the parameters of the error amplifier are specified is from 0.5 V to 3.6 V. The output of the error amplifier connects internally to the non-inverting input of the PWM comparator. The range of the error-amplifier output of 0.25 V to 4.25 V far exceeds the PWM comparator input-ramp signal range, which is from 0.8 V to 2.8 V. The soft-start signal serves as an additional non-inverting input of the error amplifier. The lower of the two non-inverting inputs of the error amplifier is the dominant input and sets the duty cycle where the output signal of the error amplifier is compared with the internal ramp at the inputs of the PWM comparator.

Soft Start and Enable (SS/EN)

The soft-start pin SS/EN is a multi-function pin used for the following operations:

- Closed-loop soft start with the gradual duty-cycle increase from the minimum set by TMIN up to the steady-state duty cycle required by the regulated output voltage
- Setting hiccup-mode conditions during cycle-by-cycle overcurrent limit
- On/off control for the converter

During soft start, one of the voltages at the SS/EN or EA+ pins, whichever is lower (SS/EN – 0.55 V) or EA+ voltage (see the Block Diagram), sets the reference voltage for a closed feedback loop. Both SS/EN and EA+ signals are non-inverting inputs of the error amplifier, with the COMP pin being its output. Thus the soft start always goes under the closed feedback loop and the voltage at the COMP pin sets the duty cycle. The duty cycle defined by the COMP voltage cannot be shorter than the TMIN pulse set by the user. However, if the cycle-by-cycle current limit circuit sets the shortest duty cycle, then that duty cycle becomes dominant over the duty cycle defined by the COMP voltage or by the TMIN block.

An external capacitor C_{SS}, connected between SS/EN pin and ground, defines the soft-start duration and the internal charge current that has typical value of 25 µA. Pulling the soft-start pin externally below 0.55 V shuts down the controller. The release of the soft-start pin enables the controller to start, and if there is no current-limit condition, the duty cycle applied to the output inductor gradually increases until it reaches the steady-state duty cycle defined by the regulated output voltage of the converter. This happens when the voltage at the SS/EN pin reaches and then exceeds the voltage at the EA+ pin, V(SS/EN) ≥ VNI / 0.55 V. Thus, for the given soft-start time t_{SS}, Equation 1 or Equation 2 can define the C_{SS} value:

$$C_{SS(master)} = \frac{T_{SS} \times 25\,\mu A}{(VNI + 0.55)} \quad (1)$$

$$C_{SS(slave)} = \frac{T_{SS}}{825K \times Ln\left(\frac{20.6}{20.6 - VNI - 0.55}\right)} \quad (2)$$

For example, in Equation 1, if the user selects soft-start time T_{SS} to be 10 ms, and the VNI is 2.5 V, then the soft-start capacitor C_{SS} is equal to 82 nF.

NOTE

For a converter configured in slave mode, make sure to place an 825-kΩ resistor from the SS pin to ground.

Light-Load Power-Saving Mode

The UCD28950 offers four different light-load management techniques for improving the efficiency of a power converter over a wide load-current range.

1. Adaptive delay,
   (a) ADEL, which sets and optimizes the dead-time control for the primary switches over a wide load-current range.
   (b) ADELEF, which sets and optimizes the delay-time control between the primary-side switches and the secondary-side switches.
2. TMIN, sets the minimum duty cycle as long as the part is not in current-limit mode.
3. Dynamic synchronous rectifier on/off control in DCM mode, for increased efficiency at light loads. The DCM mode starts when the voltage at CS pin is lower than the threshold set by the user. In DCM mode, the device pulls the synchronous output drive signals OUTE and OUTF low.
4. Burst mode, for maximum efficiency at very light loads or no load. Burst mode has an even number of PWM TMIN pulses followed by off-time. The TMIN duration set by the user defines transition to the burst mode.

Adaptive Delay, (Delay between OUTA and OUTB, OUTC and OUTD (*DELAB, DELCD, ADEL*))

The resistor R_{AB} from the DELAB pin, DELAB to GND, along with the resistor divider R_{AHI} from the CS pin to the ADEL pin and R_A from the ADEL pin to GND sets the delay T_{ABSET} between one of outputs OUTA or OUTB going low and another output going high Figure 6.

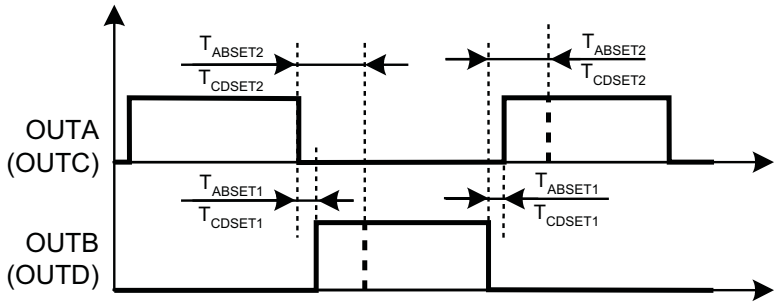


Figure 6. Delay Definitions Between OUTA and OUTB, OUTC and OUTD

This delay gradually increases as a function of the CS signal from T_{ABSET1}, which is measured at V_{CS} = 1.8 V, to T_{ABSET2}, which is measured at V_{CS} = 0.2 V. This approach ensures there is no shoot-through current during the high-side and low-side MOSFET switching and optimizes the delay for the ZVS condition over a wide load-current range. The resistor divider R_{AHI} and R_A determines the setting of the proportional ratio between longest and shortest. Tying the CS and ADEL pins together achieves the maximum ratio. Connecting ADEL to GND fixes the delay, which is then defined only by the resistor R_{AB} from DELAB to GND. The delay T_{CDSET1} and T_{CDSET2} settings and their behavior for outputs OUTC and OUTD are very similar to the one described for OUTA and OUTB. The difference is that resistor R_{CD} connected between the DELCD pin and GND sets the delay T_{CDSET}. Delays for outputs OUTC and OUTD share with the outputs OUTA and OUTB the same CS voltage-dependence pin ADEL.

The following Equation 3 defines the delay time T_{ABSET} .

$$T_{ABSET} = \left(\frac{5 \times R_{AB}}{0.15\,V + CS \times K_A \times 1.46} \right) ns + 5ns \quad (3)$$

The same equation defines the delay time T_{CDSET} in another leg, except R_{CD} replaces R_{AB}.

$$T_{CDSET} = \left(\frac{5 \times R_{CD}}{0.15\,V + CS \times K_A \times 1.46} \right) ns + 5ns \quad (4)$$

In these equations R_{AB} and R_{CD} are in kΩ and CS, the voltage at pin CS, is in volts, and K_A is a numerical coefficient in the range from 0 to 1. The delay time T_{ABSET} and T_{CDSET} are in ns. These equations are empirical approximations derived from measured data. Thus, there is no unit agreement in the equations. As an example, assume R_{AB} = 15 kΩ, CS = 1 V and K_A = 0.5. Then T_{ABSET} is 90.25 ns. In both Equation 3 and Equation 4, K_A is the same, defined as:

$$K_A = \frac{R_A}{R_A + R_{AHI}} \quad (5)$$

K_A sets how the delay is sensitive to CS voltage variation. If K_A = 0 (ADEL shorted to GND), the delay is fixed. If K_A = 1 (ADEL is tied to CS), the delay is maximum at CS = 0.2 V and gradually decreases when CS goes up to 1.8 V. The ratio between the maximum and minimum delay can be up to 6:1.

TI recommends to start by setting K_A = 0 and setting T_{ABSET} and T_{CDSET} relatively large, using equations or plots in the data sheet to avoid hard switching or even shoot-through current. Accordingly, resistors R_{AB} and R_{CS} set the delay between outputs A, B and C, D. Program the optimal delays at light load first. Then by changing K_A, set the optimal delay for the outputs A, B at maximum current. K_A for outputs C, D is the same as for A,D. Usually outputs C and D have ZVS if sufficient delay is provided.

NOTE

The allowed resistor range on DELAB and DELCD, R_{AB} and R_{CD} is 13 kΩ to 90 kΩ.

R_A and R_{AHI} define the portion of voltage at pin CS applied to the pin ADEL (See the Typical Application Diagram, Figure 2). K_A defines how significantly the delay time depends on CS voltage. K_A varies from 0, where ADEL pin is shorted to ground (R_A = 0) and the delay does not depend on CS voltage, to 1, where ADEL ties to CS (R_{AH} = 0). Setting K_A, R_{AB}, and R_{CD} provides the ability to maintain optimal ZVS conditions of primary switches over load current, because the voltage at CS pin includes reflected load current to the primary side through the current-sensing circuit. The plots in Figure 7 and Figure 8 show the delay-time settings as a function of the CS voltage and K_A for two different conditions: R_{AB} = R_{CD} = 13 kΩ (Figure 7) and R_{AB} = R_{CD} = 90 kΩ (Figure 8).

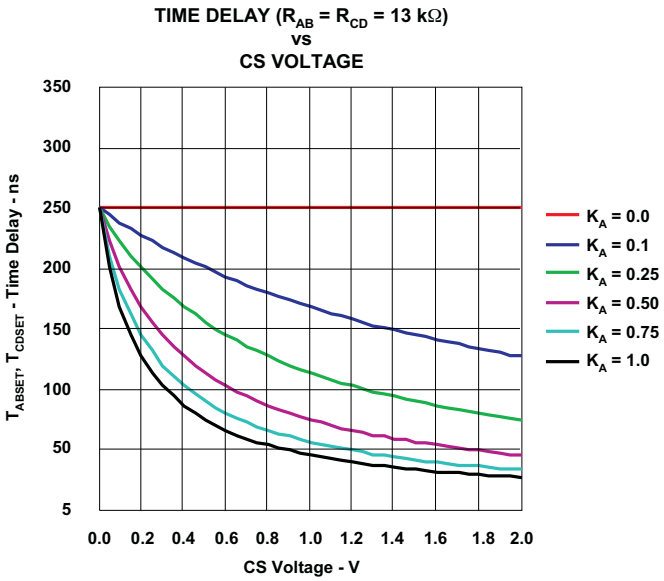


Figure 7. Delay-Time Set t_{ABSET} and t_{CDSET} (Over CS Voltage Variation and Selected K_A for R_{AB} and R_{CD} Equal 13 kΩ)

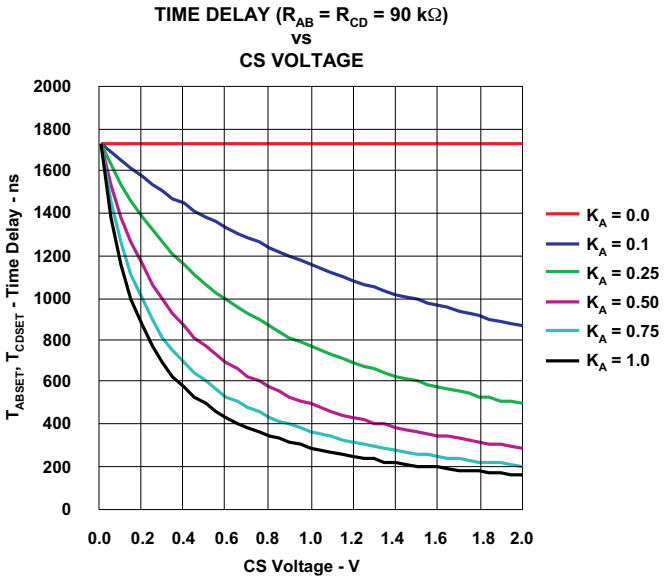


Figure 8. Delay-Time Set t_{ABSET} and t_{CDSET} (Over CS Voltage Variation and Selected K_A for R_{AB} and R_{CD} Equal 90 kΩ)

Adaptive Delay (Delay Between OUTA and OUTF, OUTB and OUTE (*DELEF, ADELEF*))

Resistor R_{EF} from the DELEF pin to GND along with resistor divider R_{AEFHI} from the CS pin to the ADELEF pin and R_{AEF} from the ADELEF pin to GND sets equal delays t_{AFSET} and t_{BESET} between outputs OUTA or OUTB going low and related output OUTF or OUTE going low Figure 9.

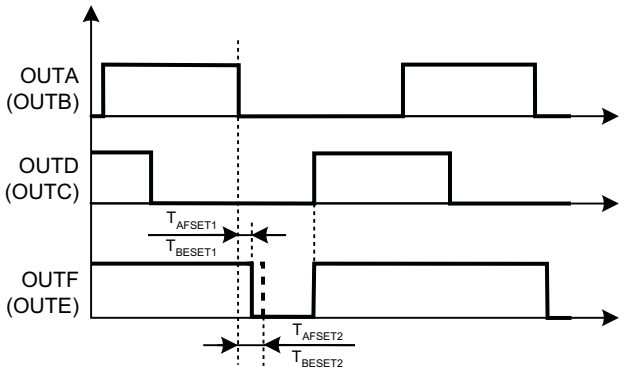


Figure 9. Delay Definitions Between OUTA and OUTF, OUTB and OUTE

These delays gradually increase as a function of the CS signal from t_{AFSET1}, measured at V_{CS} = 0.2 V, to T_{AFSET2}, measured at V_{CS} = 1.8 V. Opposite to the DELAB and DELCD behavior, this delay is longest (T_{AFSET2}) when the signal at CS pin is maximum and shortest (T_{AFSET1}) when the CS signal is minimmum. This approach reduces the synchronous-rectifier MOSFET body-diode conduction time over a wide load-current range, thus improving efficiency and reducing diode recovery time. The resistor divider R_{AEFHI} and R_{AEF}, determines the setting of the proportional ratio between the longest and shortest delay. If CS and ADELEF are shorted, the ratio is maximized. Connecting ADELEF to GND fixes the delay, defined only by resistor R_{EF} from DELEF to GND.

Equation 6 defines delay time t_{AFSET}. The same Figure 1 defines the delay time t_{BESET}.

$$T_{AFSET} = \left(\left(\frac{5 \times R_{EF}}{2.65\,V - CS \times K_{EF} \times 1.32} \right) ns + 4\,ns \right) \tag{6}$$

In this equation R_{EF} is in kΩ, CS, which is the voltage at pin CS, is in volts and K_{EF} is a numerical gain factor of CS voltage from 0 to 1. Delay time t_{AFSET} is in ns. This equation is an empirical approximation of measured data, thus, there is no unit agreement in it. As an example calculation, assume R_{EF} = 15 kΩ, CS = 1 V and K_{EF} = 0.5. Then t_{AFSET} is 41.7 ns. The definition of K_{EF} is:

$$K_{EF} = \frac{R_{AEF}}{R_{AEF} + R_{AEF(hi)}} \tag{7}$$

R_{AEF} and R_{AEFHI} define the portion of the voltage at pin CS applied to pin ADELEF (See the Typical Application Diagram). K_{EF} defines how significantly the delay time depends on the CS voltage. K_{EF} varies from 0, with the ADELEF pin shorted to ground (R_{AEF} = 0) and the delay independent of the CS voltage, to 1, with ADELEF tied to CS (R_{AEFHI} = 0).

NOTE

The allowed resistor range on DELEF, R_{EF} is 13 kΩ to 90 kΩ.

The plots in Figure 10 and Figure 11 show delay time settings as function of the CS voltage and K_{EF} for two different conditions: R_{EF} = 13 kΩ (Figure 10) and R_{EF} = 90 kΩ (Figure 11)

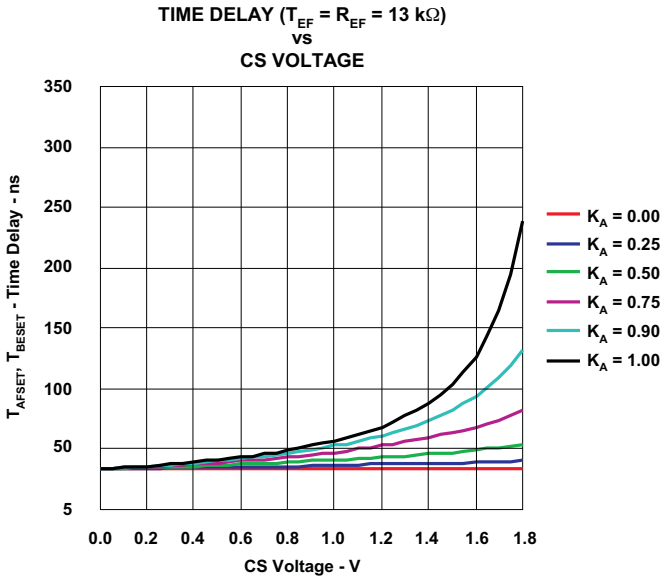


Figure 10. Delay Time t_{AFSET} and t_{BESET} (Over CS Voltage and Selected K_{EF} for R_{EF} Equal 13 kΩ)

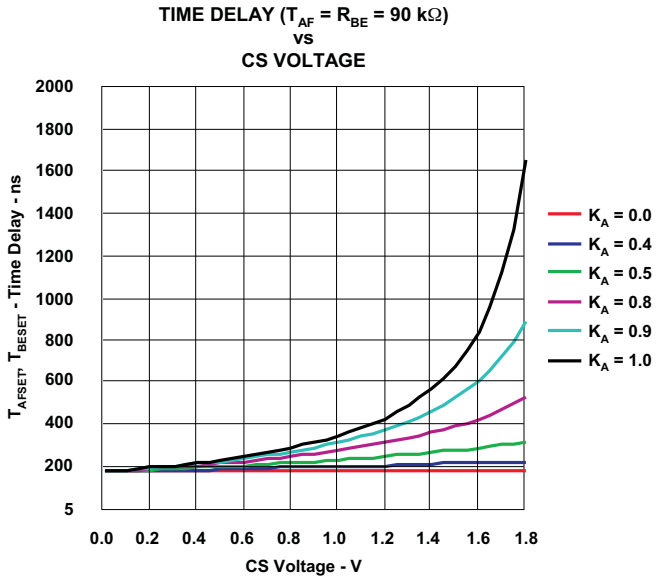


Figure 11. Delay Time t_{AFSET} and t_{BESET} (Over CS Voltage and Selected K_{EF} for R_{EF} Equal 90 kΩ)

Minimum Pulse (TMIN)

Resistor R_{TMIN} from the TMIN pin to GND sets the fixed minimum pulse, TMIN, applied to the output rectifier, enabling ZVS of the primary switches at light load. If the output PWM pulse demanded by the feedback loop is shorter than TMIN, then the controller proceeds to the burst mode of operation, where the off-time dictated by the feedback loop follows an even number of TMIN pulses. The time it takes to raise the sufficient magnetizing current in the power transformer to maintain ZVS dictates the proper selection of TMIN. Equation 8 defines the minimum pulse TMIN.

$$TMIN = \left(5.92 \times R_{TMIN}\right) ns \tag{8}$$

In this equation, R_{TMIN} is in kΩ and TMIN is in ns.

NOTE

The minimum allowed resistor on TMIN, R_{TMIN} is 13 kΩ.

The related plot is Figure 12.

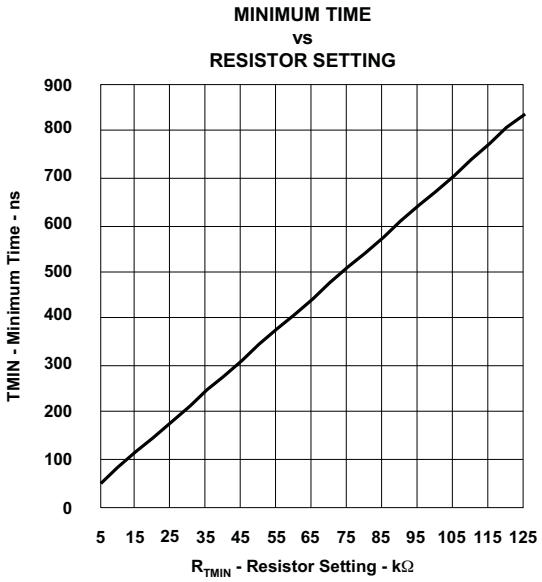


Figure 12. Minimum Time TMIN Over Setting Resistor R_{TMIN}

Equation 9 determines the value of minimum duty cycle DMIN.

$$DMIN = \left(TMIN \times F_{SW(osc)} \times 10^{-4}\right)\% \tag{9}$$

Here, $f_{SW(osc)}$ is oscillator frequency in kHz, TMIN is the minimum pulse in ns, and DMIN is in percent.

Burst Mode

If the converter is commanding a duty cycle lower than TMIN, then the controller goes into burst mode. The controller always delivers an even number of power cycles to the power transformer. The controller always stops its bursts with the OUTB and OUTC power-delivery cycle. If the controller still demands a duty cycle less than TMIN, then the controller goes into shutdown mode. Then it waits until the converter demands a duty cycle equal or higher than TMIN before the controller puts out TMIN or a PWM duty cycle as dictated by the COMP voltage pin.

Switching Frequency Setting (RT)

Connecting an external resistor R_T between the RT and VREF pins sets the fixed-frequency operation and configures the controller as a master providing synchronization output pulses at the SYNC pin with 0.5 duty cycle and frequency equal to the internal oscillator. To set the converter in slave mode, connect the external resistor R_T between the RT pin and GND, and place an 825-kΩ resistor from the SS pin to GND in parallel to the SS_EN capacitor. This configures the controller as a slave. The slave controller operates with 90° phase shift relatively to the master converter if their SYNC pins are tied together. The switching frequency of the converter is equal to the frequency of output pulses. The following Equation 10 defines the nominal switching frequency of the converter configured as a master (resistor R_T between the RT pin and V_{REF}). On the UCC28950-Q1 there is an internal clock oscillator frequency which is twice that of the controller output frequency.

$$F_{SW(nom)} = \left(\frac{2.5 \times 10^3}{\left(\frac{RT}{V_{REF} - 2.5\,V} + 1 \times \frac{k\Omega}{V} \right)} \right) kHz \quad (10)$$

In this equation, R_T is in kΩ, VREF is in volts, and $f_{SW(nom)}$ is in kHz. This is also an empirical approximation, and thus there is no unit agreement. Assume, for example, VREF = 5 V, R_T = 65 kΩ. Then the switching frequency $f_{SW(nom)}$ is 92.6 kHz.

Equation 11 defines the nominal switching frequency of the converter with the converter configured as a slave and resistor R_T connected between the RT pin and GND.

$$F_{SW(nom)} = \left(\frac{2.5 \times 10^3}{\left(\frac{RT}{2.5\,V} + 1 \times \frac{k\Omega}{V} \right)} \right) kHz \quad (11)$$

In this equation, RT is in kΩ and f is in kHz. Notice that for VREF = 5 V, Equation 10 and Equation 11 yield the same results.

The plot in Figure 13 shows how $f_{SW(nom)}$ depends on the resistor R_T value when the VREF = 5 V. As it is seen from Equation 10 and Equation 11, the switching frequency $f_{SW(nom)}$ setting is for the same value for either master or slave configuration, provided the same resistor value R_T is used.

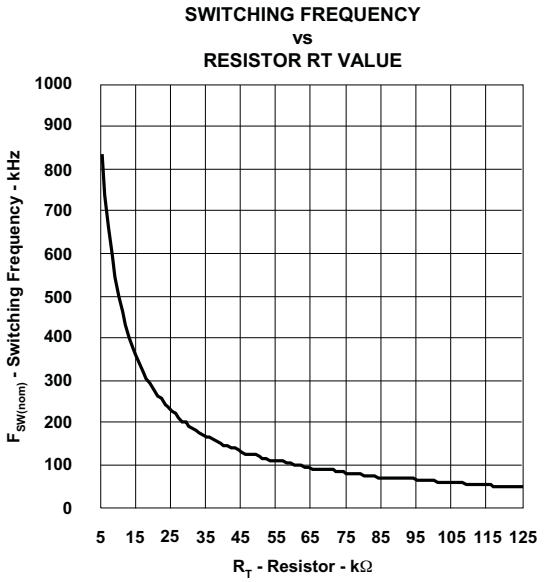


Figure 13. Converter Switching Frequency $f_{SW(nom)}$ Over Resistor RT Value

Slope Compensation (RSUM)

Slope compensation is the technique that adds additional ramp signal to the CS signal and applies to the:

- Input of PWM comparator in case of peak current mode control
- Input of cycle-by-cycle current limit comparator

This prevents sub-harmonic oscillation at D > 50% (some publications suggest it might happen even at D < 50%). At low duty cycle and light load, the slope-compensation ramp reduces the noise sensitivity of peak-current-mode control.

Too much additional slope-compensation ramp reduces benefits of PCM control. In the case of cycle-by-cycle current limit, the average current limit becomes lower, and this might reduce the start-up capability with large output capacitance. The optimal compensation slope varies depending on duty cycle, L_O and L_M.

The controller operating in peak-current-mode control or during the cycle-by-cycle current limit at duty cycle above 50% requires slope compensation. Placing a resistor from the RSUM pin to ground allows the controller to operate in peak-current-control mode. Connecting the RSUM pin through a resistor to VREF switches the controller to voltage-mode control with the internal PWM ramp. However, the resistor value still provides CS signal compensation for cycle-by-cycle current limit. In other words, in VMC, slope compensation is applied only to the cycle-by-cycle comparator. While in PCM, the slope compensation applies to both the PWM and cycle-by-cycle current-limit comparators.

Figure 14 shows the operational logic of the slope-compensation circuit.

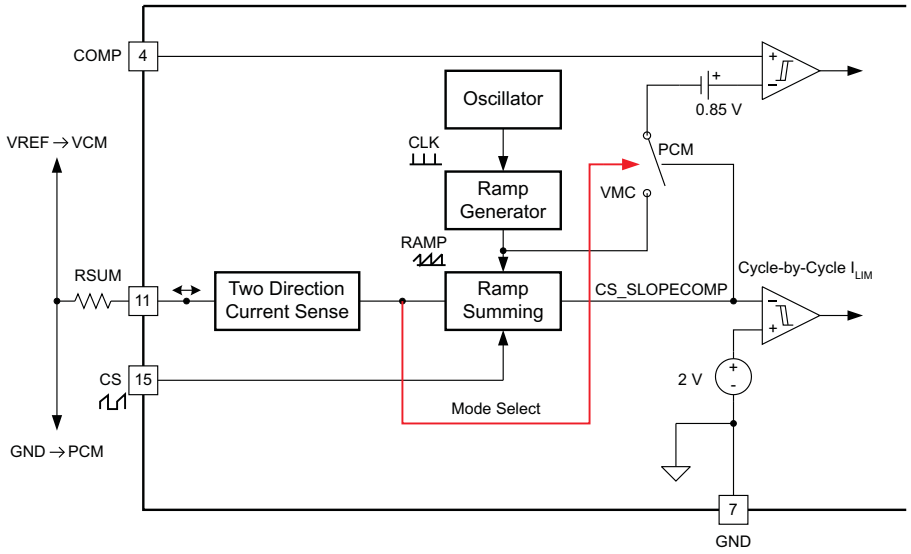


Figure 14. Operational Logic of Slope-Compensation Circuit

Equation 12 defines the slope of the additional ramp, me, added to CS signal by placing a resistor from the RSUM pin to ground.

$$me = \left(\frac{2.5}{0.5 \times R_{SUM}} \right) \frac{V}{\mu s} \tag{12}$$

If the resistor from the RSUM pin connects to the VREF pin, then the controller operates in voltage mode control, still having the slope compensation added to CS signal used for the cycle-by-cycle current limit. In such a case, Equation 13 defines the slope.

$$me = \left(\frac{(V_{REF} - 2.5\,V)}{0.5 \times R_{SUM}} \right) \frac{V}{\mu s} \tag{13}$$

In Equation 12 and Equation 13, the VREF is in volts, RSUM is in kΩ, and me is in V/µs. These are empirical equations without unit agreement. As an example, substituting VREF = 5 V and RSUM = 40 kΩ yields the result 0.125 V/µs. Figure 15 shows the related plot of me as function of RSUM. Because VREF = 5 V, the plots generated from Equation 12 and Equation 13 coincide.

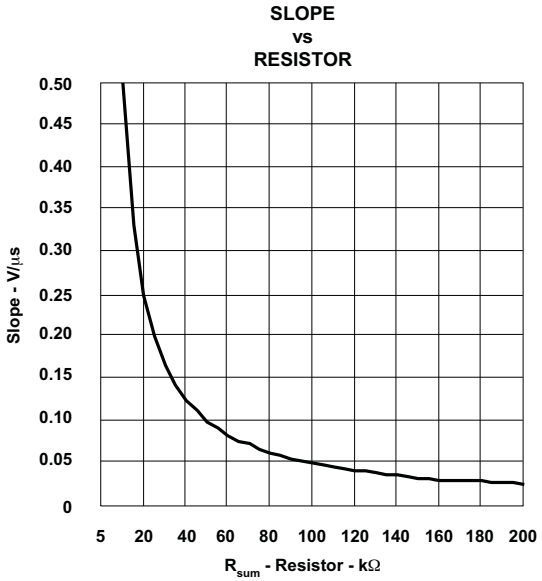


Figure 15. Slope of the Added Ramp Over Resistor RSUM

NOTE

The recommended resistor range for R_{SUM} is 10 kΩ to 1 MΩ.

Dynamic SR ON/OFF Control (DCM Mode)

The voltage at the DCM pin provided by the resistor divider Rdcmhi between the VREF pin and DCM, and Rdcm from the DCM pin to GND, sets the percentage of the 2-V current-limit threshold for the current-sense pin, (CS). If the CS pin voltage falls below the DCM pin threshold voltage, then the controller initiates the light-load power-saving mode, and shuts down the synchronous rectifiers, OUTE and OUTF. If the CS pin voltage is higher than the DCM pin threshold voltage, then the controller runs in CCM mode. Connecting the DCM pin to VREF makes the controller run in DCM mode and shuts off both outputs OUTE and OUTF. Shorting the DCM pin to GND disables the DCM feature, and the controller runs in CCM mode under all conditions.

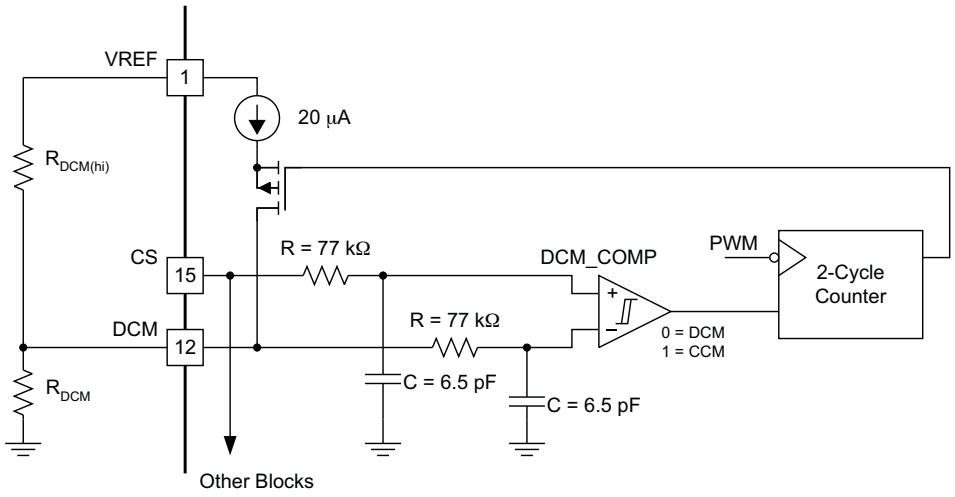


Figure 16. DCM Functional Block

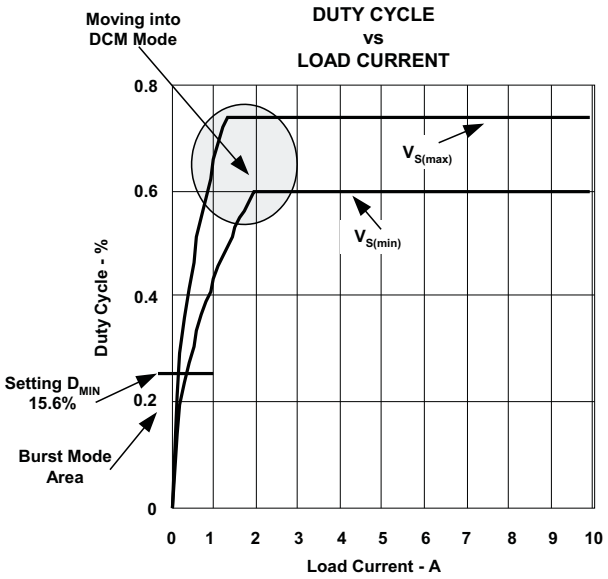


Figure 17. Duty-Cycle Change Over Load-Current Change

There is a nominal 20-µA switched current source used to create hysteresis. The current source is active only when the system is in DCM Mode. Otherwise, the curent source is inactive and does not affect the node voltage. Therefore, when in the DCM region, the DCM threshold is the voltage divider plus ΔV as explained in Equation 14. When in the CCM region, the threshold is the voltage set by the resistor divider. When the CS pin reaches the threshold set on the DCM pin, the system waits to see two consecutive falling-edge PWM cycles before switching from CCM to DCM and from DCM to CCM. The magnitude of the hysteresis is a function of the external resistor-divider impedance. Calculate the hysteresis using Equation 14:

$$\Delta V = 2 \times 10^{-5} \frac{R_{DCMHI} \times R_{DCM}}{R_{DCMHI} + R_{DCM}} \quad (14)$$

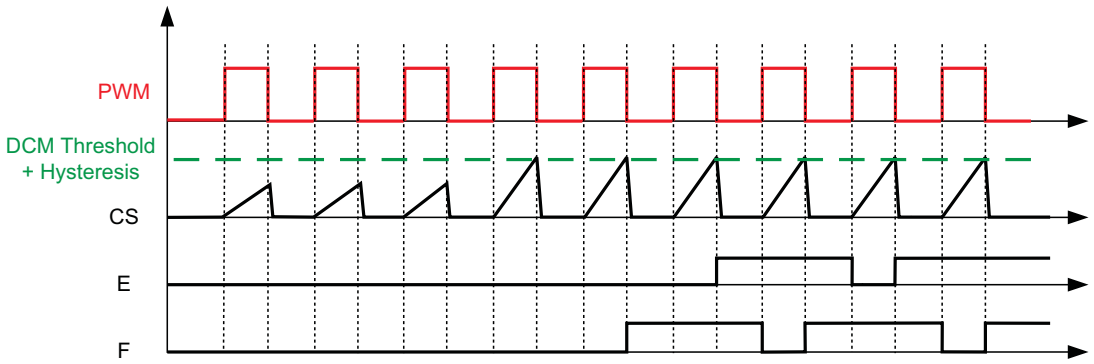


Figure 18. Moving From DCM to CCM Mode

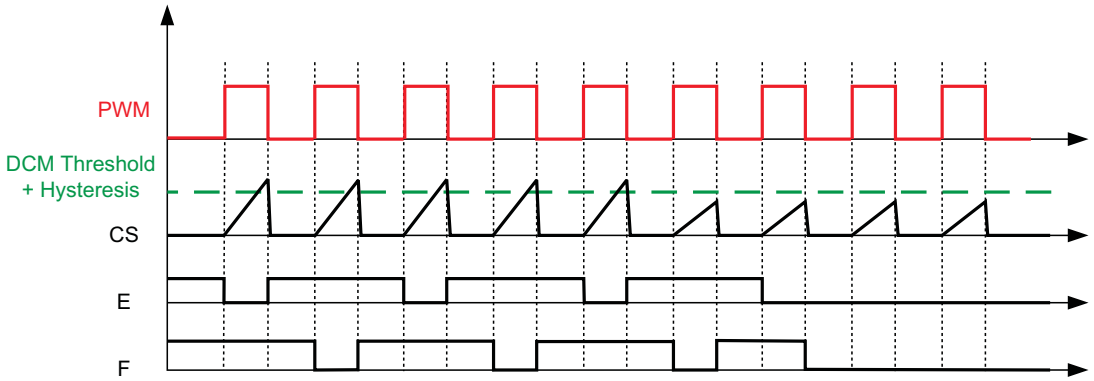


Figure 19. Moving From CCM to DCM Mode

Use DCM in order to prevent reverse current in the output inductor, which could cause the synchronous FETs to fail.

Current Sensing (CS)

Use of the signal from the current-sense pin is for cycle-by-cycle current limit, peak-current mode control, light-load efficiency management and setting the delay time for outputs OUTA, OUTB, OUTC, OUTD and delay time for outputs OUTE, OUTF. Connect the current-sense resistor R_{CS} between CS and GND. Depending on layout, to prevent a potential electrical noise interference, TI recommends putting a small R-C filter between the R_{CS} resistor and CS pin.

Cycle-by-Cycle Current-Limit Current Protection and Hiccup Mode

The cycle-by-cycle current limit provides peak current limiting on the primary side of the converter when the load current exceeds its predetermined threshold. For peak-current-mode control, prevention of the controller from false tripping due to switching noise requires a certain leading-edge blanking time. In order to save the external RC filter for the blanking time, the device has an internal 30-ns filter at the CS input. The total propagation delay, t_{CS}, from the CS pin to the outputs is 100 ns. circuit still requires an external RC filter if the power stage requires more blanking time. The 2-V, ±3% cycle-by-cycle current-limit threshold is optimal for efficient current-transformer-based sensing. The duration of converter operation in cycle-by-cycle current limiting depends on the value of soft-start capacitor and how severe the overcurrent condition is. Efficient sensing is achieved by the internal discharge current I_{DS} Equation 15 and Equation 16 at SS pin.

$$I_{DS(master)} = \left(-25 \times \left(1 - D\right) + 5\right)\mu A \tag{15}$$

$$I_{DS(slave)} = \left(-25 \times \left(1 - D\right)\right)\mu A \tag{16}$$

The soft-start capacitor value also determines the so-called hiccup mode off-time duration. Figure 20 shows the behavior of the converter during different modes of operation, along with related soft-start capacitor charge and discharge currents.

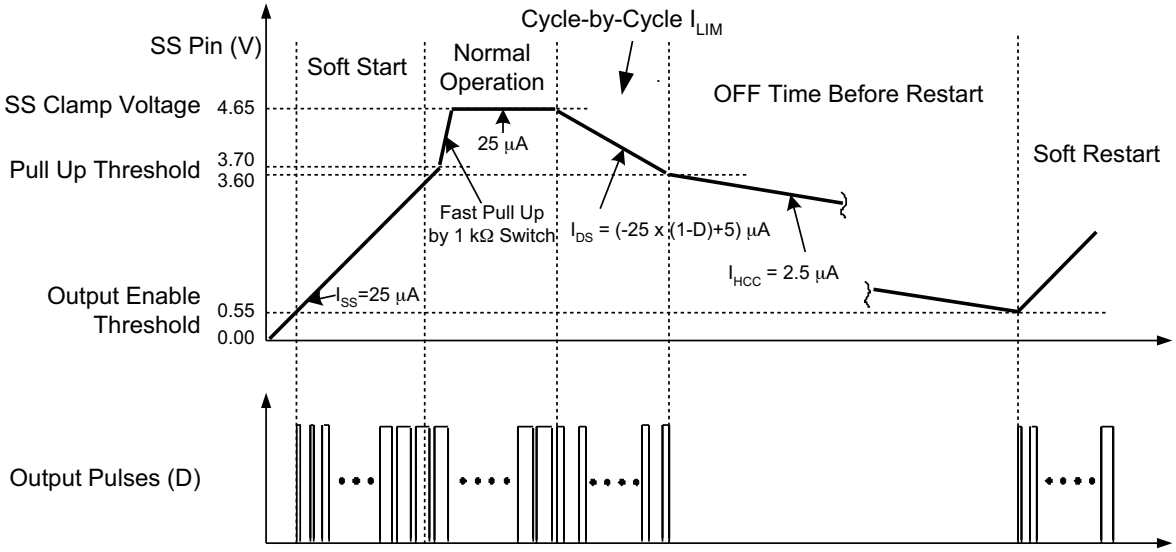


Figure 20. Timing Diagram of Soft-Start Voltage V_{SS}

The largest discharge current of 20 µA is when the duty cycle is close to zero. This current sets the shortest operation time during the cycle-by-cycle current limit, defined as:

$$T_{CL(on\_master)} = \frac{C_{SS} \times (4.65\,V - 3.7\,V)}{20\,\mu A} \quad (17)$$

$$T_{CL(on\_slave)} = \frac{C_{SS} \times (4.65\,V - 3.7\,V)}{25\,\mu A} \quad (18)$$

Thus, if soft-start capacitor C_{SS} = 100 nF is selected, then the $t_{CL(on)}$ time is 5 ms.

To calculate the hiccup off-time $t_{CL(off)}$ before the restart, use Equation 19 or Equation 20 :

$$T_{CL(off\_master)} = \frac{C_{SS} \times (3.6\,V - 0.55\,V)}{2.5\,\mu A} \quad (19)$$

$$T_{CL(off\_slave)} = \frac{C_{SS} \times (3.6\,V - 0.55\,V)}{4.9\,\mu A} \quad (20)$$

With the same soft-start capacitor value of 100 nF, the off-time before the restart is 122 ms. Notice that if the overcurrent condition happens before the soft-start capacitor voltage reaches the 3.7-V threshold during start-up, the controller limits the current, but the soft-start capacitor continues to be charged. Immediately on reaching the 3.7-V threshold, an internal 1-kΩ $r_{DS(on)}$ switch quicly pulls the soft-start voltage up to the 4.65-V threshold, and the cycle-by-cycle current-limit-duration timing starts by discharging the soft-start capacitor. Depending on specific design requirements, the user can override default parameters by applying external charge or discharge currents to the soft-start capacitor. Figure 20 shows the whole cycle-by-cycle current-limit and hiccup operation. In this example, the cycle-by-cycle current limit lasts about 5 ms followed by 122 ms of off-time.

Similar to the overcurrent condition, the user can override the hiccup mode with restart by connecting a pullup resistor between the SS and VREF pins. If the pullup current provided by the resistor exceeds 2.5 µA, then the controller remains in the latch-off mode. In this case, calculate the value of an external soft-start capacitor with the additional pullup current taken into account. One can reset the latch-off mode externally by forcibly discharging the soft-start capacitor below 0.55 V or lowering the V_{DD} voltage below the UVLO threshold.

Synchronization (SYNC)

The UCC28950-Q1 allows flexible configuration of converters operating in synchronized mode by connecting all SYNC pins together and by configuration of the controllers as master and/or slaves. The controller configured as master (resistor between RT and VREF) provides synchronization pulses at the SYNC pin with the frequency equal to 2× the converter frequency $f_{SW(nom)}$ and 0.5 duty cycle. The controller configured as a slave (resistor between RT and GND and an 825-kΩ resistor from the SS_EN pin to GND) does not generate the synchronization pulses. The slave controller synchronizes its own clock to the falling edge of the synchronization signal, thus operating 90° phase-shifted versus the master converter frequency $f_{SW(nom)}$. Because the slave is synchronized to the falling edge of the SYNC pulses, the slave operates at 180° delayed versus the CLK of the master CLK or 90° delayed versus output-switching pulses of the master.

Such operation between master and slave provides the maximum input-capacitor and output-capacitor ripple-cancellation effect by tying the inputs and outputs of the converters together. To avoid system issues during the synchronized operation of a few converters, take care of the following conditions.

- For any slave-configured converter, the SYNC frequency must be greater than or equal to 1.8 times the converter frequency.
- A slave converter does not start until it has received at least one synchronization pulse.
- For any converters are configured as slaves, then each converter operates at its own frequency without synchronization after receiving at least one synchronization pulse. Thus, If there is an interruption of synchronization pulses at the slave converter, then the controller uses its own internal clock pulses to maintain operation based on the R_T value connected to GND in the slave converter.
- In master mode, SYNC pulses start after the SS pin passes its enable threshold, which is 0.55 V.
- A slave starts generating SS/EN voltage even without having received synchronization pulses.
- RI recommends that the SS on the master controller start before the SS on the slave controller; therefore, for proper operation, the SS/EN pin on the master converter must reach its enable threshold voltage before SS/EN on the slave converter starts. On the same note, TI recommends that the t_{MIN} resistors on both master and slave be set at the same value.

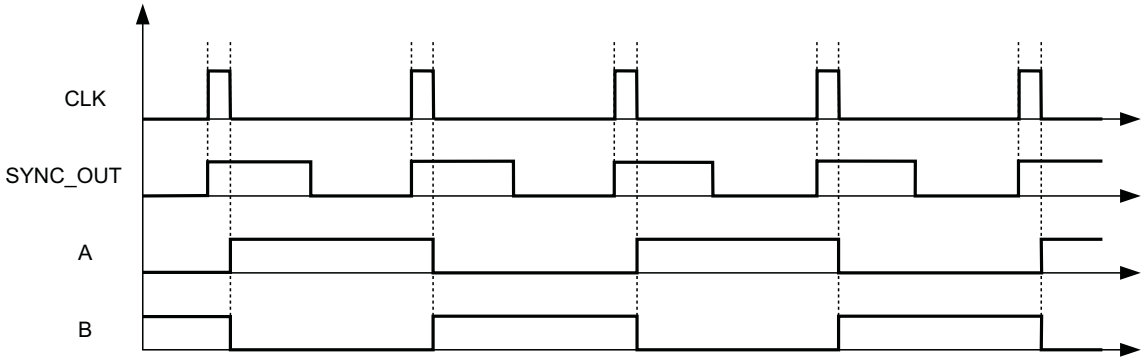


Figure 21. SYNC_OUT (Master Mode) Timing Diagram

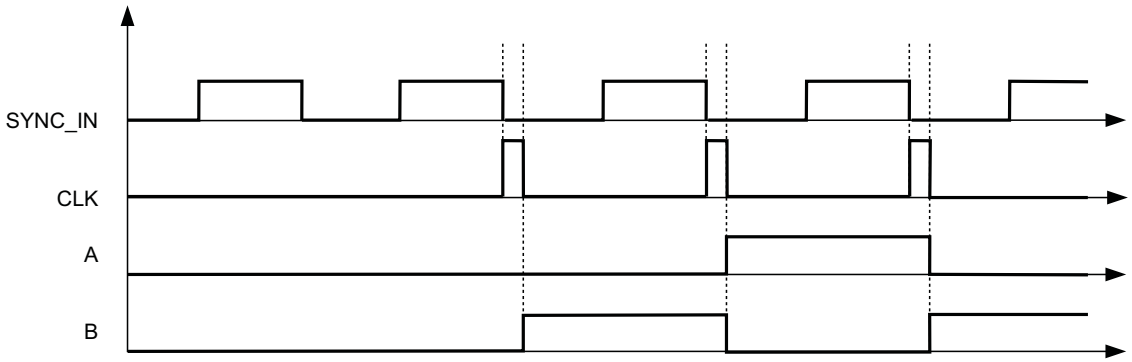


Figure 22. SYNC_IN (Slave Mode) Timing Diagram

Outputs (OUTA, OUTB, OUTC, OUTD, OUTE, OUTF)

- All MOSFET control outputs have 0.2-A drive capability.
- The control outputs are configured as P-MOS and N-MOS totem poles with typical $r_{DS(on)}$ of 20 Ω and 10 Ω, respectively.
- The control outputs are capable of charging 100-pF capacitor within 12 ns and discharging within 8 ns.
- The amplitude of the output control pulses is equal to V_{DD}.
- Design of the control outputs is for use with external-gate MOSFET/IGBT drivers.
- Design optimization prevents the latch-up of outputs, which extensive tests have verified.

The UCC28950-Q1 has outputs OUTA and OUTB driving the active leg, initiating the duty-cycle leg of the power MOSFETs in the phase-shifted full-bridge power stage, and outputs OUTC and OUTD driving the passive leg, completing the duty cycle leg, as the typical timing diagram in Figure 50 shows. Optimization of outputs OUTE and OUTF is for driving the synchronous rectifier MOSFETs (Figure 23). These outputs, designed to drive relatively small capacitive loads like inputs of external MOSFET or IGBT drivers, have 200-mA peak-current capabilities. Recommended load capacitance should not exceed 100 pF. The amplitude of output signal is equal to the V_{DD} voltage.

The capacitors C_{OSS} shown in Figure 23 are internal MOSFET capacitances that must be taken into account during the design procedure to estimate the zero-voltage condition and switching losses.

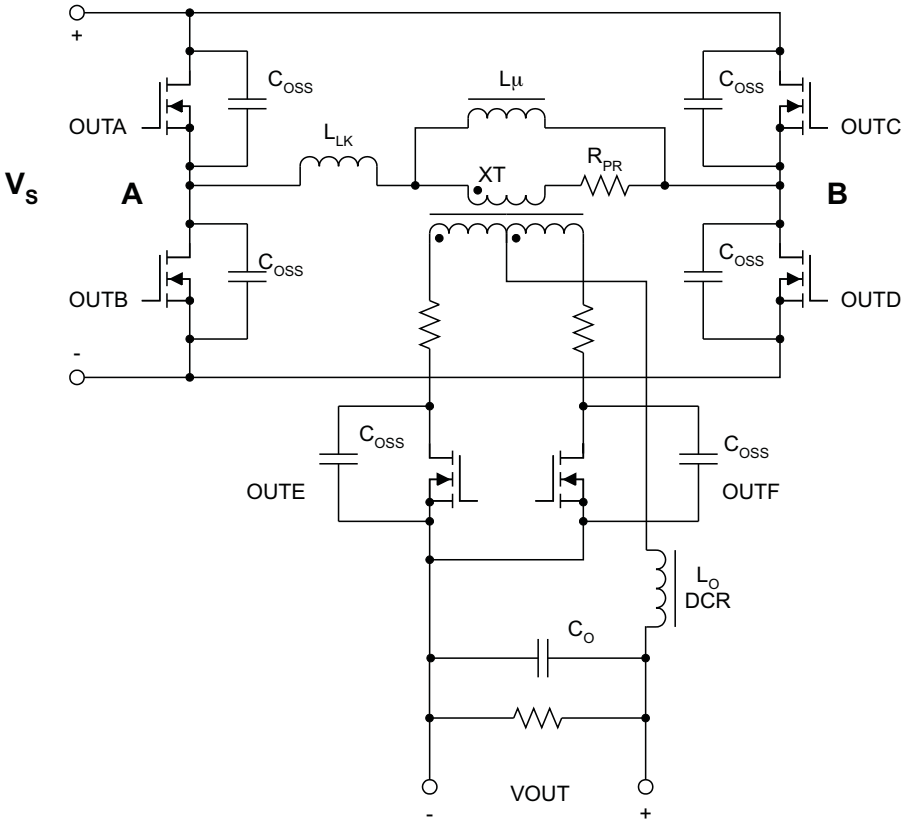


Figure 23. Power Stage

Supply Voltage (VDD)

Connect this pin to a bias supply in the 8-V to 17-V range. Place high quality, low-ESR and -ESL, ceramic bypass capacitor C_{VDD} of at least 1-µF, from this pin to GND. TI recommends using a 10-Ω resistor in series with the VDD pin to form an RC filter with the C_{VDD} capacitor.

Ground (GND)

This node is the reference for all other signals. TI recommends having a separate, quiet analog plane connected in one place to the power plane. The analog plane combines the components related to the pins VREF, EA+, EA-, COMP, SS/EN, DELAB, DELCD, DELEF, TMIN, RT, RSUM. The power plane combines the components related to the pins DCM, ADELEF, ADEL, CS, SYNC, OUTF, OUTE, OUTD, OUTC, OUTB, OUTA, and VDD. Figure 24 shows an example of layout and ground-plane connections.

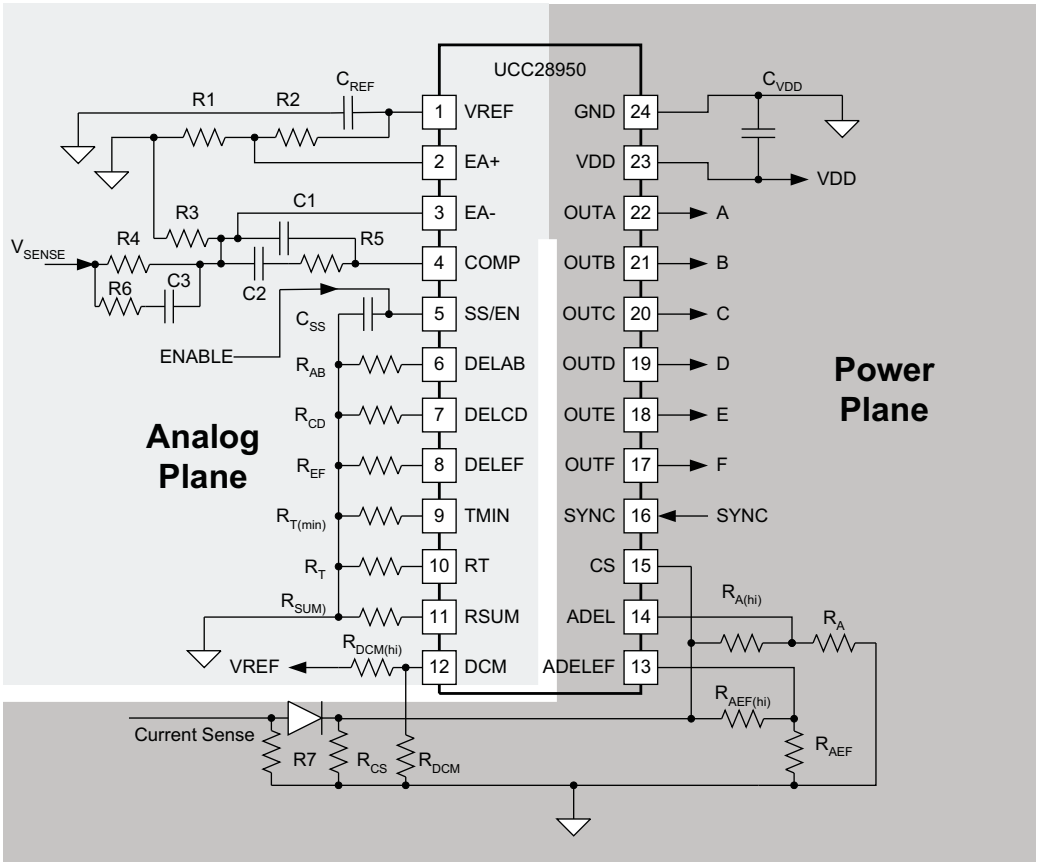


Figure 24. Layout Recommendation for Analog and Power Planes

TYPICAL CHARACTERISTICS

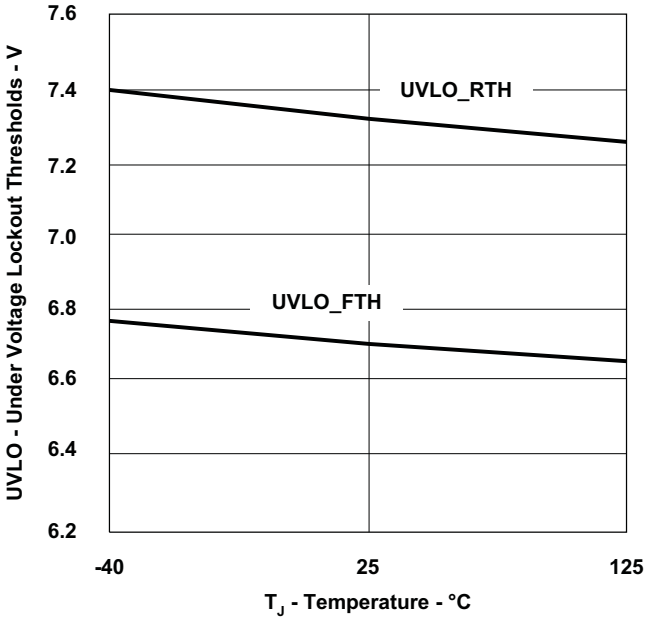


Figure 25.

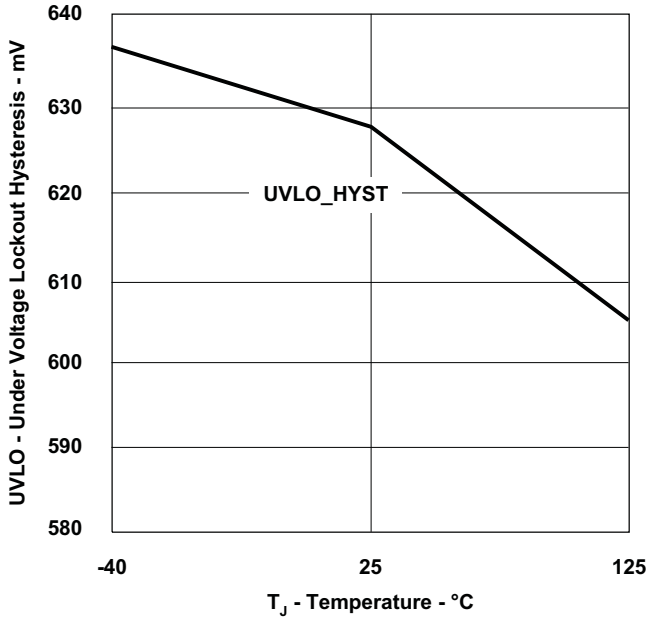


Figure 26.

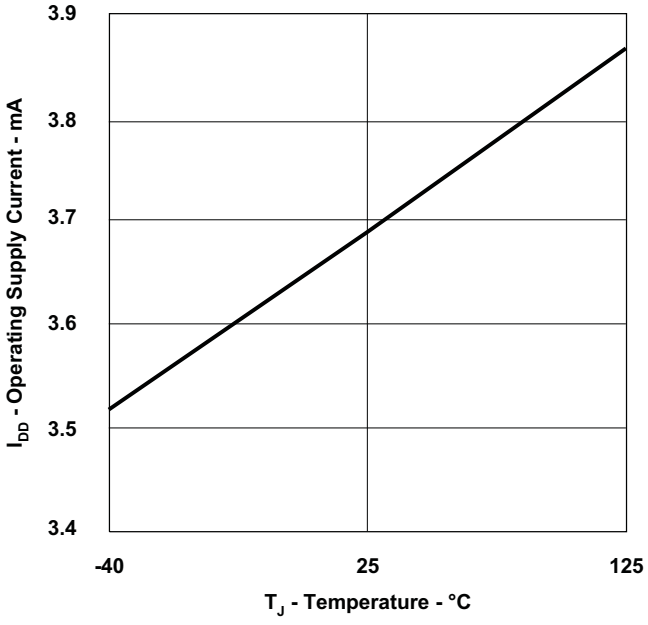


Figure 27.

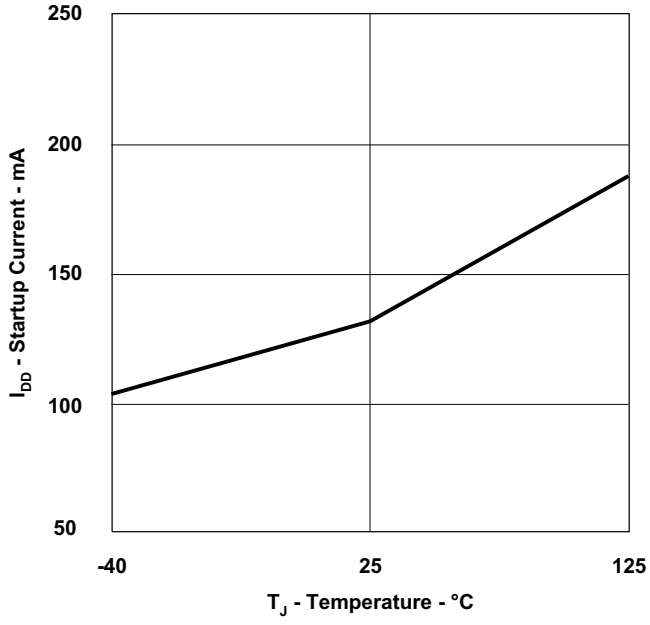


Figure 28.

TYPICAL CHARACTERISTICS (continued)

VOLTAGE REFERENCE (VDD = 12 V) vs TEMPERATURE

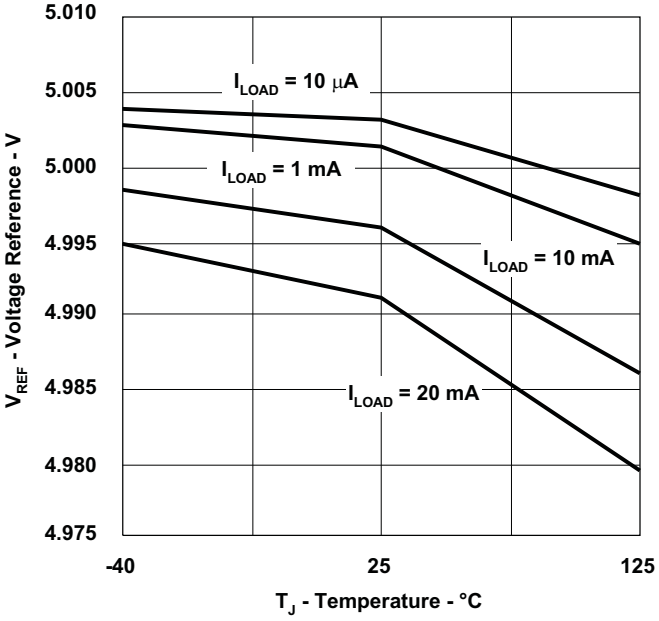


Figure 29.

LINE VOLTAGE REGULATION (I_{LOAD} = 10 mA) vs TEMPERATURE

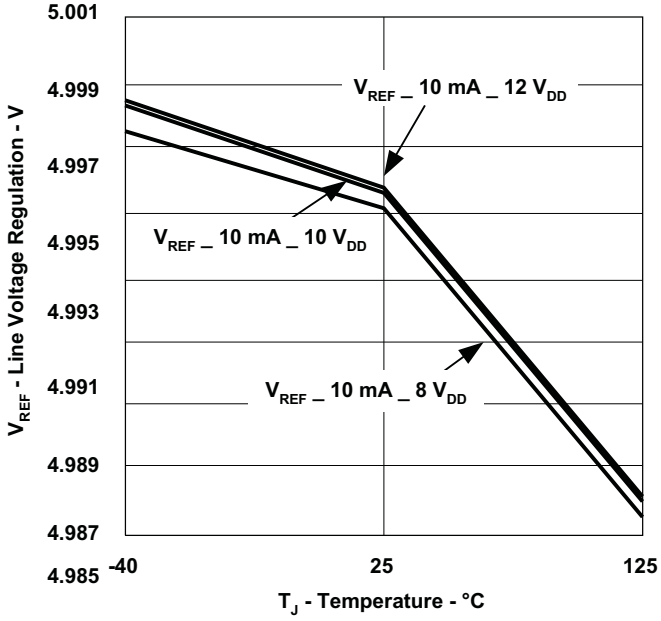


Figure 30.

SHORT CIRCUIT CURRENT vs TEMPERATURE

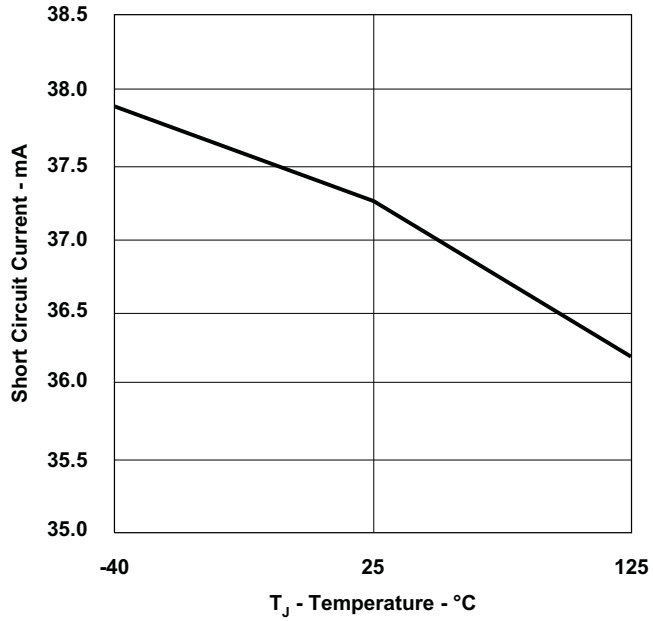


Figure 31.

MAXIMUM DUTY CYCLE vs TEMPERATURE

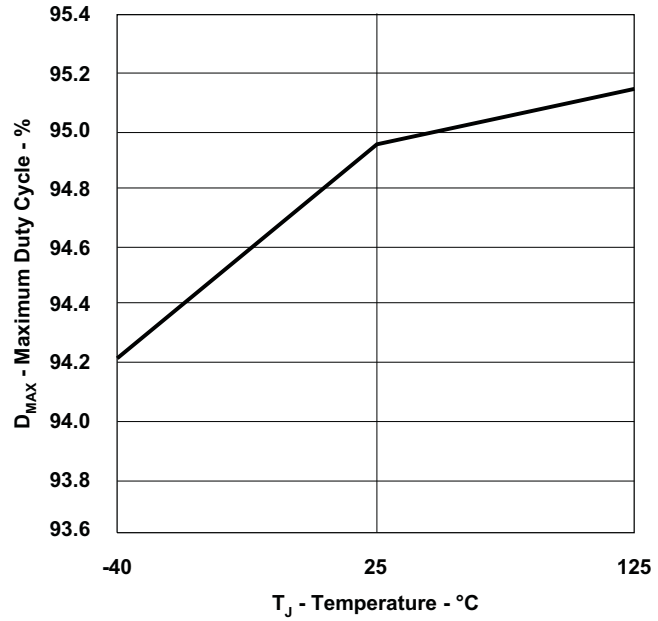


Figure 32.

TYPICAL CHARACTERISTICS (continued)

NOMINAL SWITCHING FREQUENCY vs TEMPERATURE

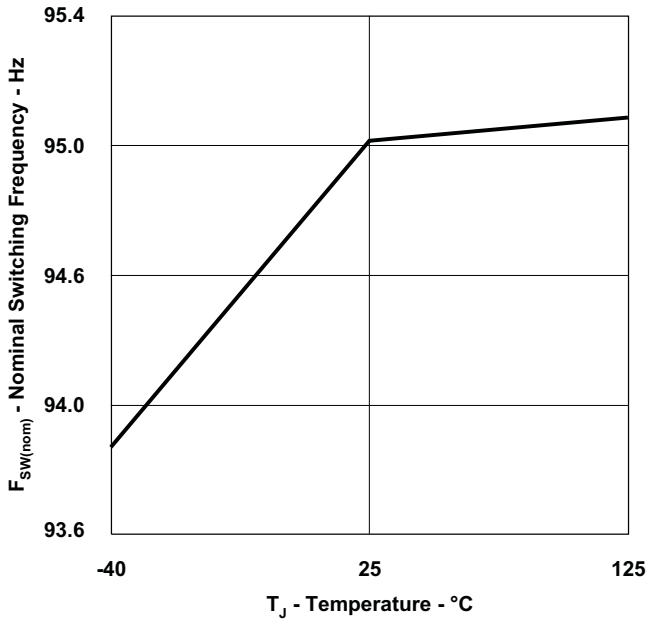


Figure 33.

MAXIMUM SWITCHING FREQUENCY vs TEMPERATURE

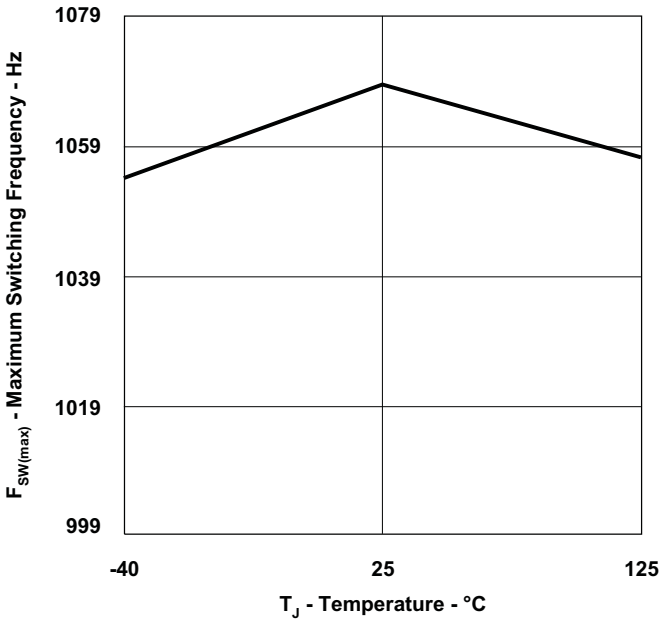


Figure 34.

ERROR AMPLIFIER OFFSET VOLTAGE vs TEMPERATURE

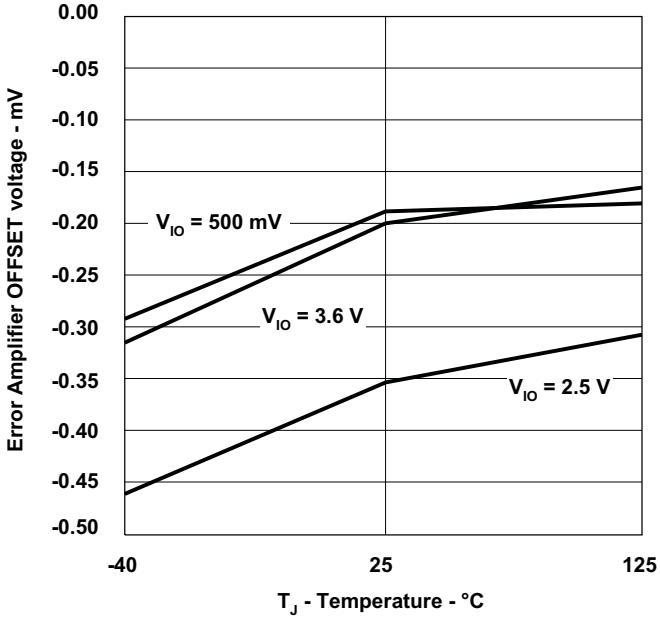


Figure 35.

VOLTAGE ERROR AMPLIFIER (Open Loop Gain) vs TEMPERATURE

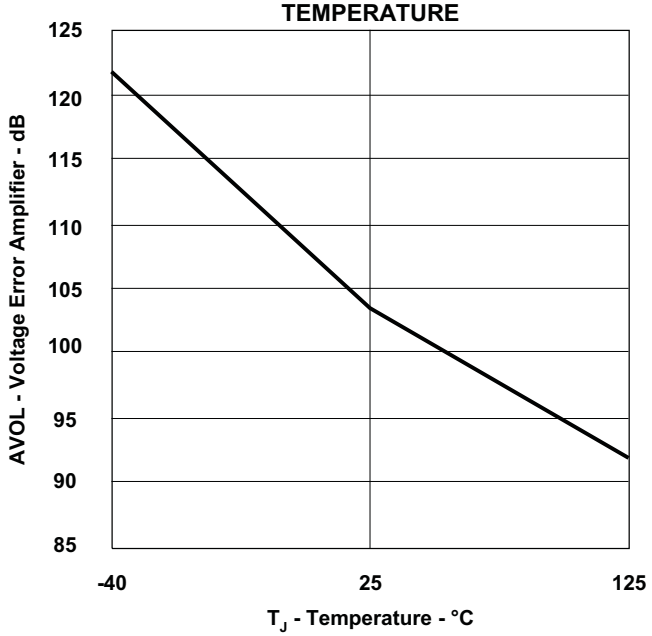


Figure 36.

TYPICAL CHARACTERISTICS (continued)

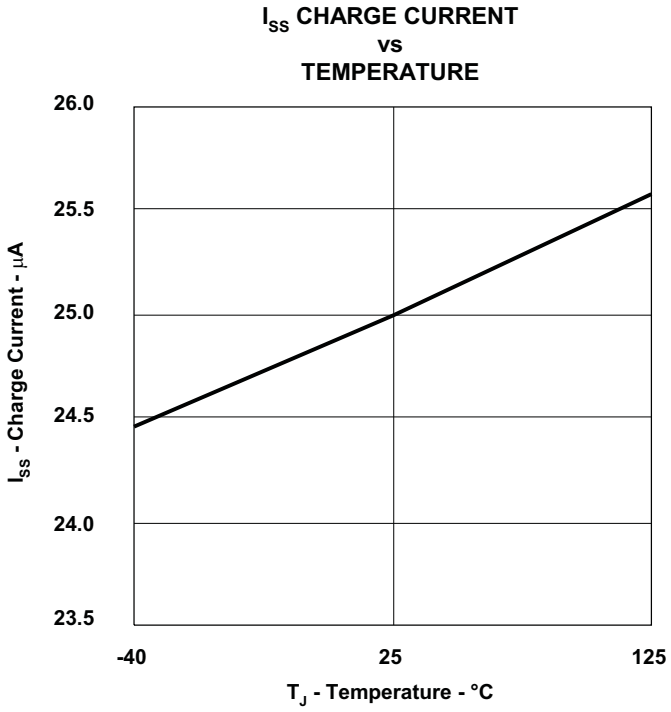


Figure 37.

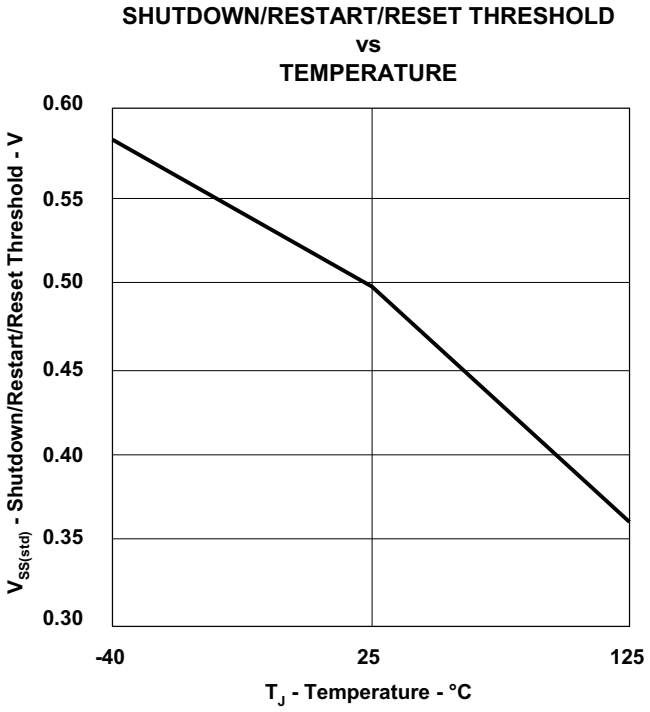


Figure 38.

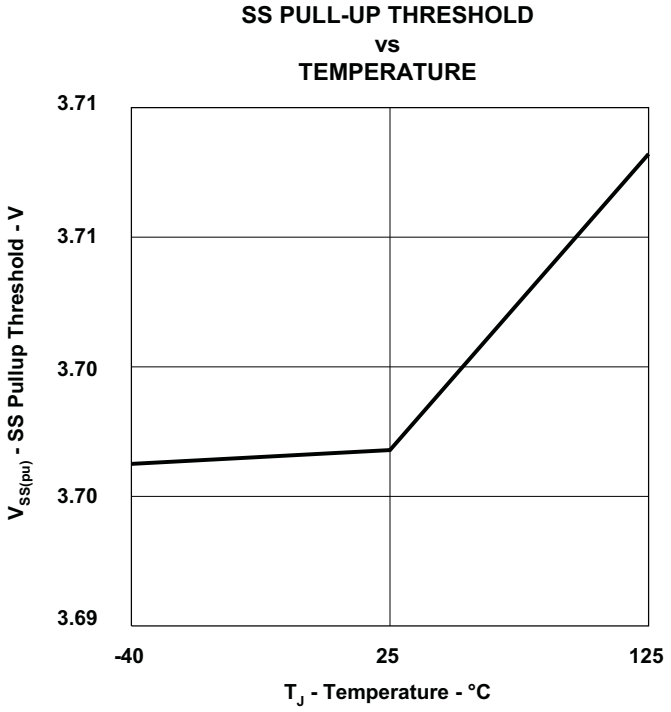


Figure 39.

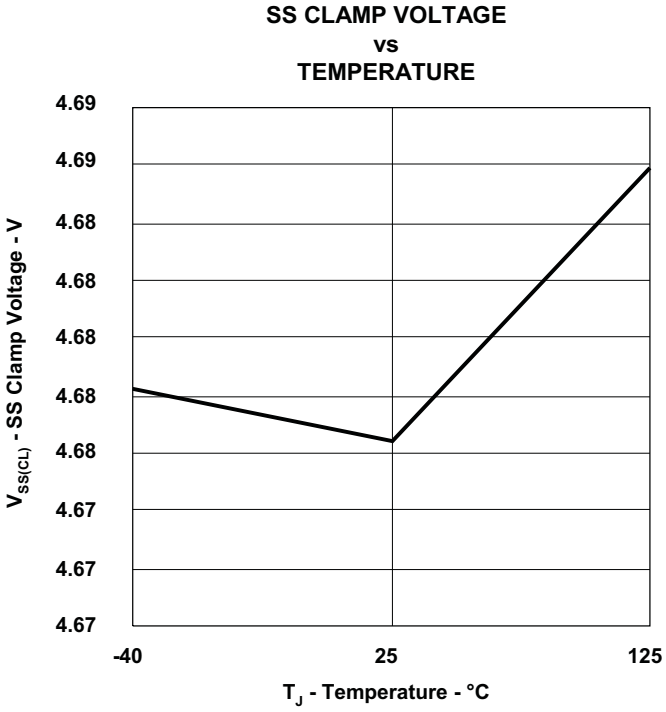


Figure 40.

TYPICAL CHARACTERISTICS (continued)

CURRENT SENSE CYCLE-BY-CYCLE LIMIT vs TEMPERATURE

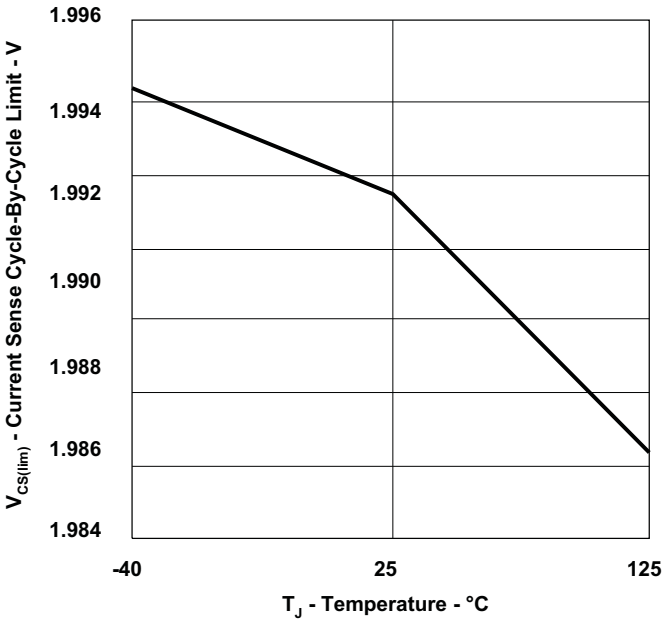


Figure 41.

CURRENT SENSE PROPAGATION DELAY vs TEMPERATURE

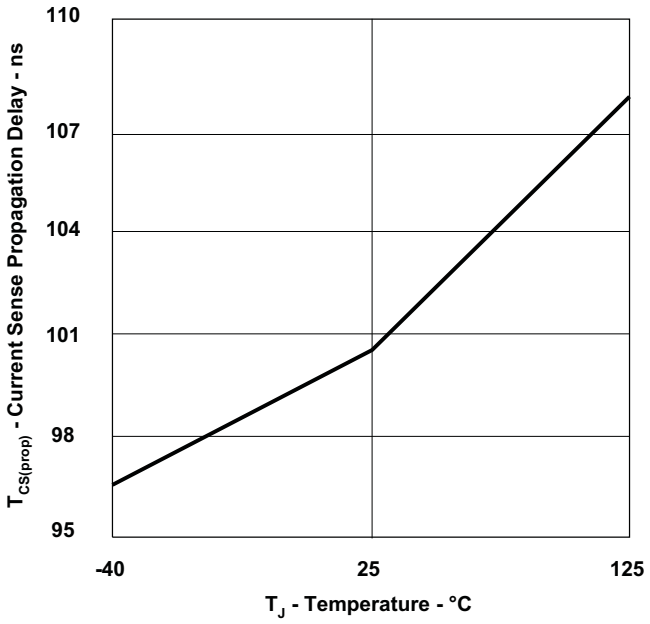


Figure 42.

OUTPUTS SINK RESISTANCE vs TEMPERATURE

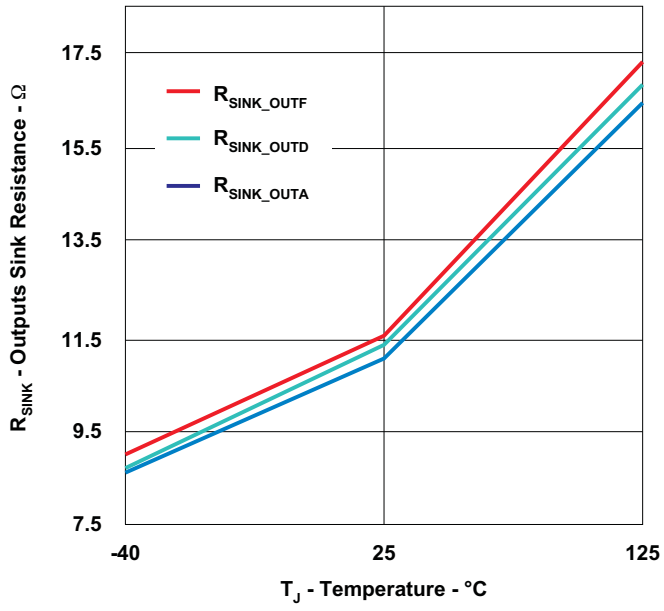


Figure 43.

OUTPUTS SINK RESISTANCE vs TEMPERATURE

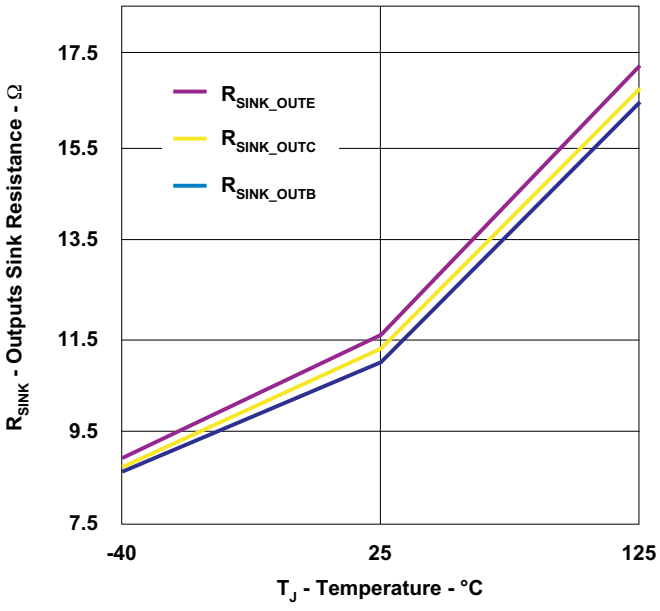


Figure 44.

TYPICAL CHARACTERISTICS (continued)

OUTPUTS SOURCE RESISTANCE vs TEMPERATURE

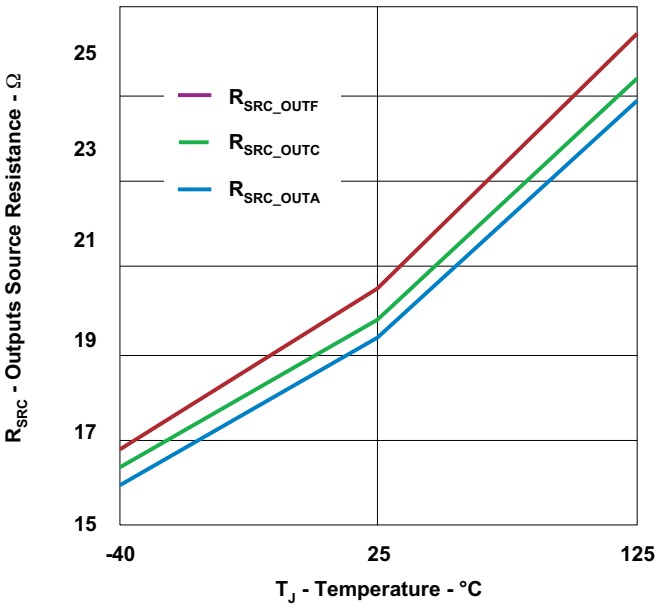


Figure 45.

OUTPUTS SOURCE RESISTANCE vs TEMPERATURE

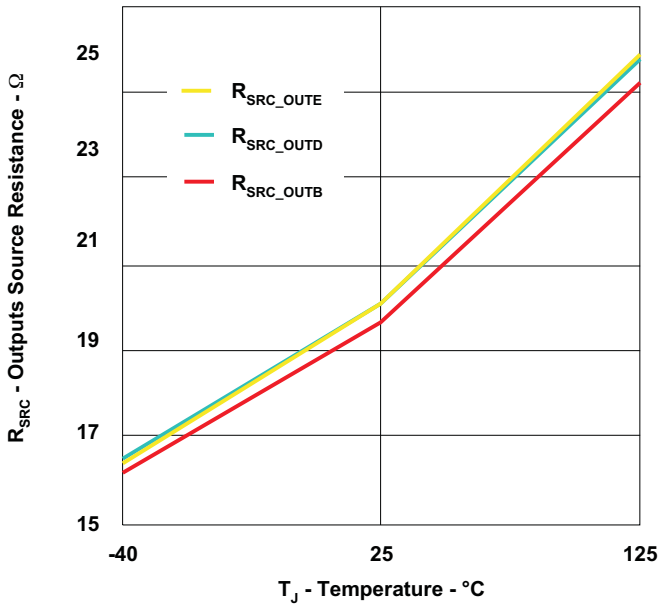


Figure 46.

DEAD TIME DELAY vs TEMPERATURE

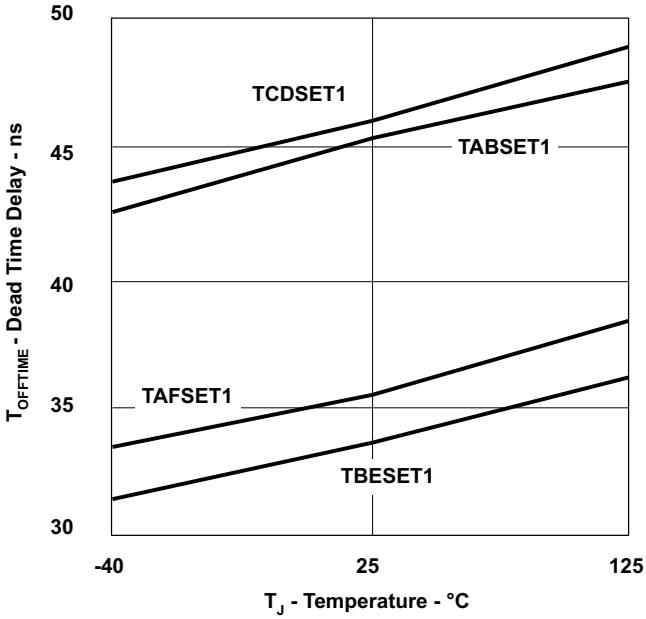


Figure 47.

DEAD TIME DELAY vs TEMPERATURE

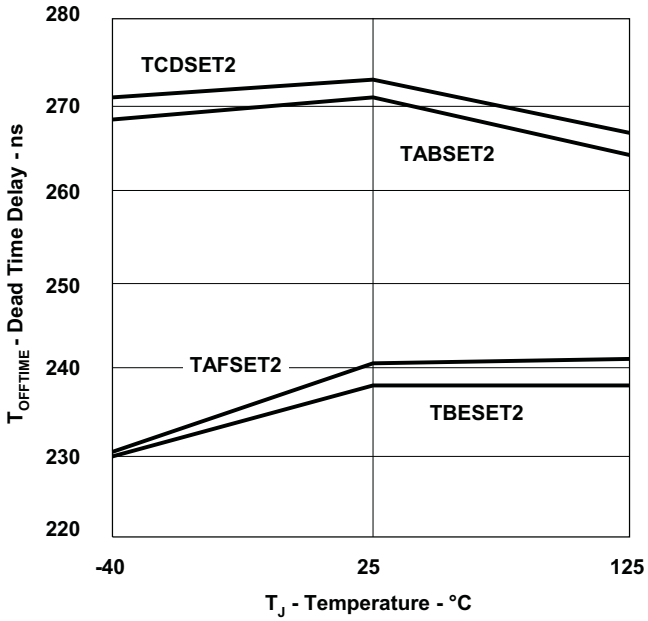


Figure 48.

TYPICAL CHARACTERISTICS (continued)

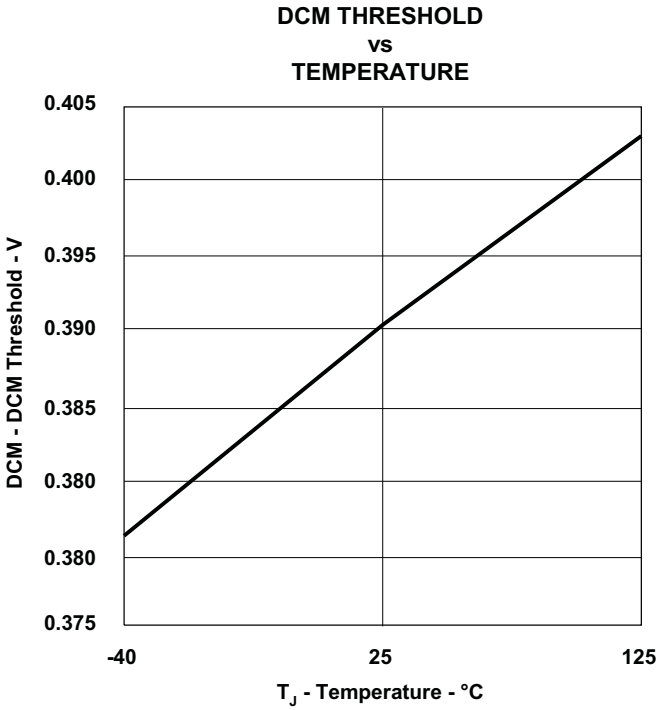


Figure 49.

APPLICATION INFORMATION

UCC28950-Q1 Application Description

Using the synchronous rectification technique, a control algorithm providing ZVS conditions over the entire load current range, accurate adaptive timing of the control signals between primary and secondary FETs, and special operating modes at light load for the highest efficiency and power saving achieves the efficiency improvement of a phase-shifted full-bridge dc-dc converter with the UCC28950-Q1. Figure 50 shows a simplified electrical diagram of this converter. The location of the controller device is on the secondary side of converter, although it could be on primary side as well. Location on the secondary side allows easy power-system level communication and better handling of some transient conditions that require fast, direct control of the synchronous rectifier MOSFETs. The power stage includes primary-side MOSFETs, QA, QB, QC, QD and secondary-side synchronous rectifier MOSFETs, QE and QF. For example, for the 12-V output converters in power supplies for servers use of the center-tapped rectifier scheme with an L-C output filter as a popular choice.

To maintain high efficiency at different output power conditions, the converter operates in nominal synchronous rectification mode at mid- and high-output power levels, transitioning to the diode-rectifier mode at light load, and further followed by the burst mode as the output power becomes even lower. All these transitions are based on current sensing on the primary side, using the current-sense transformer in this specific case.

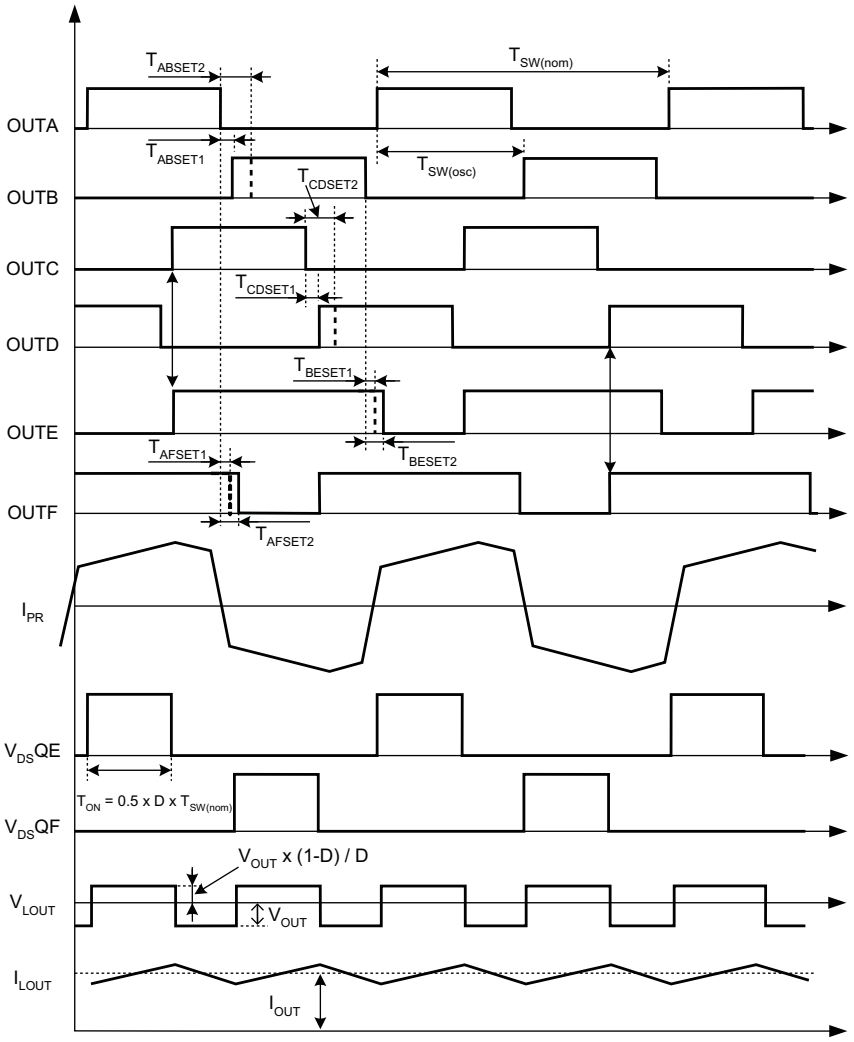


Figure 50. Major Waveforms of Phase-Shifted Converter

Figure 50 shows major waveforms of the phase-shifted converter during the nominal operation mode. The upper six waveforms in Figure 50 show the output drive signals of the controller. In the nominal mode, the outputs OUTE and OUTF overlap during the part of the switching cycle when the circuitry causes both rectifier MOSFETs to conduct and shorts the windings of the power transformer. Current, I_{PR}, is the current flowing through the primary winding of power transformer. The bottom four waveforms show the drain-source voltages of the rectifier MOSFETs, V_{DS_QE} and V_{DS_QF}, the voltage at the output inductor, V L_{OUT}, and the current through the output inductor, I L_{OUT}. Proper timing between the primary switches and synchronous rectifier MOSFETs is critical to achieve highest efficiency and reliable operation in this mode. The controller device adjusts the turnoff timing of the rectifier MOSFETs as a function of load current to ensure the minimum conduction time and reverse-recovery losses of their internal body diodes.

ZVS is an important feature of relatively high-input-voltage converters to reduce switching losses associated with the internal parasitic capacitances of power switches and transformers. The controller ensures ZVS conditions over the entire load-current range by adjusting the delay time between the primary MOSFETs switching in the same leg in accordance with the load variation. The controller also limits the minimum on-time pulse applied to the power transformer at light load, allowing the storage of sufficient energy in the inductive components of the power stage for the ZVS transition.

While the load current coninues reducing from the mid-load current down to the no-load condition, the controller selects the most-efficient power-saving mode by moving the converter from the nominal operation mode to the discontinuous-current diode-rectification mode and, eventually, at very light-load and at no-load condition, to the burst mode. Figure 51 shows these modes and the related output signals, OUTE, OUTF, driving the rectifier MOSFETs.

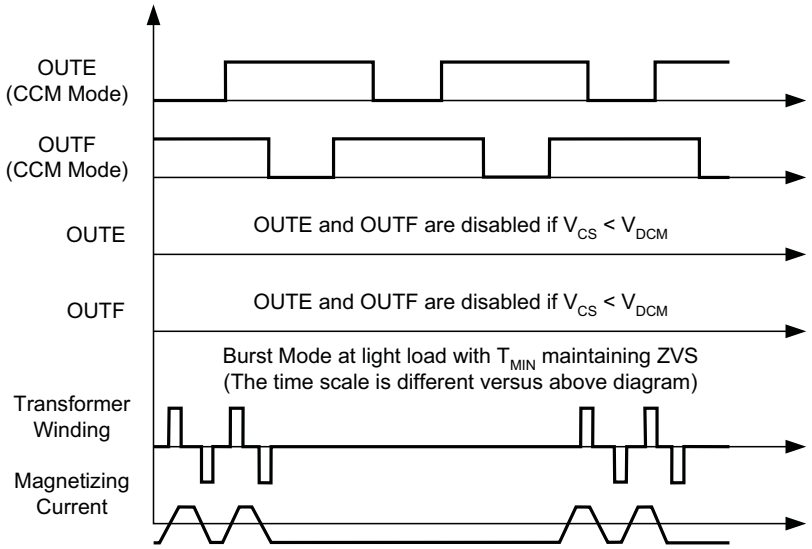


Figure 51. Major Waveforms During Transitions Between Different Operating Modes

It is necessary to prevent the reverse current flow through the synchronous rectifier MOSFETs and output inductor at light load, during parallel operation, and during some transient conditions. Such reverse current results in circulating of some extra energy between the input-voltage source and the load and, therefore, causes increased losses and reduces efficiency. Another negative effect of such reverse current is the loss of the ZVS condition. The suggested control algorithm prevents reverse current flow, still maintaining most of the benefits of synchronous rectification by switching off the drive signals of the rectifier MOSFETs in a predetermined way. At some predetermined load-current threshold, the controller disables outputs OUTE and OUTF by bringing them down to zero.

Synchronous rectification using MOSFETs requires some electrical energy to drive the MOSFETs. There is a condition below some light-load threshold when the MOSFET drive related losses exceed the saving provided by synchronous rectification. At such light loads, it is best to disable the drive circuit and use the internal body diodes of the rectifier MOSFETs, or external diodes in parallel with the MOSFETs, for more-efficient rectification. In most practical cases, disabling the drive circuit close to DCM mode is necessary. This mode of operation is discontinuous-current diode-rectification mode.

At very light-load and no-load conditions, the duty cycle, demanded by the closed-feedback-loop control circuit for output voltage regulation, can be very low. This could lead to loss of the ZVS condition and increased switching losses. To avoid the loss of ZVS, the control circuit limits the minimum on-time pulse applied to the power transformer, using the resistor from the TMIN pin to GND. Therefore, the only way to maintain regulation at very light load and in the no-load condition is to skip some pulses. The controller skips pulses in a controllable manner to avoid saturation of the power transformer. This is operation in burst mode. In burst mode, there is always an even number of pulses applied to the power transformer before the skipping off-time. Thus, the flux in the core of the power transformer always starts from the same point during the start of every burst of pulses.

Voltage Loop Compensation Recommendation

For best results in the voltage loop TI recommends using a Type 2 or Type 3 compensation network (Figure 52). A Type 2 compensation network does not require passive components C_{Z2} and R_{Z2}. Type 1 compensation is not versatile enough for a phase-shifted full bridge. When evaluating COMP for best results, TI recommends putting a 1-kΩ resistor between the scope probe and the COMP pin of the UCC28950-Q1.

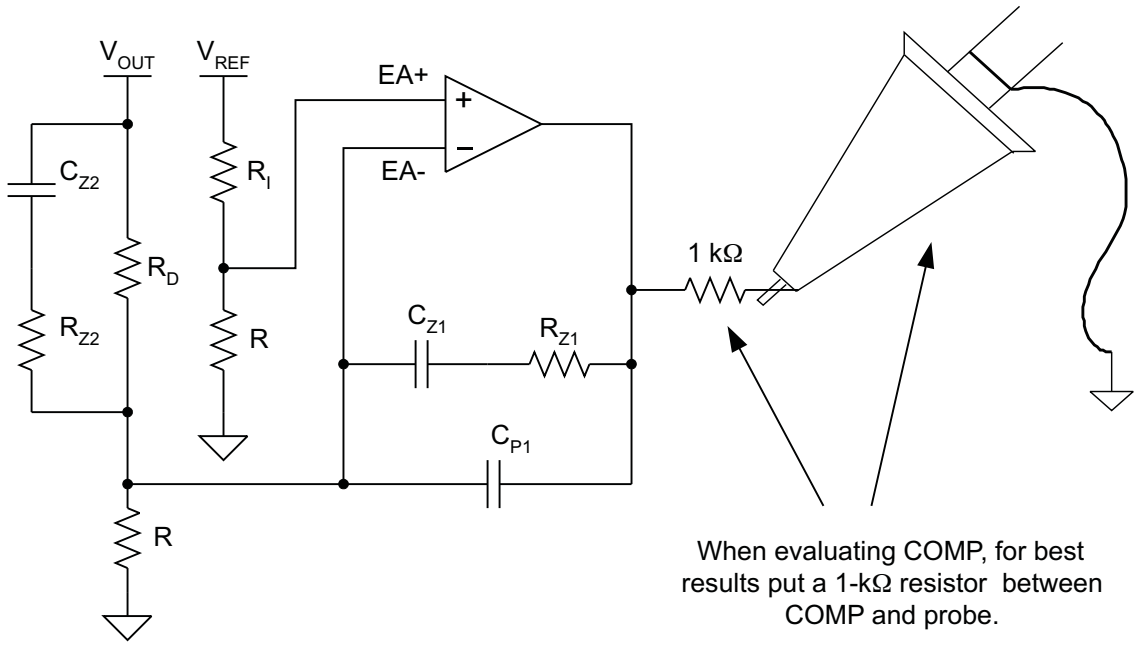


Figure 52. Type 3 Compensation Evaluation

Experimental Results Example

The following experimental results are based on 660-W output-power prototype of a phase-shifted full-bridge dc-dc converter. The input voltage is 300 V to 400 V and the output is 12 V, 55 A. The primary MOSFETs are SPA11N60CFD and the synchronous rectifier MOSFETs are FDP047AN08A0, two in parallel. Figure 53 shows the measured efficiency of the prototype.

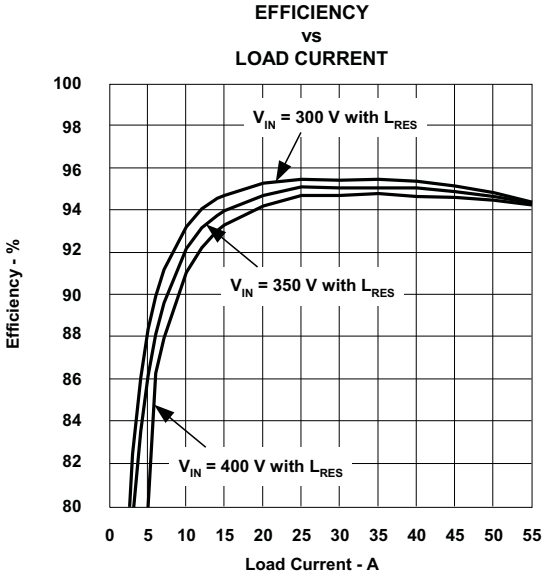


Figure 53. Efficiency of the Prototype Phase-Shifted Converter (V_{IN} = 300 V, 350 V and 400 V, V_{OUT} = 12 V)

Because of the power saving need even at very light and no-load conditions, the user must carefully optimize operation at light-load conditions to set the proper boundaries between different operation modes. Figure 54 shows the result of this optimization. This plot demonstrates the power savings while moving from the synchronous rectification mode above 1-A load current, into the discontinuous current mode with the diode rectification between 0.3-A and 1-A load current, and eventually into the burst mode operation at load current below 0.3 A.

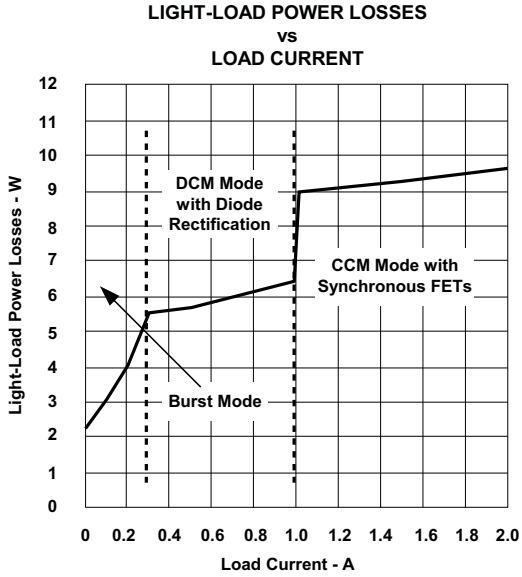


Figure 54. Power Losses of the Prototype at Light-Load and No-Load Conditions

REVISION HISTORY

Changes from Revision A (July, 2012) to Revision B	Page
• Removed Package column from Ordering Information table.	3
• Removed row 1 from Ordering Information table; changed Top-side Marking from U28950Q to UCC28950Q.	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28950QPWRQ1	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28950Q	Samples
UCC28950TPWRQ1	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	UCC28950Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC28950-Q1 :

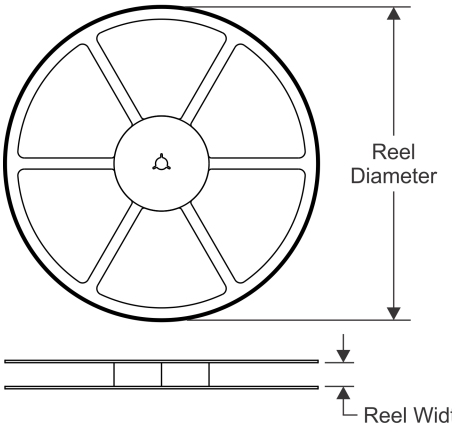
- Catalog: UCC28950

NOTE: Qualified Version Definitions:

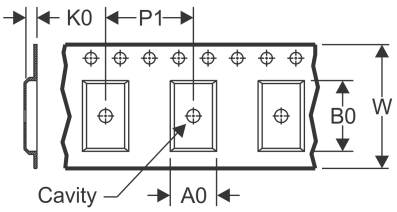
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

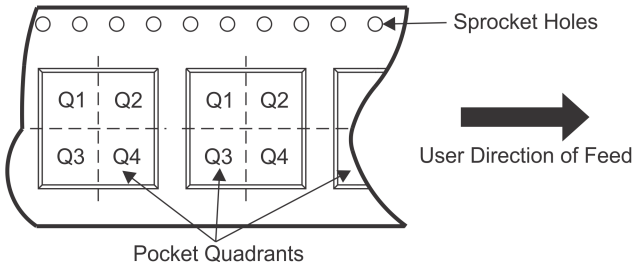


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

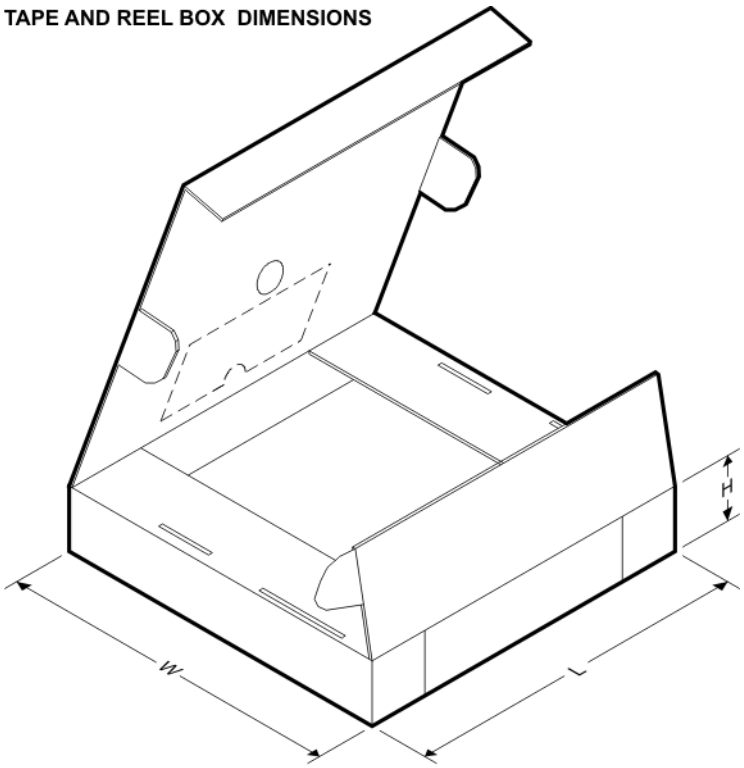
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28950QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
UCC28950TPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

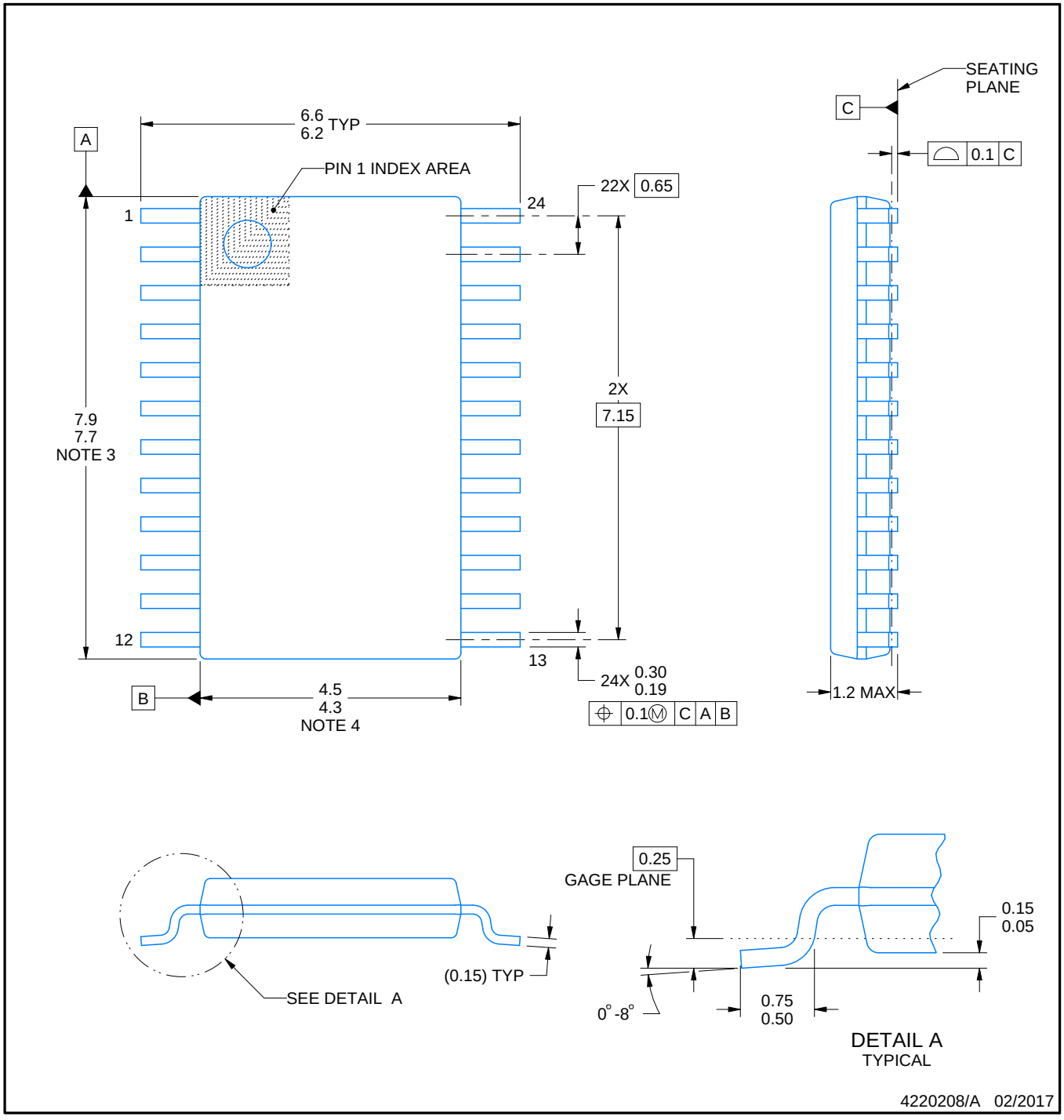
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28950QPWRQ1	TSSOP	PW	24	2000	350.0	350.0	43.0
UCC28950TPWRQ1	TSSOP	PW	24	2000	350.0	350.0	43.0

PACKAGE OUTLINE

PW0024A

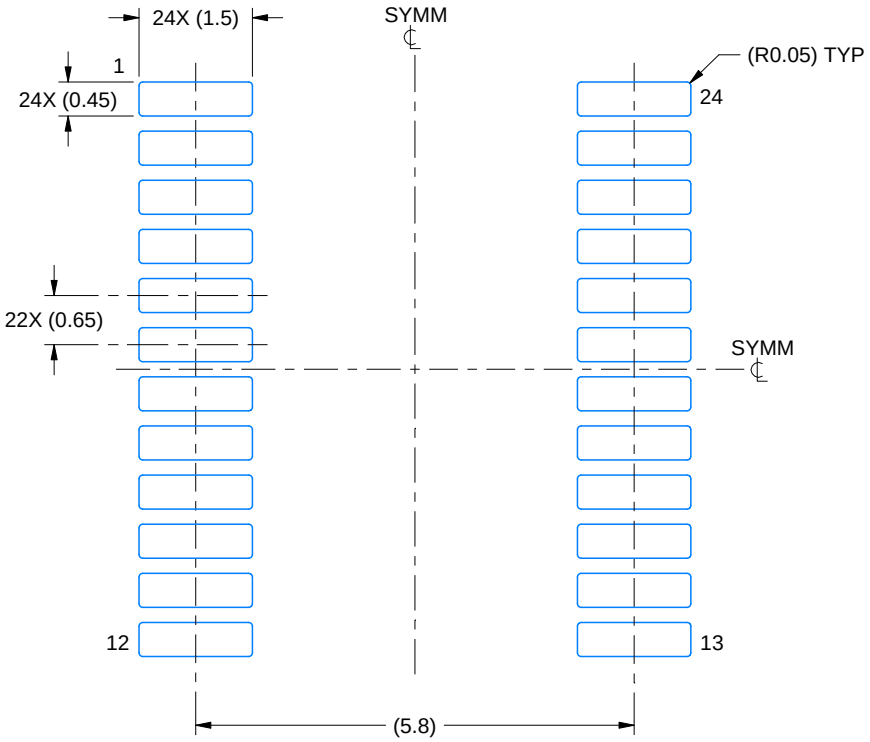
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

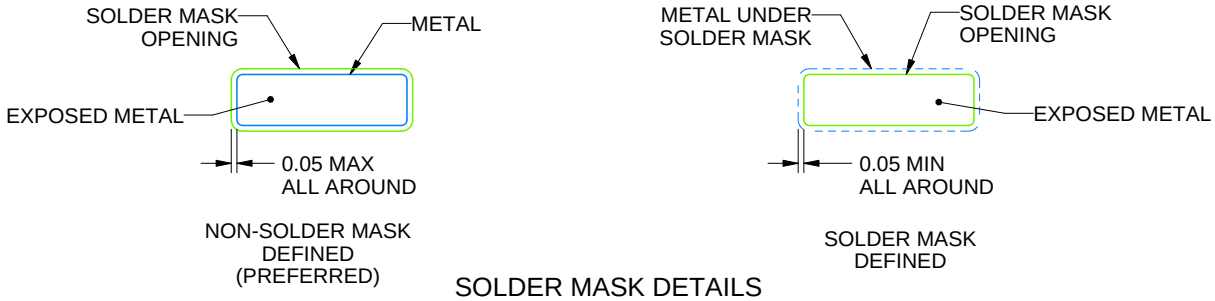


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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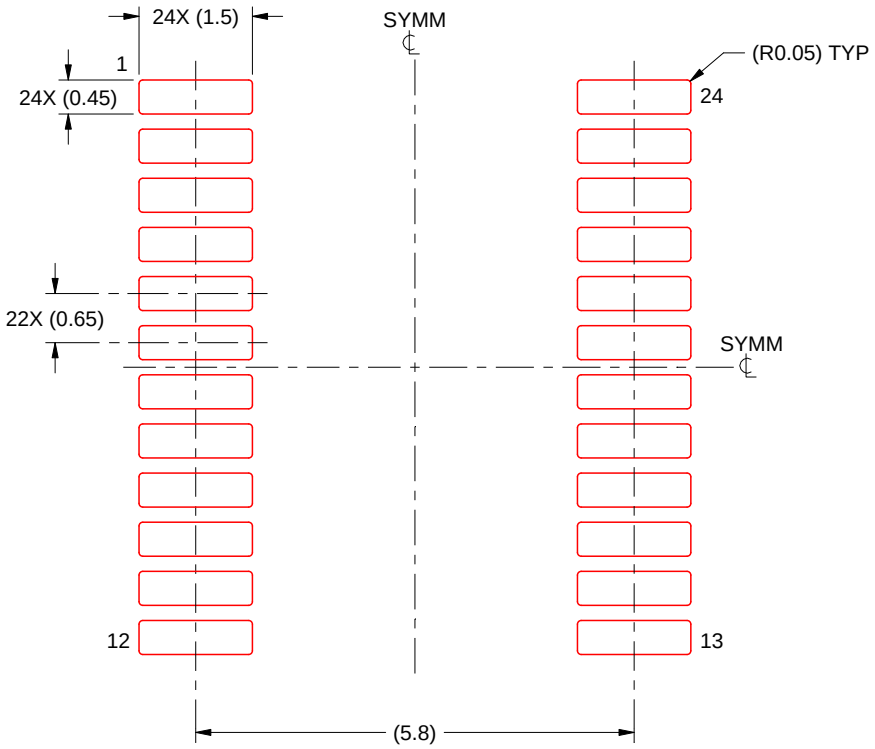
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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