

# NTF3055L175

## Power MOSFET 2.0 A, 60 V, Logic Level

### N-Channel SOT-223

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

#### Features

- This is a Pb-Free Device

#### Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

#### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	60	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 1.0\text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Gate-to-Source Voltage Continuous Non-repetitive ( $t_p \leq 10\text{ ms}$ )	$V_{GS}$	$\pm 15$ $\pm 20$	Vdc Vpk
Drain Current Continuous @ $T_A = 25^\circ\text{C}$ Continuous @ $T_A = 100^\circ\text{C}$ Single Pulse ( $t_p \leq 10\text{ }\mu\text{s}$ )	$I_D$ $I_D$ $I_{DM}$	2.0 1.2 6.0	Adc Adc Apk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2) Derate above $25^\circ\text{C}$	$P_D$	2.1 1.3 0.014	W W W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 25\text{ Vdc}$ , $V_{GS} = 5.0\text{ Vdc}$ , $I_{L(pk)} = 3.6\text{ A}$ , $L = 10\text{ mH}$ , $V_{DS} = 60\text{ Vdc}$ )	$E_{AS}$	65	mJ
Thermal Resistance Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{\theta JA}$ $R_{\theta JA}$	72.3 114	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

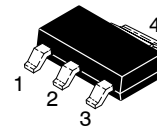
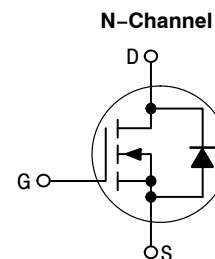
1. When surface mounted to an FR4 board using 1" pad size, 1 oz. (Cu. Area 0.995 in<sup>2</sup>).
2. When surface mounted to an FR4 board using minimum recommended pad size, 2-2.4 oz. (Cu. Area 0.272 in<sup>2</sup>).



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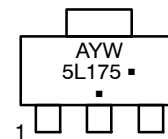
<http://onsemi.com>

**2.0 AMPERES, 60 VOLTS**  
 **$R_{DS(on)} = 175\text{ m}\Omega$**



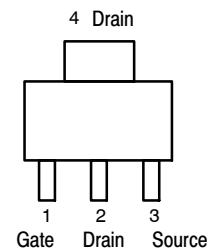
SOT-223  
CASE 318E  
STYLE 3

#### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
W = Work Week  
5L175 = Device Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

#### PIN ASSIGNMENT



#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTF3055L175

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 –	72.8 74.4	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ± 15 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	–	–	± 100	nAdc

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 –	1.7 4.2	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 1.0 Adc)	R <sub>DS(on)</sub>	–	155	175	mΩ
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 2.0 Adc) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 1.0 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	–	0.32 0.57	0.42 –	Vdc
Forward Transconductance (Note 3) (V <sub>DS</sub> = 8.0 Vdc, I <sub>D</sub> = 1.5 Adc)	g <sub>fs</sub>	–	3.2	–	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 V, f = 1.0 MHz)	C <sub>iss</sub>	–	194	270	pF
Output Capacitance		C <sub>oss</sub>	–	70	100	
Transfer Capacitance		C <sub>rss</sub>	–	29	40	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 2.0 Adc, V <sub>GS</sub> = 5.0 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 3)	t <sub>d(on)</sub>	–	10.2	20	ns
Rise Time		t <sub>r</sub>	–	21	40	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	14.3	30	
Fall Time		t <sub>f</sub>	–	15.3	30	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 2.0 Adc, V <sub>GS</sub> = 5.0 Vdc) (Note 3)	Q <sub>T</sub>	–	5.1	10	nC
		Q <sub>1</sub>	–	1.4	–	
		Q <sub>2</sub>	–	2.5	–	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 2.0 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 2.0 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C) (Note 3)	V <sub>SD</sub>	– –	0.84 0.68	1.0 –	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 2.0 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	–	28.3	–	ns
		t <sub>a</sub>	–	15.6	–	
		t <sub>b</sub>	–	12.7	–	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	0.027	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

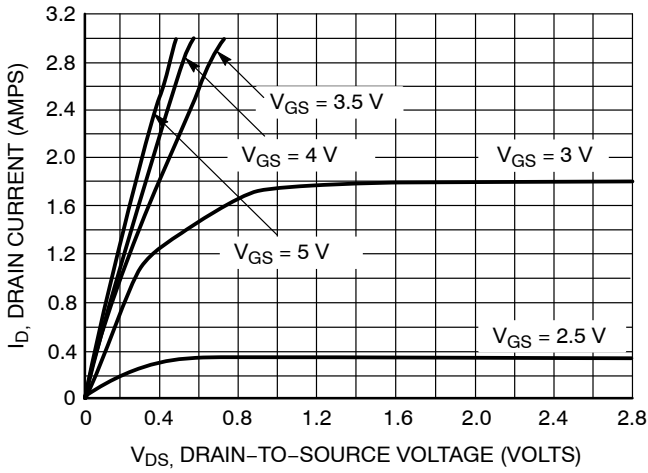


Figure 1. On-Region Characteristics

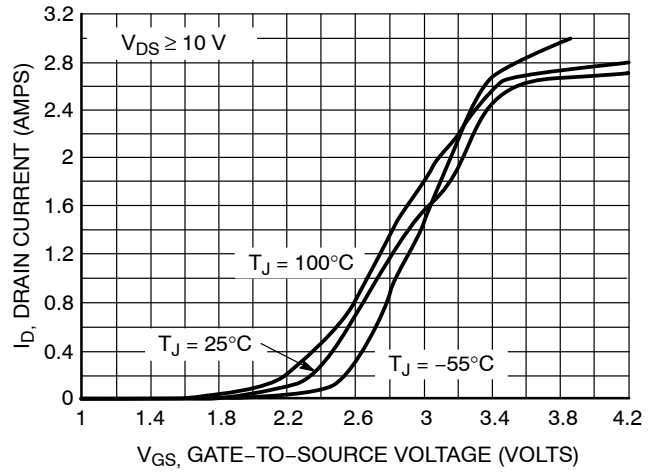


Figure 2. Transfer Characteristics

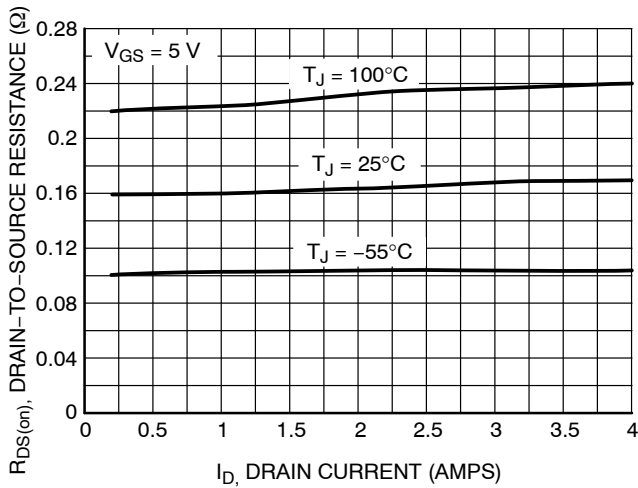


Figure 3. On-Resistance versus Gate-to-Source Voltage

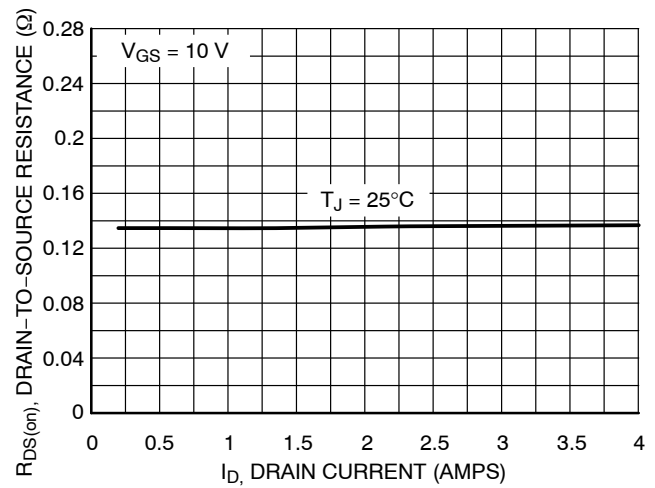


Figure 4. On-Resistance versus Drain Current and Gate Voltage

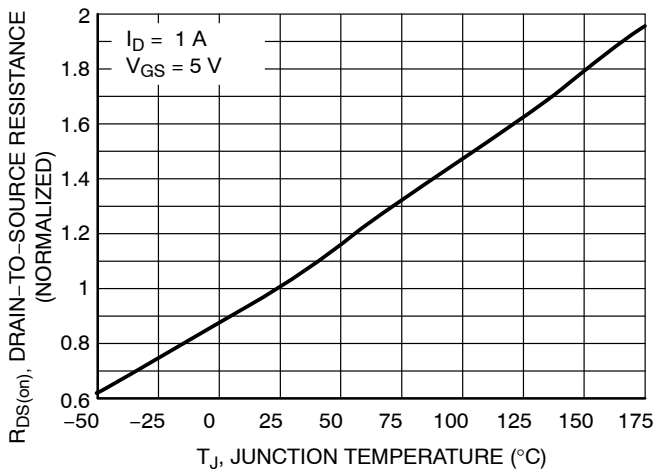


Figure 5. On-Resistance Variation with Temperature

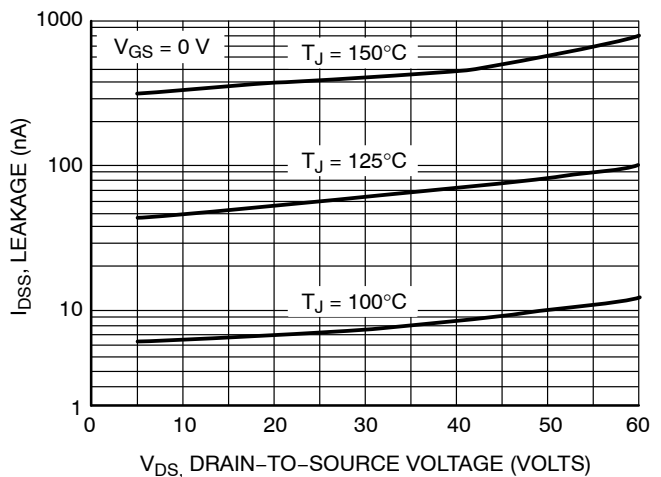


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

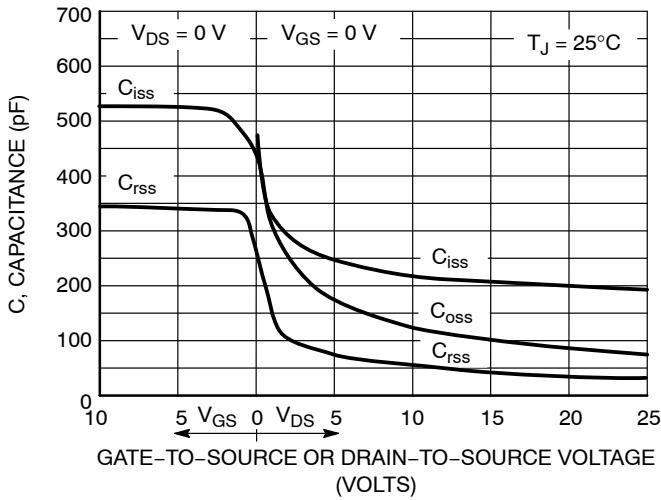


Figure 7. Capacitance Variation

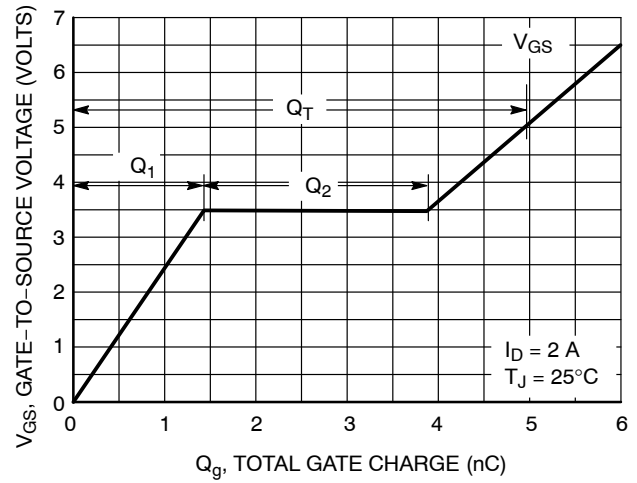


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

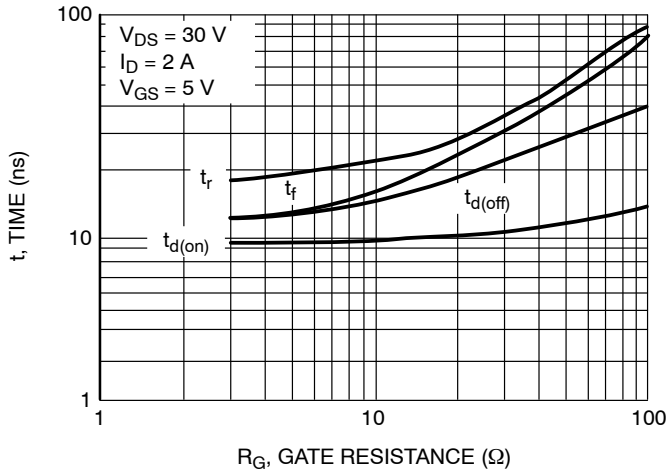


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

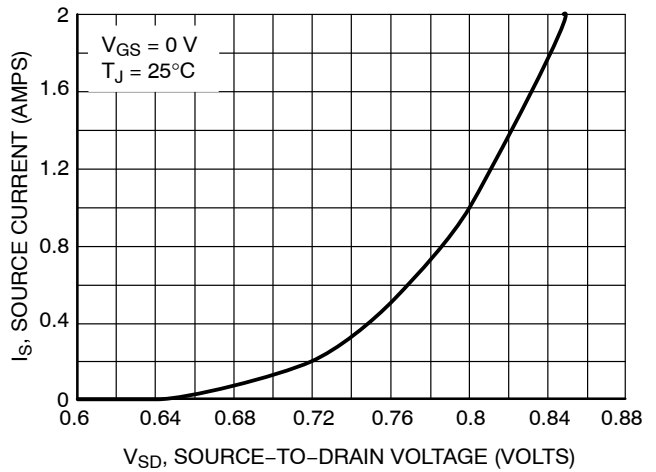


Figure 10. Diode Forward Voltage versus Current

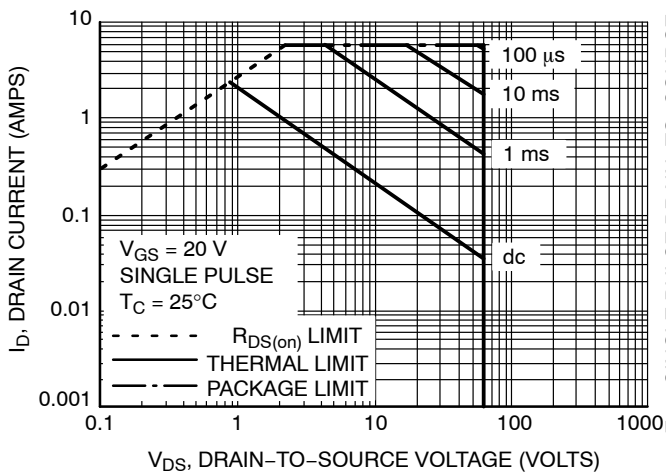


Figure 11. Maximum Rated Forward Biased Safe Operating Area

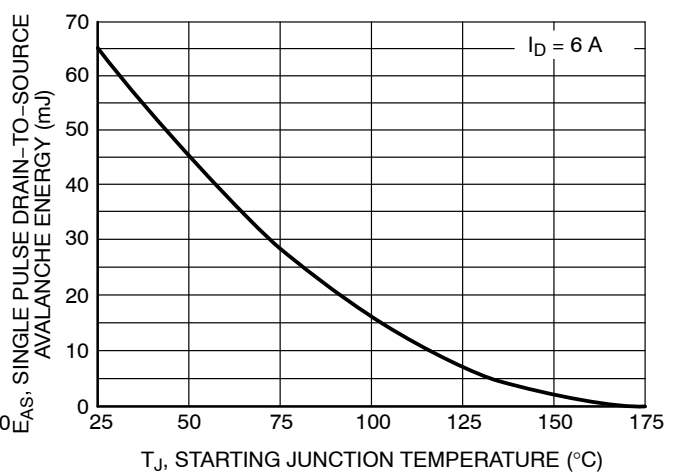


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

# NTF3055L175

## TYPICAL ELECTRICAL CHARACTERISTICS

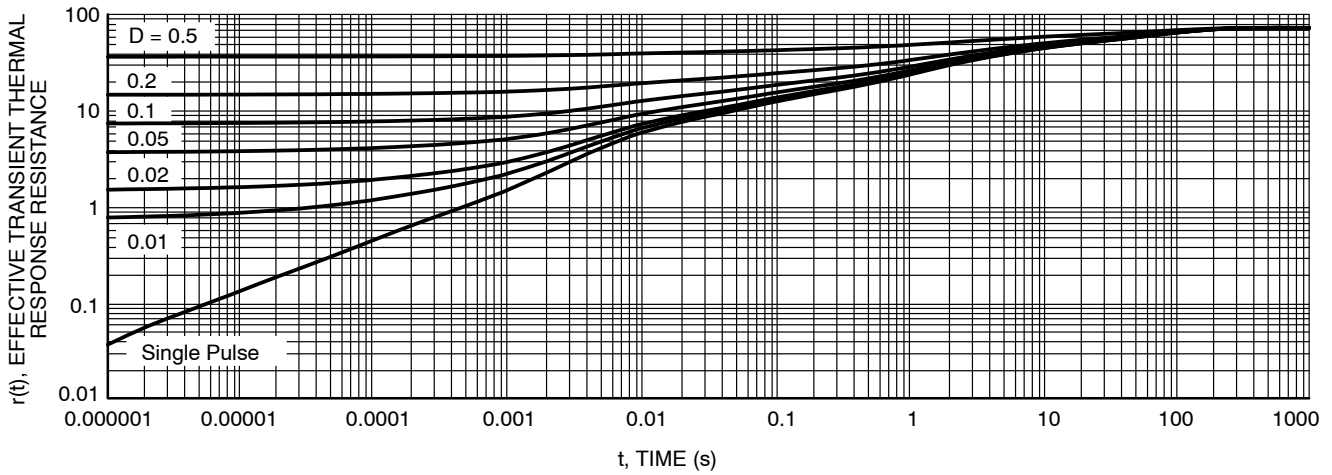


Figure 13. Thermal Response

### ORDERING INFORMATION

Device	Package	Shipping†
NTF3055L175T1G	SOT-223 (TO-261) (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
$\theta$	0°	---	10°



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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |  |   |   |   |   |
|--|---|---|---|---|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |   |   |

**GENERIC  
 MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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