AK5704

Low-Power 4-ch 32-bit ADC with MIC-Amp

1. General Description

The AK5704 is a high performance analog front-end AD converter IC ideal for voice recognition, voice control, and conferencing applications. The device has a built-in 4-ch 32-bit ADC and a low noise microphone amplifier and extracts full performance of a high S/N microphone with low power consumption by achieving dynamic range of 105dB. It is possible to support up to 16-ch microphone array by connecting multiple AK5704's. In addition, since it incorporates ultra-low power consumption voice activity detection, power consumption during wait time is greatly reduced.

2. Features

1. Recording Function
- **4-Channel Low Power 32-bit ADC**
  2-types Digital Filter (Low-latency [5/fs] Sharp Roll-off and Voice)
- **Single-ended Inputs or Full-differential Inputs**
- **MIC Amplifier Gain: +30 dB to 0 dB, 3 dB step**
- **2-output MIC Power Supplies: 2.8 V / 2.5 V / 1.8 V / Direct Mode Selectable**
- **ADC Characteristics:**
  S/N, DR: 105 dB, THD+N: –90 dB, (Gain = 0 dB)
  S/N, DR: 96 dB, THD+N: –86 dB, (Gain = +18 dB)
- **Excellent Power Supply Noise Reduction**
  PSRR: 60dB
  Spurious Free Dynamic Range: 100dBc
- **4-Channel Digital MIC Interface**
- **Programmable Phase Adjustment**
- **Microphone Sensitivity Adjustment**

2. Digital Voice Activity Detector

3. Programmable Digital Filter
- **Mixer**
- **2nd order HPF and LPF**
- **Digital ALC (Automatic Level Control): 4-ch Link Mode, 2-ch Mode**

4. Digital Audio interface
- **Master/Slave mode**
- **Sampling Frequency:**
  8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 88.2 k, 96 k, 176.4 k, 192 kHz
- **Interface Format**
  - 32/24/16-bit I²S/MSB justified, 16-bit PCM Short/Long Frame
  - 4-ch TDM
  - 8/12/16-ch Cascade TDM

5. Built-in PLL

6. Control I/F: I²C-bus (400kHz)

7. Operation Temperature Range: Ta = –40 to 85°C

8. Power Supply:
- **AVDD (ADC, MIC, PLL): 1.7 to 1.9 V or 3.0V to 3.6V**
- **TVDD (Host & Audio I/F, LDO12): 1.65 to 3.6 V**

9. Package: 28-pin QFN

3. Table of Contents

4. Block Diagram

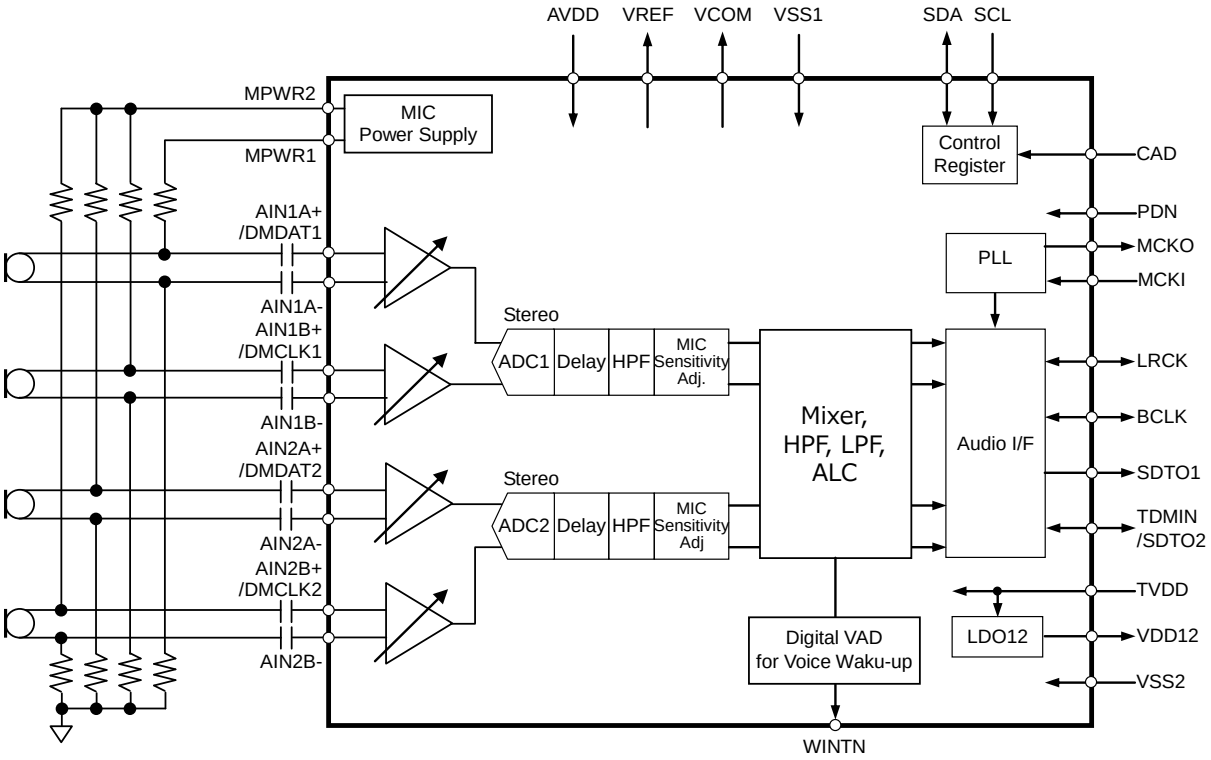
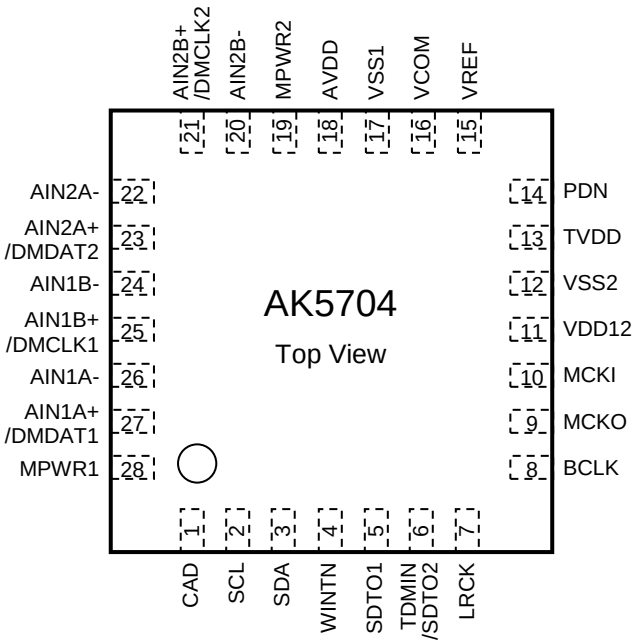


Figure 1. AK5704 Block Diagram

5. Pin Configurations and Functions

5.1. Pin Configurations

28-pin QFN



5.2. Functions

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
1	CAD	I	I^2C Chip Address Pin	TVDD/ VSS2	TVDD
2	SCL	I	I^2C Serial Data Clock Pin	TVDD/ VSS2	TVDD
3	SDA	I/O	I^2C Serial Data Input/Output Pin	TVDD/ VSS2	TVDD
4	WINTN	O	Interrupt Output Pin	TVDD/ VSS2	TVDD
5	SDTO1	O	Audio Serial Data Output 1 Pin	TVDD/ VSS2	TVDD
6	TDMIN	I	TDM Data Input Pin (Default) (SDTO2E bit = "0")	TVDD/ VSS2	TVDD
	SDTO2	O	Audio Serial Data Output 2 Pin (SDTO2E bit = "1")		
7	LRCK	I/O	Frame Sync Clock Pin	TVDD/ VSS2	TVDD
8	BCLK	I/O	Audio Serial Data Clock Pin	TVDD/ VSS2	TVDD
9	MCKO	O	Master Clock Output Pin	TVDD/ VSS2	TVDD
10	MCKI	I	Master Clock Input Pin	TVDD/ VSS2	TVDD
11	VDD12	-	LDO12 (1.2 V) Output Pin This pin must be connected to the VSS2 pin with a 2.2 µF ±50 % capacitor in series.	TVDD/ VSS2	TVDD
12	VSS2	-	Digital Ground Pin		
13	TVDD	-	Digital I/F & LDO12 Power Supply Pin		TVDD
14	PDN	I	Power down Pin "L": Power-down, "H": Power-Up	TVDD/ VSS2	TVDD
15	VREF	O	Voltage Reference Pin This pin must be connected to the VSS1 pin with a 2.2 µF ±50% Ceramic capacitor in series.	AVDD/ VSS1	AVDD
16	VCOM	O	Common Voltage Output Pin This pin must be connected to the VSS1 pin with a 2.2 µF ±50% Ceramic capacitor in series.	AVDD/ VSS1	AVDD
17	VSS1	-	Analog Ground Pin		
18	AVDD	-	Analog Power Supply Pin		AVDD
19	MPWR2	O	MIC Power Supply 2 Pin	AVDD/ VSS1	AVDD

Note 1. Do not connect a load to the VDD12 pin, the VCOM pin and the VREF pin.

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
20	AIN2B-	I	Negative Analog Input 2B Pin	AVDD/ VSS1	AVDD
21	AIN2B+	I	Positive Analog Input 2B Pin (DMIC2 bit = “0”)	AVDD/ VSS1	AVDD
	DMCLK2	O	Digital Microphone Clock Output 2 Pin (DMIC2 bit = “1”)		
22	AIN2A-	I	Negative Analog Input 2A Pin	AVDD/ VSS1	AVDD
23	AIN2A+	I	Positive Analog Input 2A Pin (DMIC2 bit = “0”)	AVDD/ VSS1	AVDD
	DMDAT2	I	Digital Microphone Data Input 2 Pin (DMIC2 bit = “1”)		
24	AIN1B-	I	Negative Analog Input 1B Pin	AVDD/ VSS1	AVDD
25	AIN1B+	I	Positive Analog Input 1B Pin (DMIC1 bit = “0”)	AVDD/ VSS1	AVDD
	DMCLK1	O	Digital Microphone Clock Output 1 Pin (DMIC1 bit = “1”)		
26	AIN1A-	I	Negative Analog Input 1A Pin	AVDD/ VSS1	AVDD
27	AIN1A+	I	Positive Analog Input 1A Pin (DMIC1 bit = “0”)	AVDD/ VSS1	AVDD
	DMDAT1	I	Digital Microphone Data Input 1 Pin (DMIC1 bit = “1”)		
28	MPWR1	O	MIC Power Supply 1 Pin	AVDD/ VSS1	AVDD

Note 2. All input pins except analog input pins (AIN1A+, AIN1A−, AIN1B+, AIN1B−, AIN2A+, AIN2A−, AIN2B+ and AIN2B− pins) should not be left floating.

5.3. Handling of Unused Pin

The unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	MPWR1, MPWR2,	Open
	AIN1A+, AIN1A−, AIN1B+, AIN1B−	Open and DMIC1 bit = “0”
	AIN2A+, AIN2A−, AIN2B+, AIN2B−	Open and DMIC2 bit = “0”
Digital	MCKO, WINTN, SDTO1	Open
	MCKI, TDMIN	Connect to VSS2

5.4. Pin State In Power-down Mode

No.	Pin Name	I/O	Pin Power-down (PDN pin = “L”)	Register Power-down (PDN pin = “H”)
1	CAD	I	Hi-z	←
2	SCL	I	Hi-z	←
3	SDA	I/O	Hi-z	←
4	WINTN	O	Hi-z	“H” (TVDD)
5	SDTO1	O	Pull-down to VSS2 by 49kΩ (typ.)	“L” (VSS2)
6	TDMIN	I	Pull-down to VSS2 by 49kΩ (typ.)	“L” (VSS2)
	SDTO2	O		
7	LRCK	I/O	Pull-down to VSS2 by 49kΩ (typ.)	“L” (VSS2)
8	BCLK	I/O	Pull-down to VSS2 by 49kΩ (typ.)	“L” (VSS2)
9	MCKO	O	Pull-down to VSS2 by 49kΩ (typ.)	“L” (VSS2)
10	MCKI	I	Hi-z	←
11	VDD12	-	Pull-down to VSS2 by 700Ω (typ.)	Normal Operation
12	VSS2	-	-	-
13	TVDD	-	-	-
14	PDN	I	Hi-z	←
15	VREF	O	Hi-z	←
16	VCOM	O	Pull-down to VSS1 by 260Ω (typ.) @AVDD=3.3V Pull-down to VSS1 by 265Ω (typ.) @AVDD=1.8V	←
17	VSS1	-	-	-
18	AVDD	-	-	-
19	MPWR2	O	Hi-z	←
20	AIN2B-	I	Hi-z	←
21	AIN2B+	I	Hi-z	←
	DMCLK2	O		
22	AIN2A-	I	Hi-z	←
23	AIN2A+	I	Hi-z	←
	DMDAT2	I		
24	AIN1B-	I	Hi-z	←
25	AIN1B+	I	Hi-z	←
	DMCLK1	O		
26	AIN1A-	I	Hi-z	←
27	AIN1A+	I	Hi-z	←
	DMDAT1	I		
28	MPWR1	O	Hi-z	←

6. Absolute Maximum Ratings

(VSS1 = VSS2 = 0 V; Note 3, Note 4)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog	AVDD	−0.3	4.3	V
	Digital I/F & LDO12	TVDD	−0.3	4.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 5)		VINA	−0.3	4.3	V
Digital Input Voltage (Note 6)		VIND1	−0.3	TVDD+0.3 or 4.3	V
(Note 7)		VIND2	−0.3	AVDD+0.3	V
Ambient Temperature (powered applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 3. All voltages are with respect to ground.
Note 4. **VSS1 and VSS2 must be connected to the same analog ground plane.**
Note 5. AIN1A+/-, AIN1B+/-, AIN2A+/-, AIN2B+/- pins
Note 6. MCKI, BCLK, LRCK, TDMIN, CAD, SCL, SDA, PDN pins; The maximum value is lower value between “TVDD+0.3V” and “4.3V”.
Note 7. DMDAT1 and DMDAT2 pins

WARNING: Operation beyond these limits may results in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 = VSS2 = 0 V; Note 8)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 9)	Analog	AVDDL	1.7	1.8	1.9	V
		AVDDH	3.0	3.3	3.6	V
	Digital I/F & LDO12	TVDD	1.65	1.8	3.6	V

Note 8. All voltages are with respect to ground.
Note 9. The power-up sequence between AVDD and TVDD is not critical. The PDN pin must be “L” upon power-up, and should be changed to “H” after all power supplies are supplied to avoid an internal circuit error.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in datasheet.

8. Electrical Characteristics

8.1. Microphone & ADC Analog Characteristics (AVDD=3.3V: AVDDL bit = "0")

(Ta = 25°C; AVDD = 3.3V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V; Signal Frequency = 1 kHz; 24-bit Data; fs = 48 kHz, BCLK = 64fs; Measurement Bandwidth = 20 Hz to 20 kHz; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
MIC Amplifier 1/2: AIN1A+/-, AIN1B+/-, AIN2A+/-, AIN2B+/- pins					
Input Resistance		140	200	260	kΩ
MIC-Amp 1/2 Gain					
Gain Setting		0	-	+30	dB
Step Width		2	3	4	dB
MIC Power Supply: MPWR1/2 pins					
Output Voltage (Note 10)	MICL[1:0] bits = "00"	2.6	2.8	3.0	V
	MICL[1:0] bits = "01"	2.3	2.5	2.7	
	MICL[1:0] bits = "10"	1.7	1.8	1.9	
	MICL[1:0] bits = "11"	-	AVDD	-	
Load Resistance		650	-	-	Ω
Load Capacitance		-	-	130	pF
Output Noise Level (A-weighted)	MICL[1:0] bits = "00"	-	–111	-	dBV
	MICL[1:0] bits = "01"	-	–112	-	
	MICL[1:0] bits = "10"	-	–116	-	
PSRR (1kHz) (Note 11)		-	60	-	dB

Note 10. Output voltage setting of microphone power for MPWR1 and MPWR2 is common. The output voltage is proportional to AVDD. MICL[1:0] bits = "00": Typ. 2.8 x AVDD/3.3V, "01": Typ. 2.5 x AVDD/3.3V, "10": Typ. 1.8 x AVDD/3.3V
When MICL[1:0] bits are "11", MPWR1/2 output AVDD via internal switch (Switch ON resistance: Typ. 37Ω, Max. 62Ω).

Note 11. PSRR is referred to all power supplies with 100mVpp sine wave.

Parameter				Min.	Typ.	Max.	Unit
ADC1/2 Analog Input Characteristics: AIN1A+, AIN1B+, AIN2A+, AIN2B+ pins (**Single-ended Input**) → ADC1/2 → SDTO1/2							
Resolution				-	-	32	Bits
Input Full Scale Voltage (Note 12)			0 dB	1.85	2.02	2.18	Vpp
			+18 dB	-	0.255	-	Vpp
THD+N	–1 dBFS	fs = 48 kHz BW = 20 kHz	0 dB	-	–90	-	dB
			+18 dB	-	–86	–78	dB
		fs = 96 kHz BW = 40 kHz	0 dB	-	–90	-	dB
			+18 dB	-	–86	-	dB
		fs = 192 kHz BW = 40 kHz	0 dB	-	–90	-	dB
			+18 dB	-	–86	-	dB
Dynamic Range (–60 dBFS, A-weighted)			0 dB	99	105	-	dB
			+18 dB	-	96	-	dB
S/N (A-weighted)			0 dB	99	105	-	dB
			+18 dB	-	96	-	dB
Interchannel Isolation			0 dB	-	100	-	dB
			+18 dB	80	100	-	dB
Interchannel Gain Mismatch				-	0	0.8	dB
PSRR (1kHz) (Note 13)			0 dB	-	60	-	dB
			+18dB	-	60	-	dB
Spurious Free Dynamic Range (10kHz) (Note 14)			0 dB	-	100	-	dBc
			+18dB	-	100	-	dBc
ADC1/2 Analog Input Characteristics: AIN1A+/-, AIN1B+/-, AIN2A+/-, AIN2B+/- pins (**Differential Input**) → ADC1/2 → SDTO1/2							
Resolution				-	-	32	Bits
Input Full Scale Voltage (Note 12)			0 dB	1.85	2.02	2.18	Vpp
			+18 dB	-	0.255	-	Vpp
THD+N	–1 dBFS	fs = 48 kHz BW = 20 kHz	0 dB	-	–90	-	dB
			+18 dB	-	–86	-	dB
		fs = 96 kHz BW = 40 kHz	0 dB	-	–90	-	dB
			+18 dB	-	–86	-	dB
		fs = 192 kHz BW = 40 kHz	0 dB	-	–90	-	dB
			+18 dB	-	–86	-	dB
Dynamic Range (–60 dBFS, A-weighted)			0 dB	-	105	-	dB
			+18 dB	-	96	-	dB
S/N (A-weighted)			0 dB	-	105	-	dB
			+18 dB	-	96	-	dB
Interchannel Isolation			0 dB	-	100	-	dB
			+18 dB	-	100	-	dB
Interchannel Gain Mismatch				-	0	-	dB
PSRR (1kHz) (Note 13)			0 dB	-	60	-	dB
			+18dB	-	60	-	dB
Spurious Free Dynamic Range (10kHz) (Note 14)			0 dB	-	100	-	dBc
			+18dB	-	100	-	dBc

Note 12. Input voltage is proportional to AVDD. Typ. 2.02 Vpp x AVDD/3.3V @ MIC-Amp Gain = 0 dB

Note 13. PSRR is referred to all power supplies with 100mVpp sine wave. It is the ratio based on 100mVpp (= –26.1dBFS) at the ADC output.

Note 14. SFDR is referred to AVDD with 100mVpp sine wave. It is the dynamic range based on full scale (0 dBFS) at the ADC output.

8.2. Microphone & ADC Analog Characteristics (AVDD=1.8V: AVDDL bit = “1”)

(Ta = 25°C; AVDD = 1.8V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V; Signal Frequency = 1 kHz; 24-bit Data; fs = 48 kHz, BCLK = 64fs; Measurement Bandwidth = 20 Hz to 20 kHz; unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
MIC Amplifier 1/2: AIN1A+/-, AIN1B+/-, AIN2A+/-, AIN2B+/- pins						
Input Resistance			140	200	260	kΩ
MIC-Amp 1/2 Gain						
	Gain Setting		0	-	+30	dB
	Step Width		2	3	4	dB
MIC Power Supply: MPWR1/2 pins						
Output Voltage (Note 15)		“11”	-	AVDD	-	V

Note 15. Output voltage setting of microphone power for MPWR1 and MPWR2 is common. The setting of MICL[1:0] bits = "11" is only available.
When MICL[1:0] bits are “11”, MPWR1/2 output AVDD via internal switch (Switch ON resistance: Typ. 37Ω, Max. 62Ω).

Parameter				Min.	Typ.	Max.	Unit
ADC1/2 Analog Input Characteristics: AIN1A+, AIN1B+, AIN2A+, AIN2B+ pins (**Single-ended Input**) → ADC1/2 → SDTO1/2							
Resolution				-	-	32	Bits
Input Full Scale Voltage (Note 16)			0 dB	1.01	1.10	1.19	Vpp
			+18 dB	-	0.139	-	Vpp
THD+N	−1 dBFS	fs = 48 kHz BW = 20 kHz	0 dB	-	−80	-	dB
			+18 dB	-	−80	−72	dB
		fs = 96 kHz BW = 40 kHz	0 dB	-	−80	-	dB
			+18 dB	-	−80	-	dB
		fs = 192 kHz BW = 40 kHz	0 dB	-	−80	-	dB
			+18 dB	-	−80	-	dB
Dynamic Range (−60 dBFS, A-weighted)			0 dB	95	101	-	dB
			+18 dB	-	91	-	dB
S/N (A-weighted)			0 dB	95	101	-	dB
			+18 dB	-	91	-	dB
Interchannel Isolation			0 dB	-	100	-	dB
			+18 dB	80	100	-	dB
Interchannel Gain Mismatch				-	0	0.8	dB
PSRR (1kHz) (Note 17)			0 dB	-	60	-	dB
			+18dB	-	60	-	dB
Spurious Free Dynamic Range (10kHz) (Note 18)			0 dB	-	80	-	dBc
			+18dB	-	80	-	dBc
ADC1/2 Analog Input Characteristics: AIN1A+/-, AIN1B+/-, AIN2A+/-, AIN2B+/- pins (**Differential Input**) → ADC1/2 → SDTO1/2							
Resolution				-	-	32	Bits
Input Full Scale Voltage (Note 16)			0 dB	1.01	1.10	1.19	Vpp
			+18 dB	-	0.139	-	Vpp
THD+N	−1 dBFS	fs = 48 kHz BW = 20 kHz	0 dB	-	−80	-	dB
			+18 dB	-	−80	-	dB
		fs = 96 kHz BW = 40 kHz	0 dB	-	−80	-	dB
			+18 dB	-	−80	-	dB
		fs = 192 kHz BW = 40 kHz	0 dB	-	−80	-	dB
			+18 dB	-	−80	-	dB
Dynamic Range (−60 dBFS, A-weighted)			0 dB	-	101	-	dB
			+18 dB	-	91	-	dB
S/N (A-weighted)			0 dB	-	101	-	dB
			+18 dB	-	91	-	dB
Interchannel Isolation			0 dB	-	100	-	dB
			+18 dB	-	100	-	dB
Interchannel Gain Mismatch				-	0	-	dB
PSRR (1kHz) (Note 17)			0 dB	-	60	-	dB
			+18dB	-	60	-	dB
Spurious Free Dynamic Range (10kHz) (Note 18)			0 dB	-	80	-	dBc
			+18dB	-	80	-	dBc

Note 16. Input voltage is proportional to AVDD. Typ. 1.10 Vpp x AVDD/1.8V @ MIC-Amp Gain = 0 dB

Note 17. PSRR is referred to all power supplies with 100mVpp sine wave. It is the ratio based on 100mVpp (= −20.8dBFS) at the ADC output.

Note 18. SFDR is referred to AVDD with 100mVpp sine wave. It is the dynamic range based on full scale (0 dBFS) at the ADC output.

8.3. Power Supply Current

(Ta = 25°C; AVDD = 3.3V or 1.8V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V; unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit
Power Supply Current				
Power Up (PDN pin = "H", All circuits power-up, Note 19)				
AVDD (AVDD=3.3V: AVDDL bit = "0")	-	7.0	9.8	mA
AVDD (AVDD=1.8V: AVDDL bit = "1")	-	5.3	-	mA
TVDD	-	2.4	3.4	mA
Power Up (PDN pin = "H", LDO12 Enable, Other circuits power-down)				
AVDD (AVDD=3.3V: AVDDL bit = "0")	-	0.05	-	mA
AVDD (AVDD=1.8V: AVDDL bit = "1")	-	0.05	-	mA
TVDD	-	0.15	-	mA
Power Down (PDN pin = "L", Note 20)				
AVDD + TVDD	-	4	20	μA

Note 19. PLL Master Mode, MCKI=16MHz, BCLK=64fs, fs=48kHz (PLD[15:0] bits = 0018H, PLM[15:0] bits = 005FH, FS[3:0] bits = "1010", CM[1:0] bits = "01", PLS bit = "0", MSN = BCKO = MCKOE bit = "1"); All PMxx bits except PMDMxx bits are powered up.; MICL[1:0] bits = "00" @AVDD=3.3V, MICL[1:0] bits = "11" @AVDD=1.8V; No signal input

Note 20. All digital input pins are fixed to each power supply pin, TVDD or VSS2.

8.4. Power Consumption for Each Operation Mode

(Ta = 25°C; AVDD = 3.3V or 1.8V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V; External Slave Mode, MCKI = 256 fs, BCLK = 64fs; No signal input, MPWR OFF)

Mode	AVDD [mA]		TVDD [mA]	Total Power [mW]
AIN1/2 → 2-ch ADC (fs = 48 kHz)	3.3V	2.4	1.0	9.7
	1.8V	2.0		5.4
AIN1/2 → 2-ch ADC (fs = 96 kHz)	3.3V	4.4	1.8	17.8
	1.8V	3.7		9.9
AIN1/2 → 2-ch ADC (fs = 192 kHz)	3.3V	4.4	1.8	17.8
	1.8V	3.7		9.9
AIN1/2 → 4-ch ADC (fs = 48 kHz)	3.3V	4.5	1.2	17.0
	1.8V	4.0		9.4
AIN1/2 → 4-ch ADC (fs = 96 kHz)	3.3V	8.4	2.2	31.7
	1.8V	7.1		16.7
AIN1/2 → 4-ch ADC (fs = 192 kHz, MCKI=128fs)	3.3V	8.4	2.2	31.7
	1.8V	7.1		16.7
Voice Activity Detection Mode (AIN1A → 1-ch ADC → VAD, fs = 16kHz)	3.3V	1.2	0.5	4.9
	1.8V	1.0		2.7

8.5. ADC1/2 Short Delay Sharp Roll-off Filter (ADVF bit = "0")

<fs = 48 kHz>

(Ta = –40 to 85°C; AVDD = 1.7 to 1.9V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; fs = 48kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 21)	±0.16 dB	PB	0	-	18.8	kHz
	–0.28 dB		-	20.0	-	kHz
	–3.0 dB		-	22.8	-	kHz
Stopband (Note 21)		SB	28.4	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 22)		GD	-	5.0	-	1/fs
Group Delay Distortion		ΔGD	-	-	2.4	1/fs
ADC Digital Filter (HPF): HPFxC[1:0] bits = "00" (x=1, 2)						
Frequency Response (Note 21)	–3.0 dB	FR	-	3.7	-	Hz

Note 21. The passband and stopband frequencies scale with fs (sampling frequency). Each response refers to that of 1kHz.

Note 22. This time is from the input of an analog signal to the A channel MSB output timing of SDTO1/2. This time includes group delay of the HPF. The error of the delay at audio interface is within +1/8 [1/fs]. For the signal through the programmable filters, the group delay is increased by 1/fs.

<fs = 96 kHz>

(Ta = –40 to 85°C; AVDD = 1.7 to 1.9V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; fs = 96kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 21)	±0.16 dB	PB	0	-	37.6	kHz
	–0.28 dB		-	40.0	-	kHz
	–3.0 dB		-	45.6	-	kHz
Stopband (Note 21)		SB	56.8	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 22)		GD	-	5.0	-	1/fs
Group Delay Distortion		ΔGD	-	-	2.4	1/fs
ADC Digital Filter (HPF): HPFxC[1:0] bits = "00" (x=1, 2)						
Frequency Response (Note 21)	–3.0 dB	FR	-	7.4	-	Hz

<fs = 192 kHz>

(Ta = –40 to 85°C; AVDD = 1.7 to 1.9V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; fs = 192kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 21)	±0.12 dB	PB	0	-	37	kHz
	–1.0 dB		-	51	-	kHz
	–3.0 dB		-	65	-	kHz
	–6.0 dB		-	78	-	kHz
Stopband (Note 21)		SB	145.5	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 22)		GD	-	4.4	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
ADC Digital Filter (HPF): HPFxC[1:0] bits = "00" (x=1, 2)						
Frequency Response (Note 21)	–3.0 dB	FR	-	14.8	-	Hz

8.6. ADC1/2 Digital Filter for Voice (ADVF bit = "1")

<fs=8kHz>

(Ta = –40 to 85°C; AVDD = 1.7 to 1.9V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; fs = 8kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Voice Digital Filter						
Passband (Note 21)	-0.5dB to 0.5dB -3.0dB	PB	0 -	- 3.35	3.15 -	kHz kHz
Stopband (Note 21)		SB	4.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay (Note 22)		GD	-	15.2	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
ADC Digital Filter (HPF): HPFxC[1:0] bits = "00" (x=1, 2)						
Frequency Response (Note 21)	-3.0dB	FR	-	0.6	-	Hz

<fs=16kHz>

(Ta = –40 to 85°C; AVDD = 1.7 to 1.9V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; fs = 16kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Voice Digital Filter						
Passband (Note 21)	-0.5dB to 0.5dB -3.0dB	PB	0 -	- 6.7	6.3 -	kHz kHz
Stopband (Note 21)		SB	8.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay (Note 22)		GD	-	15.2	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
ADC Digital Filter (HPF): HPFxC[1:0] bits = "00" (x=1, 2)						
Frequency Response (Note 21)	-3.0dB	FR	-	1.2	-	Hz

8.7. DC Characteristics

(Ta = −40 to 85°C; AVDD = 1.7 to 1.9V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Normal Pin (Note 23)					
High-Level Input Voltage	VIH	70% TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30% TVDD	V
High-Level Output Voltage (Iout = −200 µA)	VOH	TVDD −0.2	-	-	V
Low-Level Output Voltage					
Except for SDA pin, Iout = 200 µA	VOL	-	-	0.2	V
SDA pin					
2 V < TVDD ≤ 3.6 V (Iout = 3 mA)	VOL	-	-	0.4	V
1.65 V ≤ TVDD ≤ 2 V (Iout = 2 mA)	VOL	-	-	20% TVDD	V
Input Leakage Current (Note 24)	Iin	−5	-	+5	µA
Digital MIC Interface (DMDAT1/2 pin Input)					
High-Level Input Voltage	VIH2	65% AVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	35% AVDD	V
Digital MIC Interface (DMCLK1/2 pin Output)					
High-Level Output Voltage (Iout = −80 µA)	VOH2	AVDD −0.4	-	-	V
Low-Level Output Voltage (Iout = 80 µA)	VOL2	-	-	0.4	V
Input Leakage Current	Iin	−5	-	+5	µA

Note 23. MCKI, MCKO, BLK, LRCK, TDMIN/SDTO2, SDTO1, CAD, SCL, SDA, PDN, WINTN pins
Note 24. PSW1N = PSW2N bits = “1“

8.8. Switching Characteristics

(Ta = −40 to 85°C; AVDD = 1.7 to 1.9V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; C_L = 50 pF(MCKO, BCLK, LRCK pins), 20 pF(SDTO1, SDTO2 pins); unless otherwise specified)

<System Clock>

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Input Timing					
Input Frequency	fMCK	0.256	-	27	MHz
Pulse Width Low	tMCKL	0.4 / fMCK	-	-	ns
Pulse Width High	tMCKH	0.4 / fMCK	-	-	ns
Master Clock Output Timing					
Output Frequency	fMCKO	-	-	24.576	MHz
Duty Cycle (Note 25)	dMCKO	-	50	-	%
LRCK Frequency (Slave mode)					
Normal mode (TDM[1:0] bits = "00")					
Frequency	fs	8	-	192	kHz
Duty Cycle	Duty	45	-	55	%
TDM128 mode (TDM[1:0] bits = "01")					
Frequency	fs	8	-	192	kHz
High Time	tLRH	1/128fs	-	-	ns
Low Time	tLRL	1/128fs	-	-	ns
TDM256 mode (TDM[1:0] bits = "10")					
Frequency	fs	8	-	96	kHz
High time	tLRH	1/256fs	-	-	ns
Low time	tLRL	1/256fs	-	-	ns
TDM512 mode (TDM[1:0] bits = "11")					
Frequency	fs	8	-	48	kHz
High Time	tLRH	1/512fs	-	-	ns
Low Time	tLRL	1/512fs	-	-	ns
BCLK Frequency (Slave mode)					
Normal mode (TDM[1:0] bits = "00")					
Frequency (Note 26)	1/tBCK	32fs	-	24.576M or 512fs	Hz
BCLK Pulse Width Low	tBCKL	32	-	-	ns
BCLK Pulse Width High	tBCKH	32	-	-	ns
TDM128 mode (TDM[1:0] bits = "01")					
Frequency	1/tBCK	-	128fs	-	Hz
BCLK Pulse Width Low	tBCKL	16	-	-	ns
BCLK Pulse Width High	tBCKH	16	-	-	ns
TDM256 mode (TDM[1:0] bits = "10")					
Frequency	1/tBCK	-	256fs	-	Hz
BCLK Pulse Width Low	tBCKL	16	-	-	ns
BCLK Pulse Width High	tBCKH	16	-	-	ns
TDM512 mode (TDM[1:0] bits = "11")					
Frequency	1/tBCK	-	512fs	-	Hz
BCLK Pulse Width Low	tBCKL	16	-	-	ns
BCLK Pulse Width High	tBCKH	16	-	-	ns

Note 25. Divided by an even number.

Note 26. The maximum value is slower frequency between "24.576MHz" and "512fs".

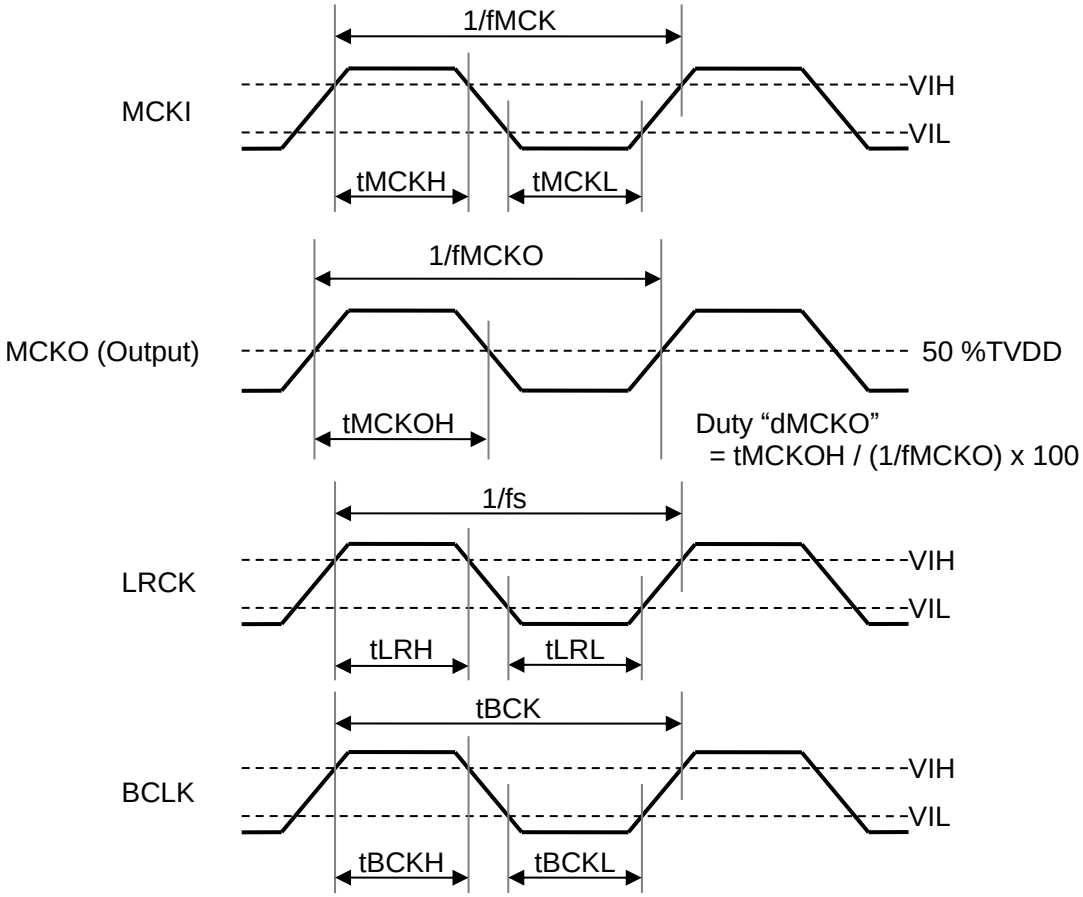


Figure 2. System Clock (Slave Mode)

<System Clock (Master mode)>

Parameter	Symbol	Min.	Typ.	Max.	Unit
LRCK Frequency (Master mode)					
Normal mode (TDM[1:0] bits = "00")					
Frequency	fs	8	-	192	kHz
Duty Cycle	Duty	-	50	-	%
TDM128 mode (TDM[1:0] bits = "01")					
Frequency	fs	8	-	192	kHz
High Time	tLRH	-	1/4fs	-	ns
TDM256 mode (TDM[1:0] bits = "10")					
Frequency	fs	8	-	96	kHz
High Time	tLRH	-	1/8fs	-	ns
TDM512 mode (TDM[1:0] bits = "11")					
Frequency	fs	8	-	48	kHz
High Time	tLRH	-	1/16fs	-	ns
BCLK Frequency (Master mode)					
Normal mode (TDM[1:0] bits = "00")					
Frequency (BCKO bit = "0")	1/tBCK	-	32fs	-	Hz
(BCKO bit = "1")	1/tBCK	-	64fs	-	Hz
BCLK Duty	dBCK	-	50	-	%
TDM128 mode (TDM[1:0] bits = "01")					
Frequency	1/tBCK	-	128fs	-	Hz
BCLK Duty	dBCK	-	50	-	%
TDM256 mode (TDM[1:0] bits = "10")					
Frequency	1/tBCK	-	256fs	-	Hz
BCLK Duty	dBCK	-	50	-	%
TDM512 mode (TDM[1:0] bits = "11")					
Frequency	1/tBCK	-	512fs	-	Hz
BCLK Duty	dBCK	-	50	-	%

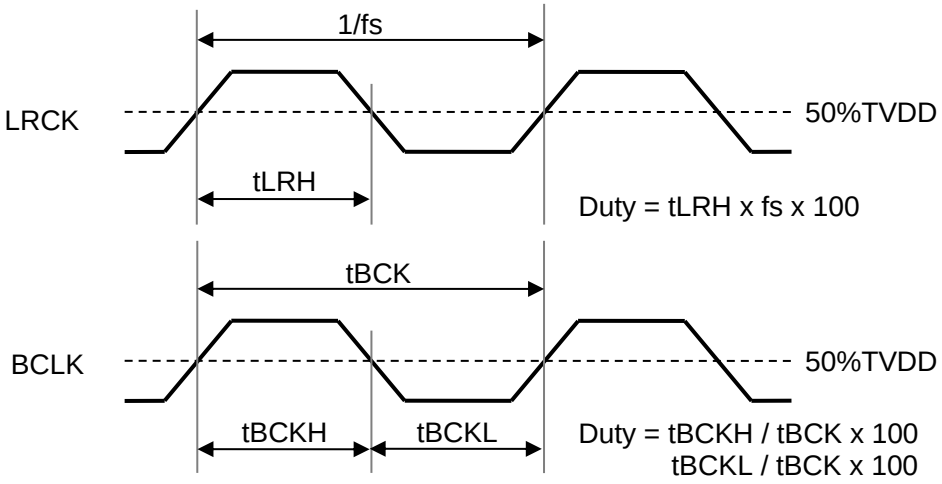


Figure 3.System Clock (Master Mode)

<Audio Interface (Slave mode)>

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Slave mode)					
Normal mode (TDM[1:0] bits = "00", DIF1 bit = "0")					
LRCK Edge to BCLK "↑" (Note 27)	tLRB	25	-	-	ns
BCLK "↑" to LRCK Edge (Note 27)	tBLR	25	-	-	ns
LRCK to SDTO (MSB) (Except I²S Mode)	tLRS	-	-	25	ns
BCLK "↓" to SDTO1/2 (Note 28)	tBSD	-	-	25	ns
PCM mode (TDM[1:0] bits = "00" , DIF1 bit = "1")					
LRCK Edge to BCLK "↑" (Note 27)	tLRB	25	-	-	ns
BCLK "↑" to LRCK Edge (Note 27)	tBLR	25	-	-	ns
BCLK "↑" to SDTO1/2 (Note 27)	tBSDD	5	-	35	ns
TDM128 mode (TDM[1:0] bits = "01")					
LRCK Edge to BCLK "↑" (Note 27)	tLRB	16	-	-	ns
BCLK "↑" to LRCK Edge (Note 27)	tBLR	16	-	-	ns
BCLK "↑" to SDTO1 (Note 27)	tBSDD	5	-	35	ns
TDMIN Hold Time	tSDH	5	-	-	ns
TDMIN Setup Time	tSDS	5	-	-	ns
TDM256 mode (TDM[1:0] bits = "10")					
LRCK Edge to BCLK "↑" (Note 27)	tLRB	16	-	-	ns
BCLK "↑" to LRCK Edge (Note 27)	tBLR	16	-	-	ns
BCLK "↑" to SDTO1 (Note 27)	tBSDD	5	-	35	ns
TDMIN Hold Time	tSDH	5	-	-	ns
TDMIN Setup Time	tSDS	5	-	-	ns
TDM512 mode (TDM[1:0] bits = "11")					
LRCK Edge to BCLK "↑" (Note 27)	tLRB	16	-	-	ns
BCLK "↑" to LRCK Edge (Note 27)	tBLR	16	-	-	ns
BCLK "↑" to SDTO1 (Note 27)	tBSDD	5	-	35	ns
TDMIN Hold Time	tSDH	5	-	-	ns
TDMIN Setup Time	tSDS	5	-	-	ns

Note 27. When the polarity of BCLK is inverted, delay time starts from BCLK "↓".
Note 28. When the polarity of BCLK is inverted, delay time starts from BCLK "↑".

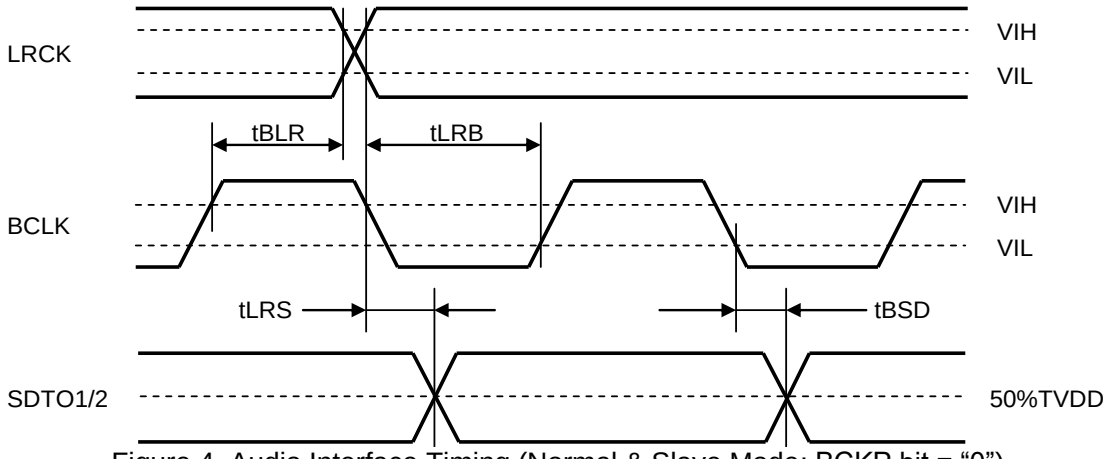


Figure 4. Audio Interface Timing (Normal & Slave Mode: BCKP bit = "0")

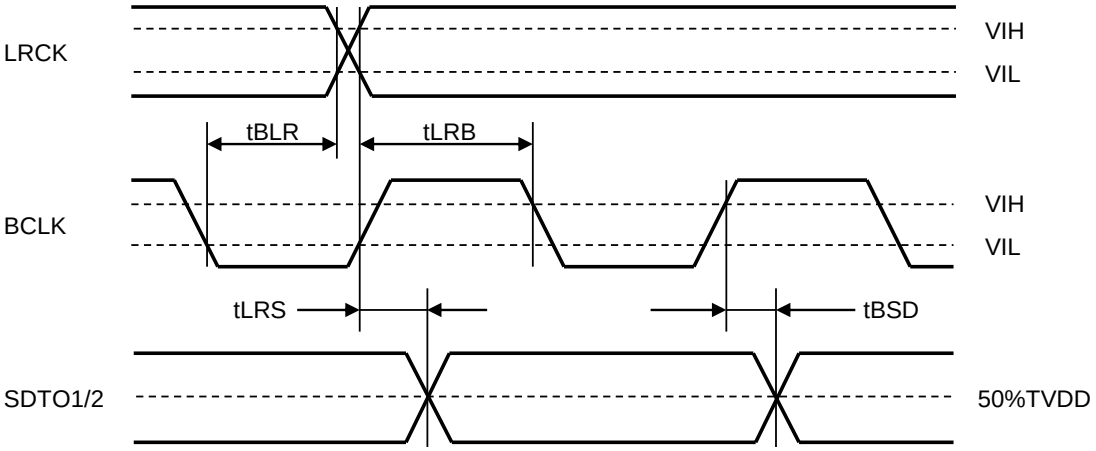


Figure 5. Audio Interface Timing (Normal & Slave Mode: BCKP bit = “1”)

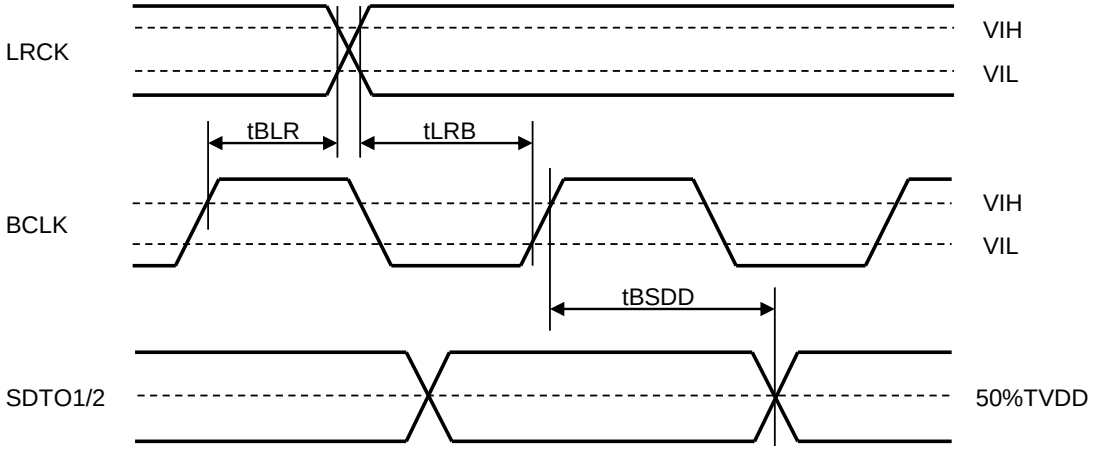


Figure 6. Audio Interface Timing (PCM & Slave Mode: BCKP bit = “0”)

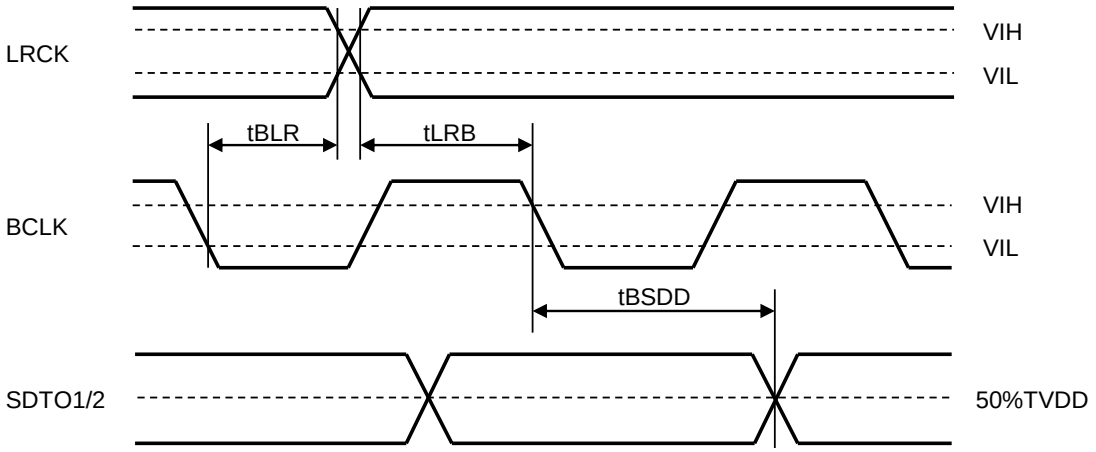


Figure 7. Audio Interface Timing (PCM & Slave Mode: BCKP bit = “1”)

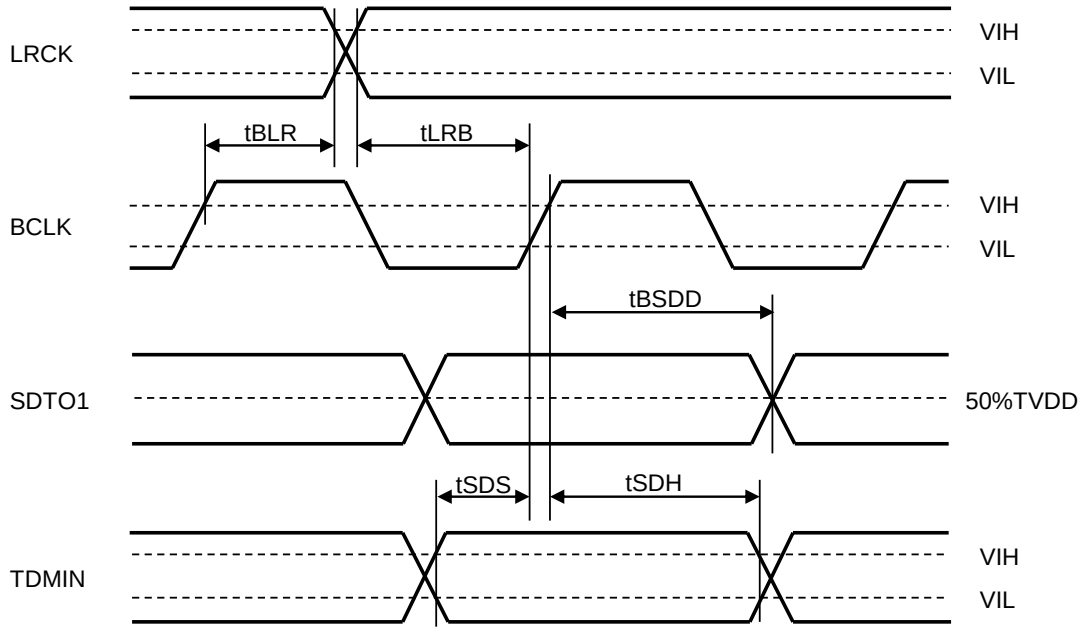


Figure 8. Audio Interface Timing (TDM & Slave mode: BCKP bit = “0”)

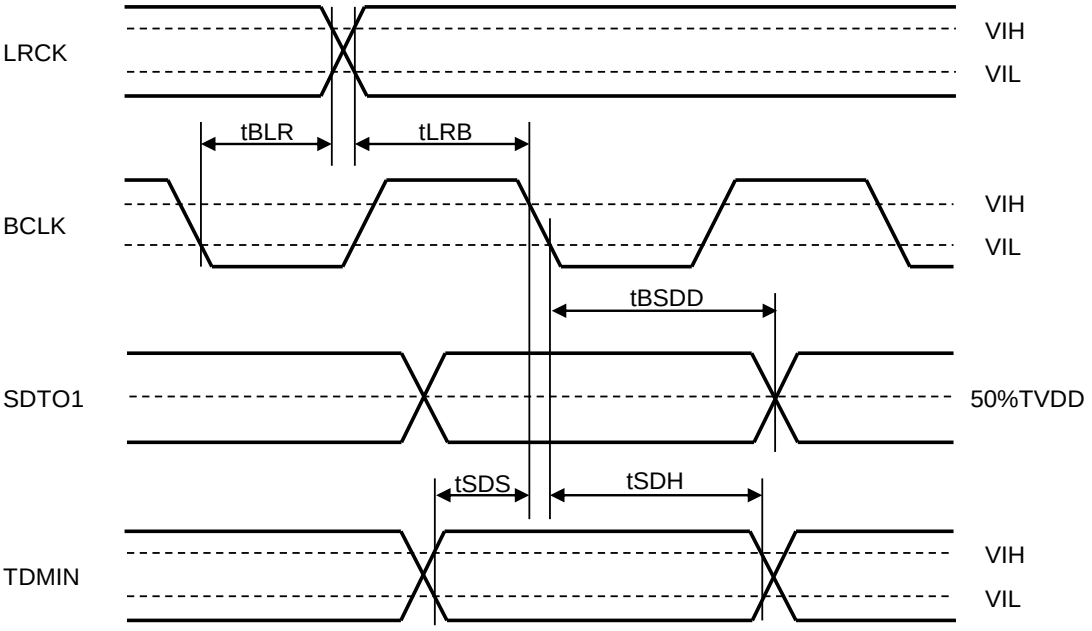


Figure 9. Audio Interface Timing (TDM & Slave Mode: BCKP bit = “1”)

<Audio Interface (Master mode)>

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Master mode)					
Normal mode (TDM[1:0] bits = "00")					
BCLK "↓" to LRCK Edge (Note 29)	tMBLR	–20	-	20	ns
BCLK "↓"to SDTO1/2 (Note 29)	tBSD	–20	-	20	ns
TDM128 mode (TDM[1:0] bits = "01")					
BCLK "↓" to LRCK Edge (Note 29)	tMBLR	–10	-	10	ns
BCLK "↓" to SDTO1/2 (Note 29)	tBSD	–10	-	10	ns
TDMIN Hold Time	tSDH	5	-	-	ns
TDMIN Setup Time	tSDS	5	-	-	ns
TDM256 mode (TDM[1:0] bits = "10")					
BCLK "↓" to LRCK Edge (Note 29)	tMBLR	–10	-	10	ns
BCLK "↓" to SDTO1 (Note 29)	tBSD	–10	-	10	ns
TDMIN Hold Time	tSDH	5	-	-	ns
TDMIN Setup Time	tSDS	5	-	-	ns
TDM512 mode (TDM[1:0] bits = "11")					
BCLK "↓" to LRCK Edge (Note 29)	tMBLR	–10	-	10	ns
BCLK "↓" to SDTO1 (Note 29)	tBSD	–10	-	10	ns
TDMIN Hold Time	tSDH	5	-	-	ns
TDMIN Setup Time	tSDS	5	-	-	ns

Note 29. When the polarity of BCLK is inverted, delay time starts from BCLK "↑".

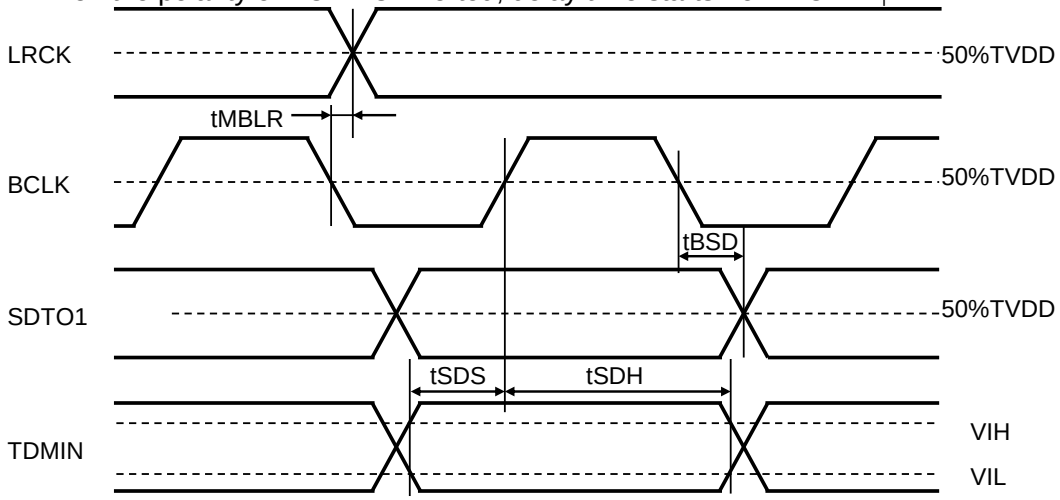


Figure 10. Audio Interface Timing (Master mode: BCKP bit = "0")

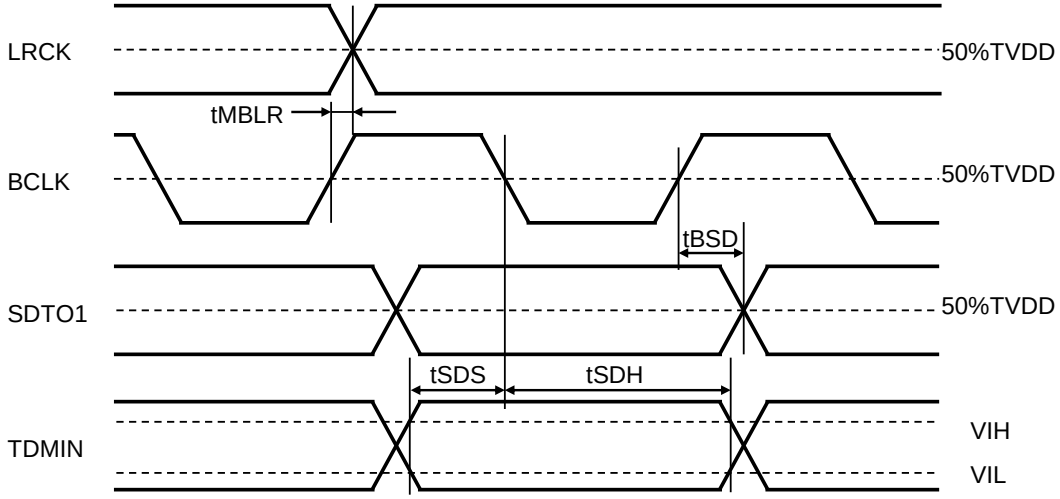
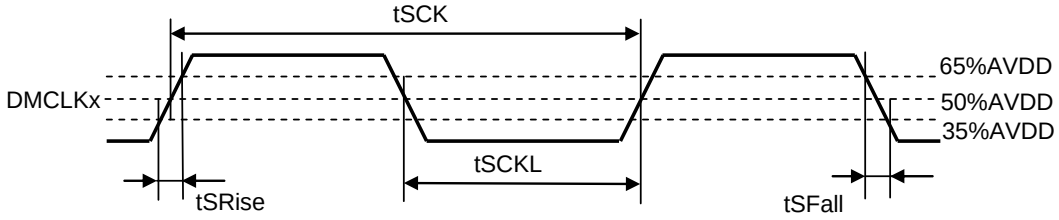


Figure 11. Audio Interface Timing (Master mode: BCKP bit = "1")

<Digital Mic Interface>

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital Audio Interface Timing: C_L = 100 pF					
DMCLK1/2 Output Timing					
Period	tSCK	-	1/(64fs)	-	ns
Rising Time	tSRise	-	-	10	ns
Falling Time	tSFall	-	-	10	ns
Duty Cycle	dSCK	45	50	55	%
Audio Interface Timing (DMCLK1/2, DMDAT1/2 pins)					
DMDAT1/2 Setup Time	tDMS	50	-	-	ns
DMDAT1/2 Hold Time	tDMH	0	-	-	ns



dSCK = 100 x tSCKL / tSCK

Figure 12. DMCLK1/2 Output Timing

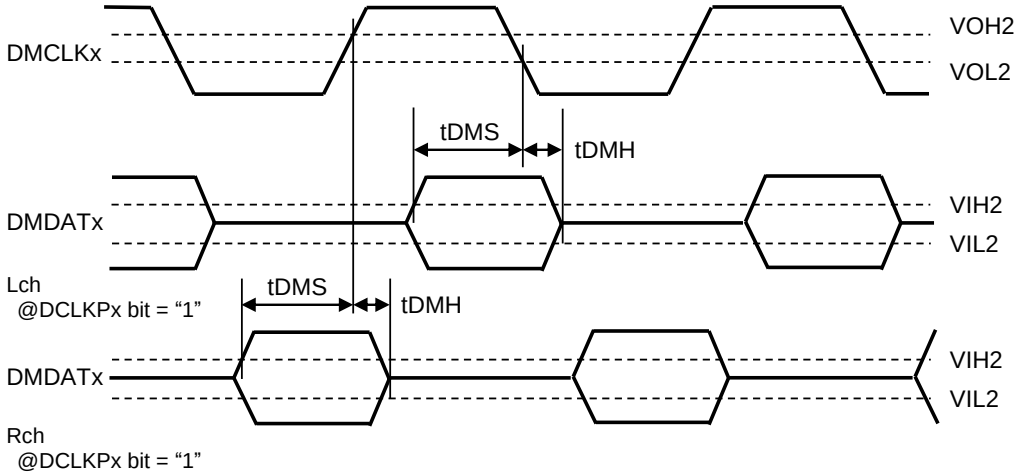


Figure 13. Audio Interface Timing

<I²C-bus: Fast Mode>

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing: (Note 30)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 31)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 30. I²C-bus is a registered trademark of NXP B.V.

Note 31. Data must be held long enough to bridge the 300ns-transition time of SCL.

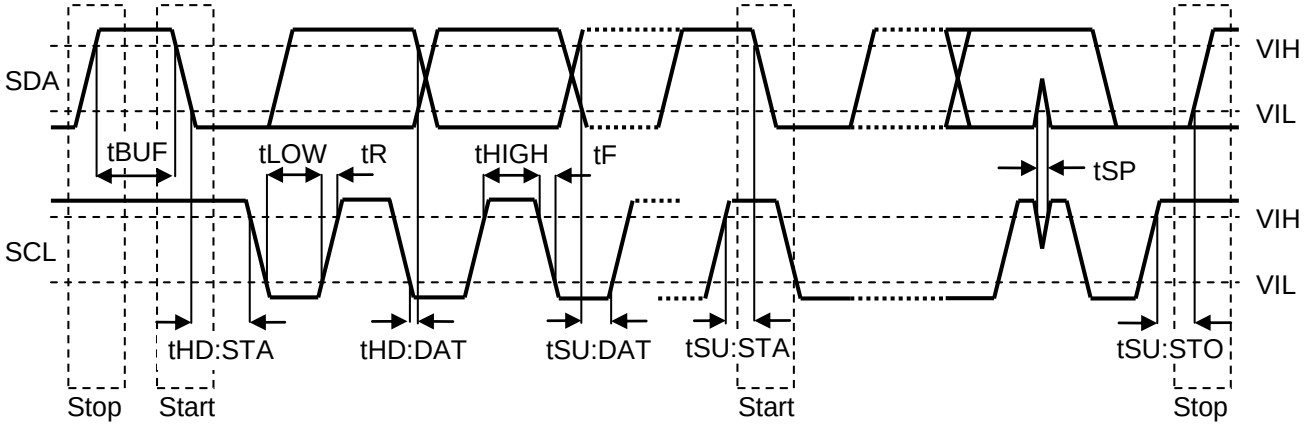


Figure 14. I²C Bus Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 32)	tPDN	1	-	-	ms
PDN Reject Pulse Width (Note 32)	tRPD	-	-	50	ns
PMADxA/B bit = “1” to SDTOx valid (Note 33)					
ADRST[2:0] bits = “000”	tPDV	-	1059	-	1/fs
ADRST[2:0] bits = “001”	tPDV	-	267	-	1/fs
ADRST[2:0] bits = “010”	tPDV	-	2115	-	1/fs
ADRST[2:0] bits = “011”	tPDV	-	531	-	1/fs
ADRST[2:0] bits = “100”	tPDV	-	4230	-	1/fs
ADRST[2:0] bits = “101”	tPDV	-	8	-	1/fs
ADRST[2:0] bits = “110”	tPDV	-	16	-	1/fs
ADRST[2:0] bits = “111”	tPDV	-	32	-	1/fs
PMDMxA/B bit = “1” to SDTOx valid (Note 34)					
ADRST[2:0] bits = “000”	tPDV	-	1059	-	1/fs
ADRST[2:0] bits = “001”	tPDV	-	267	-	1/fs
ADRST[2:0] bits = “010”	tPDV	-	2115	-	1/fs
ADRST[2:0] bits = “011”	tPDV	-	531	-	1/fs
ADRST[2:0] bits = “100”	tPDV	-	4230	-	1/fs
ADRST[2:0] bits = “101”	tPDV	-	8	-	1/fs
ADRST[2:0] bits = “110”	tPDV	-	16	-	1/fs
ADRST[2:0] bits = “111”	tPDV	-	32	-	1/fs

Note 32. The PDN pin must held “L” for longer period the or equal to tPDN period. The AK5704 will not be reset by the “L” pulse shorter than or equal to 50nsec.
Note 33. This is the count of LRCK “↑” from PMADxA/B bit = “1”.
Note 34. This is the count of LRCK “↑” from PMDMxA/B bit = “1”.

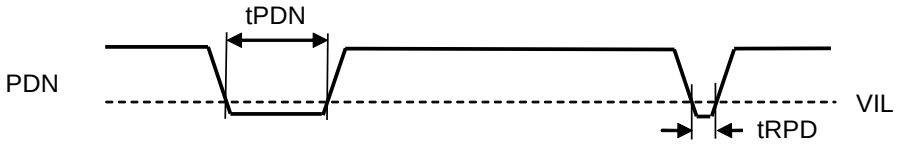


Figure 15. Power Down & Standby

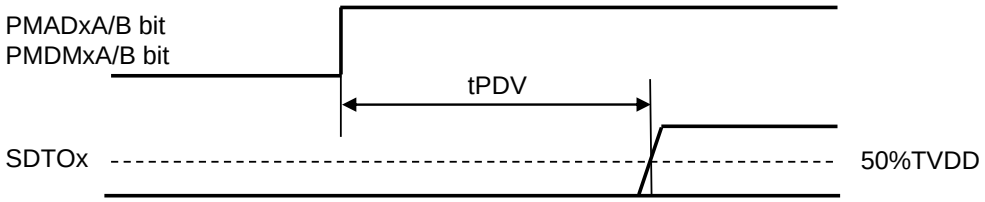


Figure 16. ADC1/2, DMIC1/2 Power Up Timing

9. Functional Descriptions

9.1. Internal Pull-down Pin

When the PDN pin = “H”, digital pins shown in Table 1 can set internal pull-down resistor to ON/OFF by PSW0N, PSW1N, PSW2N bits. The pull-down resistor is ON and the control register is “0” at default setting. The pull-down resistor setting should be made according to external conditions.

Table 1. Internal Pull-down Pin

Pin Name	I/O	Power Domain	Control bit (Note 35)
CAD	I	TVDD	-
SCL	I	TVDD	-
SDA	I/O	TVDD	-
MCKI	I	TVDD	-
MCKO	O	TVDD	PSW0N
BCLK	I/O	TVDD	PSW1N
LRCK	I/O	TVDD	PSW1N
TDMIN/SDTO2	I/O	TVDD	PSW2N
SDTO1	O	TVDD	PSW0N
PDN	I	TVDD	-
WINTN	O	TVDD	-

Pin Name	I/O	Power Domain	Control bit (Note 35)
DMCLK1	O	AVDD	-
DMDAT1	I	AVDD	-
DMCLK2	O	AVDD	-
DMDAT2	I	AVDD	-

Note 35. “-”: There is no pull-down resistor.

9.2. LDO Circuit

The PDN pin must be “L” upon power-up, and should be changed to “H” after all power supplies are supplied. Then LDO12 will be powered up.

LDO12 has an overvoltage protection circuit. This overvoltage protection circuit powers the LDO12 down when the power supply becomes unstable by an instantaneous power failure, etc. during operation. The LDO12 circuit will not return to normal operation until being reset by the PDN pin (“L” → “H”) after removing the problems.

9.3. System Clock

The AK5704 is operated by a clock generated by PLL or MCKI supplied from external. MCKI frequency will be 128fs, 256fs, 512fs or 1024fs. The master clock is set by CM[1:0] bits (Table 3) and the sampling frequency is set by FS[3:0] bits (Table 4). When changing the master clock or sampling frequency, set PMAD1A/B = PMAD2A/B = PMDM1A/B = PMDM2A/B bits = "0" and VREF bit = "1". If the clock is stopped at PMADx bit = "1", VREF bit should be set to "1".

Table 2. Clock Mode Setting (x: Do not care, N/A: Not available)

Mode	PMPLL bit	MSN bit	PLS bit	MCKI pin	BCLK pin	LRCK pin	MCKOE bit	MCKO pin
PLL Master Mode	1	1	0	Input (Table 10, Table 11, Table 12, Table 13)	Output (Table 6)	Output (Table 4)	0	"L" Output
							1	Output (Table 5)
PLL Slave Mode (Clock Source: MCKI pin)	1	0	0	Input (Table 10, Table 11, Table 12, Table 13)	Input (≥ 32fs)	Input (Table 4)	1	Output (Table 5)
PLL Slave Mode (Clock Source: BCLK pin)	1	0	1	GND	Input (Table 14, Table 15)	Input (Table 4)	0	"L" Output
							1	Output (Table 5)
EXT Master Mode	0	1	x	Input (Table 3)	Output (Table 6)	Output (Table 4)	0	"L" Output
							1	N/A
EXT Slave Mode	0	0	x	Input (Table 3)	Input (≥ 32fs)	Input (Table 4)	0	"L" Output
							1	N/A

Table 3. Setting of Master Clock Frequency

CM[1:0] bits	Master Clock Frequency	Sampling Frequency Range	
00	256fs	8 to 96 kHz	(default)
01	512fs	8 to 48 kHz	
10	1024fs	8 to 24 kHz	
11	128fs	176.4 to 192 kHz	

Table 4. Setting of Sampling Frequency (N/A: Not available)

FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	8 kHz	
0	0	0	1	11.025 kHz	
0	0	1	0	12 kHz	
0	0	1	1	N/A	
0	1	0	0	16 kHz	
0	1	0	1	22.05 kHz	
0	1	1	0	24 kHz	
0	1	1	1	N/A	
1	0	0	0	32 kHz	
1	0	0	1	44.1 kHz	
1	0	1	0	48 kHz	(default)
1	0	1	1	N/A	
1	1	0	0	88.2 kHz	
1	1	0	1	96 kHz	
1	1	1	0	176.4 kHz	
1	1	1	1	192 kHz	

Note 36. Sampling frequency has an error according to PLL division ratio. PLD[15:0], PLM[15:0] bits should be set with accuracy.

9.4. PLL

The built-in PLL generates master clock for internal operation from the clock source input to the MCKI pin or the BCLK pin. PLL starts to operate when PMPLL bit = "1".

1. PLL Output Frequency (MCKO pin)

The PLL generates master clock for internal operation and outputs frequency below from the MCKO pin.

Table 5. MCKO Output

CM[1:0] bits	MCKO pin		Sampling Frequency Range	
	MCKOE bit = "0"	MCKOE bit = "1"		
00	"L" Output	256fs	8 to 96 kHz	(default)
01	"L" Output	512fs	8 to 48 kHz	
10	"L" Output	1024fs	8 to 24 kHz	
11	"L" Output	128fs	176.4 to 192 kHz	

Note 37. When CM[1:0] bits = "01", fs=32kHz is not available. When CM[1:0] bits = "10", fs=16kHz is not available.

2. BCLK Output Frequency

When PLL Master Mode (MSN bit = "1") is used, the following frequencies is output from the BCLK pin.

Table 6. BCLK Output (x: Do not care)

TDM[1:0] bits	BCKO bit	BCLK pin	Sampling Frequency Range	
00	0	32fs	8 to 192 kHz	(default)
	1	64fs	8 to 192 kHz	
01	x	TDM128fs	8 to 192 kHz	
10	x	TDM256fs	8 to 96 kHz	
11	x	TDM512fs	8 to 48 kHz	

Note 38. When TDM[1:0] bits = "11", the setting of CM[1:0] bits = "00" is not available.

3. Internal Block Diagram of PLL

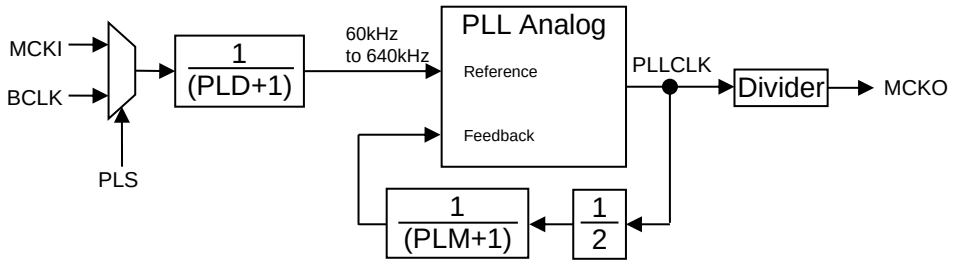


Figure 17. PLL Block Diagram

PLL clock source is selected by PLS bit.

Table 7. PLL Clock Source Select

PLS bit	Clock Source	
0	MCKI pin	(default)
1	BCLK pin	

(3-1) PLL Reference Clock Divider (PLD)

The PLL can set the division ratio of the reference clock in 16 bits. The input clock is used as PLL reference clock by dividing by (PLDx + 1).

Table 8. PLL Reference Clock Divider

PLD[15:0] bits	Division Ratio	
0000H	1	(default)
0001H to FFFFH	1/(PLD+1)	

Note 39. The reference clock should be set in the range from 60kHz to 640kHz after divided by PLD.

(3-2) PLL Feedback Clock Divider (PLM)

The division ratio of feedback clock can be set freely in 16 bits. PLLCLK is divided by ((PLM+1) x 2) and used as a PLL feedback clock. The feedback clock is fixed to “L” without dividing when PLM = 0000H.

Table 9. PLL Feedback Clock Divider

PLM[15:0] bits	Division Ratio	
0000H	Clock Stop	(default)
0001H to FFFFH	1/((PLM+1) x 2)	

4. Adaptive Frequencies

MCKI pin: 11.2896/22.5792MHz, 12.288/24.576MHz, 9.6/19.2MHz, 12/24MHz, 13/26MHz, 13.5/27MHz, 16MHz
BCLK pin: 32fs, 64fs, 128fs, 256fs, 512fs
fs: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz

5. Example of PLL Frequency Setting

5.1. PLL Reference Source: MCKI (PMPLL bit = “1”, MSN bit = “0”, “1”, PLS bit = “0”)

Table 10. PLL Frequency Setting Example (PLL reference source: MCKI) (1)

MCKI [MHz]	fs [kHz]	PLD [15:0] bits	PLM [15:0] bits	FS [3:0] bits	MCKO				Frequency Error [ppm]
					CM[1:0] bits = “00”	CM[1:0] bits = “01”	CM[1:0] bits = “10”	CM[1:0] bits = “11”	
11.2896	8	0092H	031FH	0000	256fs	512fs	1024fs	-	0
	12			0010	256fs	512fs	1024fs	-	0
	16			0100	256fs	512fs	-	-	0
	24			0110	256fs	512fs	1024fs	-	0
	32			1000	256fs	-	-	-	0
	48			1010	256fs	512fs	-	-	0
	96			1101	256fs	-	-	-	0
	192			1111	-	-	-	128fs	0
12.288	11.025	001FH	0092H	0001	256fs	512fs	1024fs	-	0
	22.05			0101	256fs	512fs	1024fs	-	0
	44.1			1001	256fs	512fs	-	-	0
	88.2			1100	256fs	-	-	-	0
	176.4			1110	-	-	-	128fs	0
22.5792	8	0092H	018FH	0000	256fs	512fs	1024fs	-	0
	12			0010	256fs	512fs	1024fs	-	0
	16			0100	256fs	512fs	-	-	0
	24			0110	256fs	512fs	1024fs	-	0
	32			1000	256fs	-	-	-	0
	48			1010	256fs	512fs	-	-	0
	96			1101	256fs	-	-	-	0
	192			1111	-	-	-	128fs	0
24.576	11.025	003FH	0092H	0001	256fs	512fs	1024fs	-	0
	22.05			0101	256fs	512fs	1024fs	-	0
	44.1			1001	256fs	512fs	-	-	0
	88.2			1100	256fs	-	-	-	0
	176.4			1110	-	-	-	128fs	0
12	8	0018H	007FH	0000	256fs	512fs	1024fs	-	0
	12			0010	256fs	512fs	1024fs	-	0
	16			0100	256fs	512fs	-	-	0
	24			0110	256fs	512fs	1024fs	-	0
	32			1000	256fs	-	-	-	0
	48			1010	256fs	512fs	-	-	0
	96			1101	256fs	-	-	-	0
	192			1111	-	-	-	128fs	0
	11.025	007CH	024BH	0001	256fs	512fs	1024fs	-	0
	22.05			0101	256fs	512fs	1024fs	-	0
	44.1			1001	256fs	512fs	-	-	0
	88.2			1100	256fs	-	-	-	0
	176.4			1110	-	-	-	128fs	0

Note 40. “-”: Not available

Table 11. PLL Frequency Setting Example (PLL reference source: MCKI) (2)

MCKI [MHz]	fs [kHz]	PLD [15:0] bits	PLM [15:0] bits	FS [3:0] bits	MCKO				Frequency Error [ppm]
					CM[1:0] bits = "00"	CM[1:0] bits = "01"	CM[1:0] bits = "10"	CM[1:0] bits = "11"	
16	8	0018H	005FH	0000	256fs	512fs	1024fs	-	0
	12			0010	256fs	512fs	1024fs	-	0
	16			0100	256fs	512fs	-	-	0
	24			0110	256fs	512fs	1024fs	-	0
	32			1000	256fs	-	-	-	0
	48			1010	256fs	512fs	-	-	0
	96			1101	256fs	-	-	-	0
	192			1111	-	-	-	128fs	0
	11.025	007CH	01B8H	0001	256fs	512fs	1024fs	-	0
	22.05			0101	256fs	512fs	1024fs	-	0
	44.1			1001	256fs	512fs	-	-	0
	88.2			1100	256fs	-	-	-	0
	176.4			1110	-	-	-	128fs	0
24	8	0031H	007FH	0000	256fs	512fs	1024fs	-	0
	12			0010	256fs	512fs	1024fs	-	0
	16			0100	256fs	512fs	-	-	0
	24			0110	256fs	512fs	1024fs	-	0
	32			1000	256fs	-	-	-	0
	48			1010	256fs	512fs	-	-	0
	96			1101	256fs	-	-	-	0
	192			1111	-	-	-	128fs	0
	11.025	007CH	0125H	0001	256fs	512fs	1024fs	-	0
	22.05			0101	256fs	512fs	1024fs	-	0
	44.1			1001	256fs	512fs	-	-	0
	88.2			1100	256fs	-	-	-	0
	176.4			1110	-	-	-	128fs	0
19.2	8	0031H	009FH	0000	256fs	512fs	1024fs	-	0
	12			0010	256fs	512fs	1024fs	-	0
	16			0100	256fs	512fs	-	-	0
	24			0110	256fs	512fs	1024fs	-	0
	32			1000	256fs	-	-	-	0
	48			1010	256fs	512fs	-	-	0
	96			1101	256fs	-	-	-	0
	192			1111	-	-	-	128fs	0
	11.025	0031H	0092H	0001	256fs	512fs	1024fs	-	0
	22.05			0101	256fs	512fs	1024fs	-	0
	44.1			1001	256fs	512fs	-	-	0
	88.2			1100	256fs	-	-	-	0
	176.4			1110	-	-	-	128fs	0

Note 41. "-": Not available

Table 12. PLL Frequency Setting Example (PLL reference source: MCKI) (3)

MCKI [MHz]	fs [kHz]	PLD [15:0] bits	PLM [15:0] bits	FS [3:0] bits	MCKO				Frequency Error [ppm]
					CM[1:0] bits = "00"	CM[1:0] bits = "01"	CM[1:0] bits = "10"	CM[1:0] bits = "11"	
9.6	8	000EH	005FH	0000	256fs	512fs	1024fs	-	0
	12			0010	256fs	512fs	1024fs	-	0
	16			0100	256fs	512fs	-	-	0
	24			0110	256fs	512fs	1024fs	-	0
	32			1000	256fs	-	-	-	0
	48			1010	256fs	512fs	-	-	0
	96			1101	256fs	-	-	-	0
	192			1111	-	-	-	128fs	0
	11.025	0018H	0092H	0001	256fs	512fs	1024fs	-	0
	22.05			0101	256fs	512fs	1024fs	-	0
	44.1			1001	256fs	512fs	-	-	0
	88.2			1100	256fs	-	-	-	0
	176.4			1110	-	-	-	128fs	0
13	8	0053H	018CH	0000	256fs	512fs	1024fs	-	7.750
	12			0010	256fs	512fs	1024fs	-	7.750
	16			0100	256fs	512fs	-	-	7.750
	24			0110	256fs	512fs	1024fs	-	7.750
	32			1000	256fs	-	-	-	7.750
	48			1010	256fs	512fs	-	-	7.750
	96			1101	256fs	-	-	-	7.750
	192			1111	-	-	-	128fs	7.750
	11.025	0025H	00A4H	0001	256fs	512fs	1024fs	-	-11.189
	22.05			0101	256fs	512fs	1024fs	-	-11.189
	44.1			1001	256fs	512fs	-	-	-11.189
	88.2			1100	256fs	-	-	-	-11.189
	176.4			1110	-	-	-	128fs	-11.189
26	8	0144H	02FFH	0000	256fs	512fs	1024fs	-	0
	12			0010	256fs	512fs	1024fs	-	0
	16			0100	256fs	512fs	-	-	0
	24			0110	256fs	512fs	1024fs	-	0
	32			1000	256fs	-	-	-	0
	48			1010	256fs	512fs	-	-	0
	96			1101	256fs	-	-	-	0
	192			1111	-	-	-	128fs	0
	11.025	004BH	00A4H	0001	256fs	512fs	1024fs	-	-11.189
	22.05			0101	256fs	512fs	1024fs	-	-11.189
	44.1			1001	256fs	512fs	-	-	-11.189
	88.2			1100	256fs	-	-	-	-11.189
	176.4			1110	-	-	-	128fs	-11.189

Note 42. "-": Not available

Table 13. PLL Frequency Setting Example (PLL reference source: MCKI) (4)

MCKI [MHz]	fs [kHz]	PLD [15:0] bits	PLM [15:0] bits	FS [3:0] bits	MCKO				Frequency Error [ppm]
					CM[1:0] bits = "00"	CM[1:0] bits = "01"	CM[1:0] bits = "10"	CM[1:0] bits = "11"	
13.5	8	00E0H	03FFH	0000	256fs	512fs	1024fs	-	0
	12			0010	256fs	512fs	1024fs	-	0
	16			0100	256fs	512fs	-	-	0
	24			0110	256fs	512fs	1024fs	-	0
	32			1000	256fs	-	-	-	0
	48			1010	256fs	512fs	-	-	0
	96			1101	256fs	-	-	-	0
	192			1111	-	-	-	128fs	0
	11.025	00B5H	02F8H	0001	256fs	512fs	1024fs	-	-3.504
	22.05			0101	256fs	512fs	1024fs	-	-3.504
	44.1			1001	256fs	512fs	-	-	-3.504
	88.2			1100	256fs	-	-	-	-3.504
	176.4			1110	-	-	-	128fs	-3.504
27	8	00E0H	01FFH	0000	256fs	512fs	1024fs	-	0
	12			0010	256fs	512fs	1024fs	-	0
	16			0100	256fs	512fs	-	-	0
	24			0110	256fs	512fs	1024fs	-	0
	32			1000	256fs	-	-	-	0
	48			1010	256fs	512fs	-	-	0
	96			1101	256fs	-	-	-	0
	192			1111	-	-	-	128fs	0
	11.025	0181H	0326H	0001	256fs	512fs	1024fs	-	3.304
	22.05			0101	256fs	512fs	1024fs	-	3.304
	44.1			1001	256fs	512fs	-	-	3.304
	88.2			1100	256fs	-	-	-	3.304
	176.4			1110	-	-	-	128fs	3.304

Note 43. "-": Not available

5.2. PLL Reference Source: BCLK [Stereo Mode] (PMPLL bit = “1”, MSN bit = “0”, PLS bit = “1”, TDM[1:0] bits = “00”)

Table 14. PLL Frequency Setting Example (PLL reference source: BCLK [Stereo Mode])

fs [kHz]	BCLK	BCLK [MHz]	PLD [15:0] bits	PLM [15:0] bits	FS [3:0] bits	MCKO			
						CM[1:0] bits = “00”	CM[1:0] bits = “01”	CM[1:0] bits = “10”	CM[1:0] bits = “11”
8	32fs	0.256	0000H	00EFH	0000	256fs	512fs	1024fs	-
12		0.384	0000H	009FH	0010	256fs	512fs	1024fs	-
16		0.512	0000H	0077H	0100	256fs	512fs	-	-
24		0.768	0001H	009FH	0110	256fs	512fs	1024fs	-
32		1.024	0001H	0077H	1000	256fs	-	-	-
48		1.536	0003H	009FH	1010	256fs	512fs	-	-
96		3.072	0007H	009FH	1101	256fs	-	-	-
192		6.144	000FH	009FH	1111	-	-	-	128fs
11.025		0.3528	0000H	009FH	0001	256fs	512fs	1024fs	-
22.05		0.7056	0001H	009FH	0101	256fs	512fs	1024fs	-
44.1		1.4112	0003H	009FH	1001	256fs	512fs	-	-
88.2		2.8224	0007H	009FH	1100	256fs	-	-	-
176.4		5.6448	000FH	009FH	1110	-	-	-	128fs
8	64fs	0.512	0000H	0077H	0000	256fs	512fs	1024fs	-
12		0.768	0001H	009FH	0010	256fs	512fs	1024fs	-
16		1.024	0001H	0077H	0100	256fs	512fs	-	-
24		1.536	0003H	009FH	0110	256fs	512fs	1024fs	-
32		2.048	0003H	0077H	1000	256fs	-	-	-
48		3.072	0007H	009FH	1010	256fs	512fs	-	-
96		6.144	000FH	009FH	1101	256fs	-	-	-
192		12.288	001FH	009FH	1111	-	-	-	128fs
11.025		0.7056	0001H	009FH	0001	256fs	512fs	1024fs	-
22.05		1.4112	0003H	009FH	0101	256fs	512fs	1024fs	-
44.1		2.8224	0007H	009FH	1001	256fs	512fs	-	-
88.2		5.6448	000FH	009FH	1100	256fs	-	-	-
176.4		11.2896	001FH	009FH	1110	-	-	-	128fs

Note 44. “-”: Not available

5.3. PLL Reference Source: BCLK [TDM Mode] (PMPLL bit = “1”, MSN bit = “0”, PLS bit = “1”, TDM[1:0] bits = “01”, “10”, “11”)

Table 15. PLL Frequency Setting Example (PLL reference source: BCLK [TDM Mode])

fs [kHz]	BCLK	BCLK [MHz]	TDM [1:0] bits	PLD [15:0] bits	PLM [15:0] bits	FS [3:0] bits	MCKO			
							CM[1:0] bits = “00”	CM[1:0] bits = “01”	CM[1:0] bits = “10”	CM[1:0] bits = “11”
8	128fs	1.024	01	0001H	0077H	0000	256fs	512fs	1024fs	-
12		1.536		0003H	009FH	0010	256fs	512fs	1024fs	-
16		2.048		0003H	0077H	0100	256fs	512fs	-	-
24		3.072		0007H	009FH	0110	256fs	512fs	1024fs	-
32		4.096		0007H	0077H	1000	256fs	-	-	-
48		6.144		000FH	009FH	1010	256fs	512fs	-	-
96		12.288		001FH	009FH	1101	256fs	-	-	-
192		24.576		003FH	009FH	1111	-	-	-	128fs
11.025		1.4112		0003H	009FH	0001	256fs	512fs	1024fs	-
22.05		2.8224		0007H	009FH	0101	256fs	512fs	1024fs	-
44.1		5.6448		000FH	009FH	1001	256fs	512fs	-	-
88.2		11.2896		001FH	009FH	1100	256fs	-	-	-
176.4		22.5792		003FH	009FH	1110	-	-	-	128fs
8	256fs	2.048	10	0003H	0077H	0000	256fs	512fs	1024fs	-
12		3.072		0007H	009FH	0010	256fs	512fs	1024fs	-
16		4.096		0007H	0077H	0100	256fs	512fs	-	-
24		6.144		000FH	009FH	0110	256fs	512fs	1024fs	-
32		8.192		000FH	0077H	1000	256fs	-	-	-
48		12.288		001FH	009FH	1010	256fs	512fs	-	-
96		24.576		003FH	009FH	1101	256fs	-	-	-
11.025		2.8224		0007H	009FH	0001	256fs	512fs	1024fs	-
22.05		5.6448		000FH	009FH	0101	256fs	512fs	1024fs	-
44.1		11.2896		001FH	009FH	1001	256fs	512fs	-	-
88.2		22.5792		003FH	009FH	1100	256fs	-	-	-
8	512fs	4.096	11	0007H	0077H	0000	256fs	512fs	1024fs	-
12		6.144		000FH	009FH	0010	256fs	512fs	1024fs	-
16		8.192		000FH	0077H	0100	256fs	512fs		-
24		12.288		001FH	009FH	0110	256fs	512fs	1024fs	-
32		16.384		001FH	0077H	1000	256fs	-	-	-
48		24.576		003FH	009FH	1010	256fs	512fs	-	-
11.025		5.6448		000FH	009FH	0001	256fs	512fs	1024fs	-
22.05		11.2896		001FH	009FH	0101	256fs	512fs	1024fs	-
44.1		22.5792		003FH	009FH	1001	256fs	512fs	-	-

Note 45. “-”: Not available

9.5. Audio Interface Format

Audio interface formats are selectable with the MSN, TDM[1:0] and DIF[1:0] bits. In all modes the serial data format is MSB first, 2's complement. Audio interface formats can be used in both master and slave modes. In master mode (MSN bit = "1"), the SDTO1/2 pins are clocked out on the falling edge (rising edge when BCKP bit = "1") of BCLK. Normal output in slave mode (TDM[1:0] bits = "00", DIF[1:0] bits = "00", "01", MSN bit = "0"), the SDTO1/2 pins are clocked out on the falling edge (rising edge when BCKP bit = "1") of BCLK. In other conditions (PCM and TDM Mode), the data is clocked out on the prior rising edge (falling edge when BCKP bit = "1") of BCLK to compensate for some delay that renders the edge of data transition near BCLK falling edge. The TDMIN pin and SDTO2 pin are shared. SDTO2E bit is set to "1" to enable the SDTO2 pin. BCLK edge polarity can be set by BCKP bit. SDTO data length is set by DLC[1:0] bits.

Table 16. Audio Interface Format (Stereo Mode)

Mode	MSN bit	TDM[1:0] bits	DIF[1:0] bits	SDTO1/2 pin	BCLK		Figure	
0	0	00	00	I²S compatible	≥ 32fs	I	Figure 18	(default)
1	0	00	01	MSB justified	≥ 32fs	I	Figure 19	
2	0	00	10	PCM Short Frame	≥ 32fs	I	Figure 20	
3	0	00	11	PCM Long Frame	≥ 32fs	I	Figure 21	
4	1	00	00	I²S compatible	32fs or 64fs	O	Figure 18	
5	1	00	01	MSB justified	32fs or 64fs	O	Figure 19	
6	1	00	10	PCM Short Frame	32fs or 64fs	O	Figure 20	
7	1	00	11	PCM Long Frame	32fs or 64fs	O	Figure 21	

Table 17. Audio Interface Format (TDM128 Mode, N/A: Not available)

Mode	MSN bit	TDM[1:0] bits	DIF[1:0] bits	SDTO1 pin	BCLK		Figure
8	0	01	00	I²S compatible	128fs	I	Figure 22
9	0	01	01	MSB justified	128fs	I	Figure 23
10	0	01	10	N/A	-	-	-
11	0	01	11	N/A	-	-	-
12	1	01	00	I²S compatible	128fs	O	Figure 22
13	1	01	01	MSB justified	128fs	O	Figure 23
14	1	01	10	N/A	-	-	-
15	1	01	11	N/A	-	-	-

Note 46. MCKI frequency needs more than twice BCLK frequency in case of EXT Master Mode.

Table 18. Audio Interface Format (TDM256 Mode, N/A: Not available)

Mode	MSN bit	TDM[1:0] bits	DIF[1:0] bits	SDTO1 pin	BCLK		Figure
16	0	10	00	I²S compatible	256fs	I	Figure 24
17	0	10	01	MSB justified	256fs	I	Figure 25
18	0	10	10	N/A	-	-	-
19	0	10	11	N/A	-	-	-
20	1	10	00	I²S compatible	256fs	O	Figure 24
21	1	10	01	MSB justified	256fs	O	Figure 25
22	1	10	10	N/A	-	-	-
23	1	10	11	N/A	-	-	-

Note 47. MCKI frequency needs more than twice BCLK frequency in case of EXT Master Mode.

Table 19. Audio Interface Format (TDM512 Mode, N/A: Not available)

Mode	MSN bit	TDM[1:0] bits	DIF[1:0] bits	SDTO1 pin	BCLK		Figure
24	0	11	00	I²S compatible	512fs	I	Figure 26
25	0	11	01	MSB justified	512fs	I	Figure 27
26	0	11	10	N/A	-	-	-
27	0	11	11	N/A	-	-	-
28	1	11	00	I²S compatible	512fs	O	Figure 26
29	1	11	01	MSB justified	512fs	O	Figure 27
30	1	11	10	N/A	-	-	-
31	1	11	11	N/A	-	-	-

Note 48. MCKI frequency needs more than twice BCLK frequency in case of EXT Master Mode.

Table 20. BCLK Edge

BCKP bit	BCLK edge referenced to LRCK edge	
0	Falling Edge	(default)
1	Rising Edge	

Table 21. Data Length Setting (N/A: Not available)

DLC[1:0] bits	SDTO Data Length	
00	24-bit Linear	(default)
01	16-bit Linear	
10	32-bit Linear	
11	N/A	

Note 49. In TDM mode, the data width of 1SLOT is set 32-bits when SDTO data length is selected 24-bits or 32-bits. In TDM mode, the data width of 1SLOT is set 16-bits when SDTO data length is selected 16-bits.

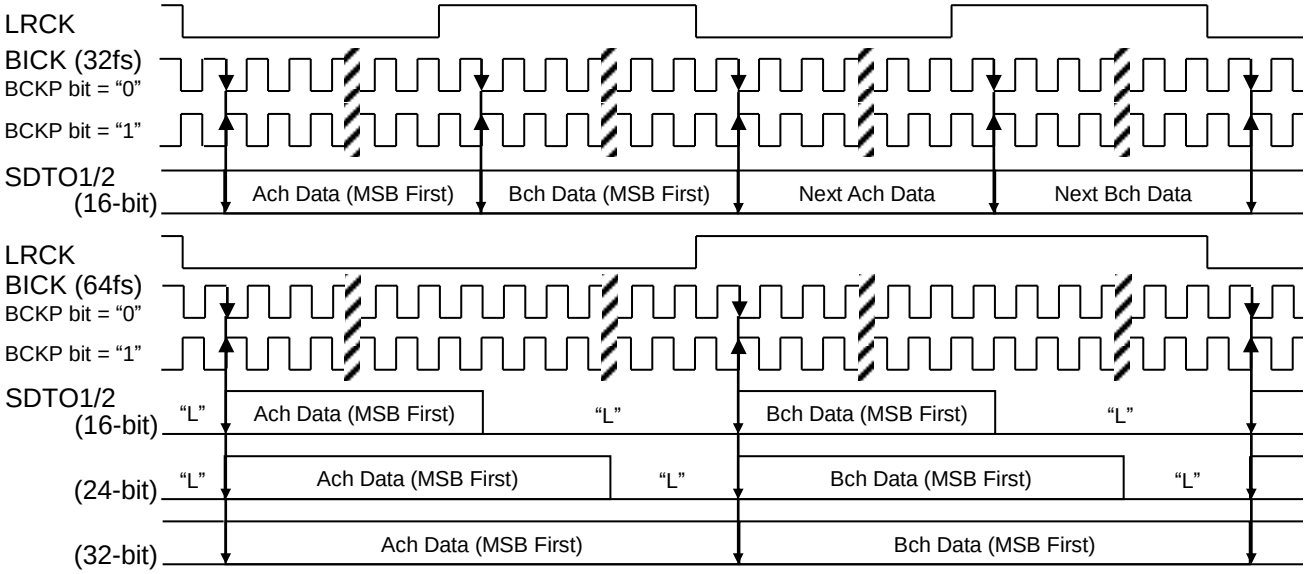


Figure 18. Mode 0/4 Timing (Normal mode, I^2S Compatible)

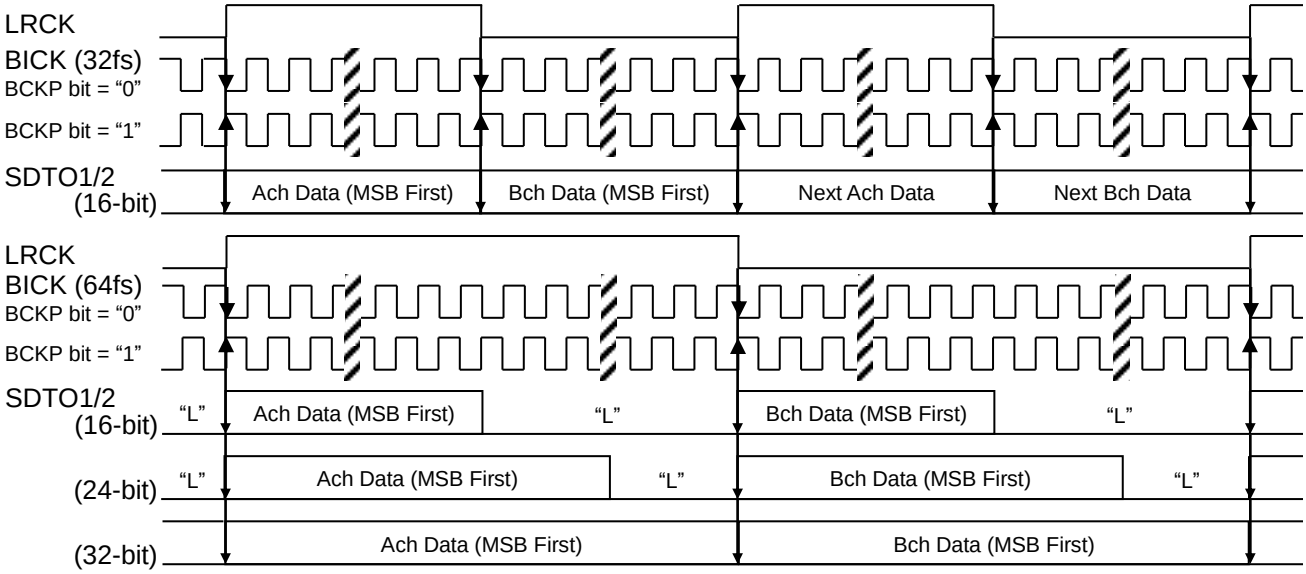


Figure 19. Mode 1/5 Timing (Normal mode, MSB Justified)

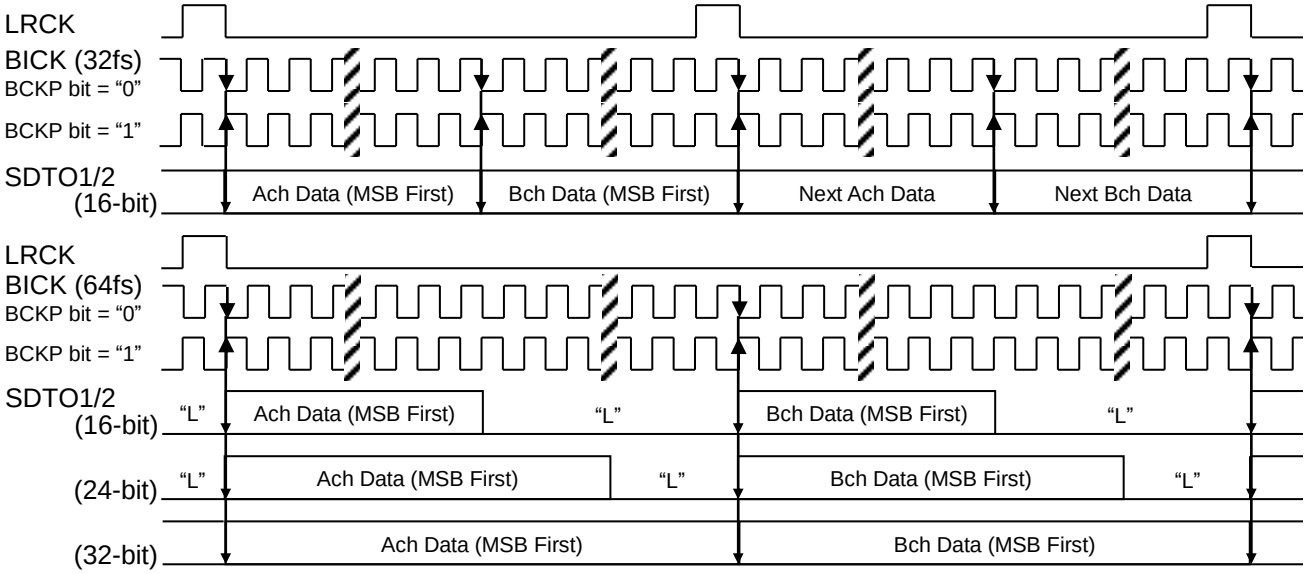


Figure 20. Mode 2/6 Timing (Normal mode, PCM Short Frame)

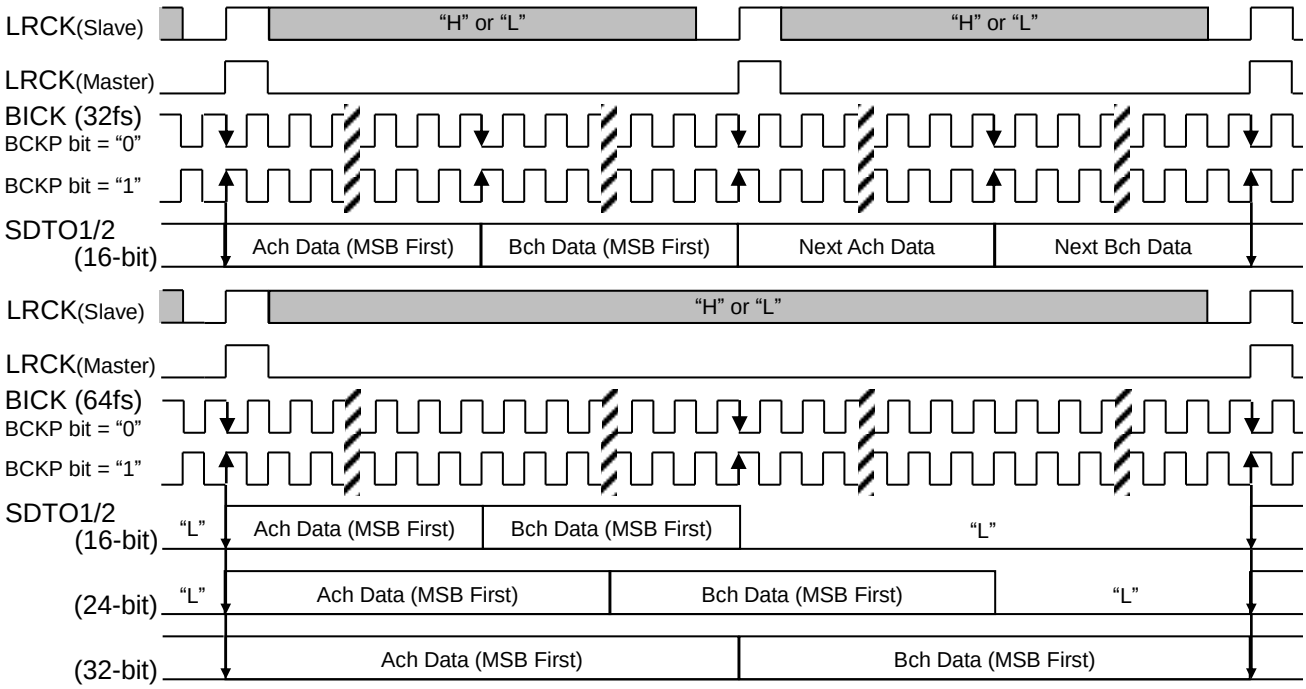


Figure 21. Mode 3/7 Timing (Normal mode, PCM Long Frame)

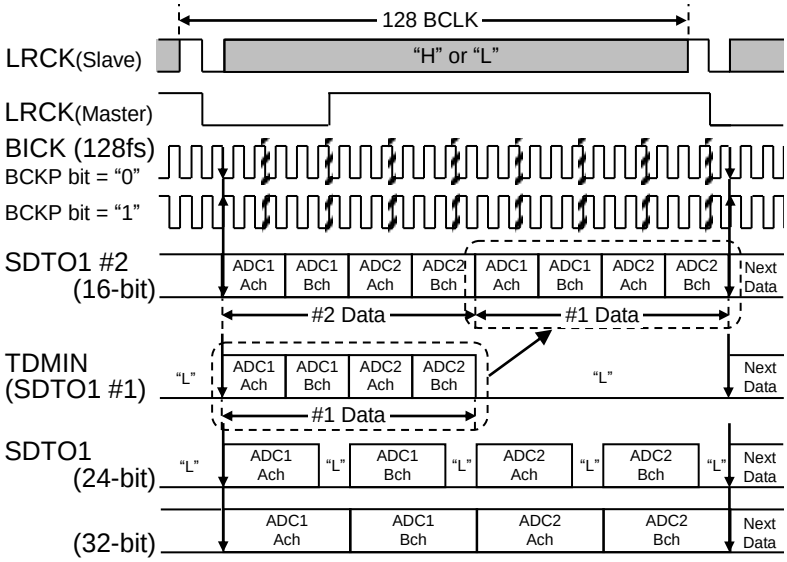


Figure 22. Mode 8/12 Timing (TDM128 mode, I²S Compatible)

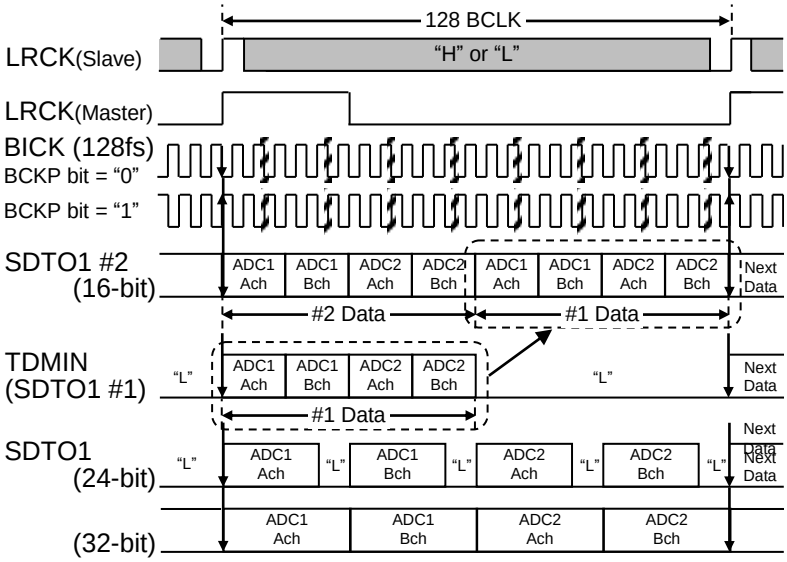


Figure 23. Mode 9/13 Timing (TDM128 mode, MSB Justified)

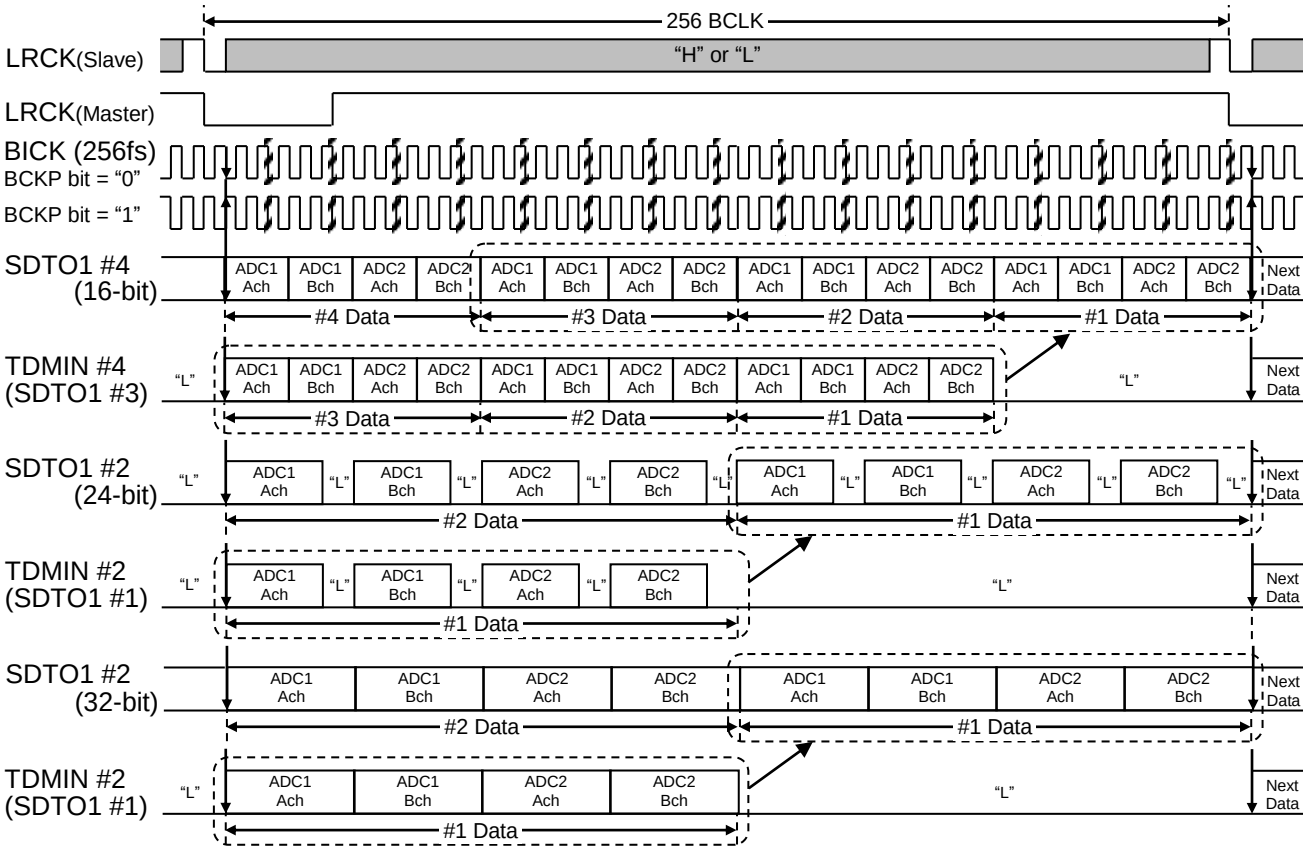


Figure 24. Mode 16/20 Timing (TDM256 mode, I²S Compatible)

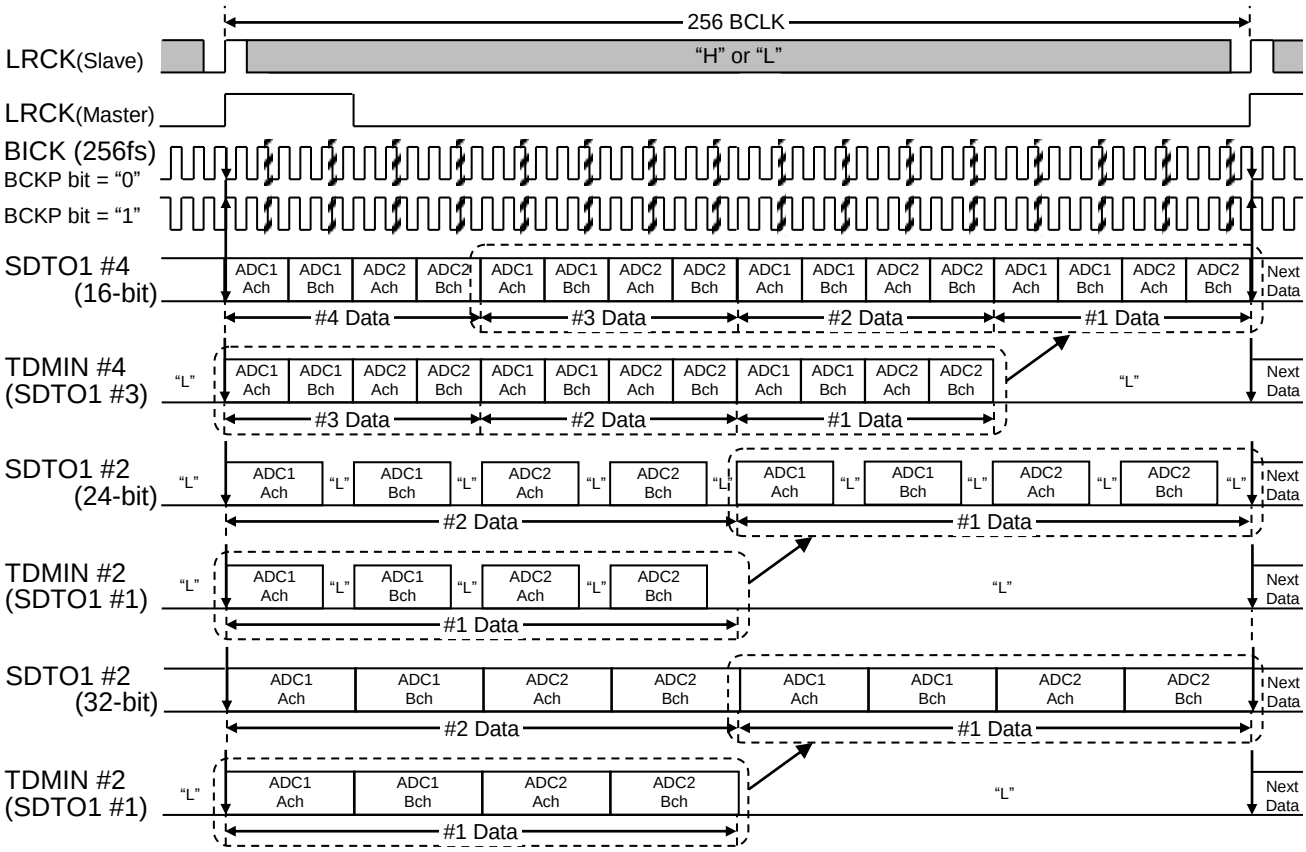


Figure 25. Mode 17/21 Timing (TDM256 mode, MSB Justified)

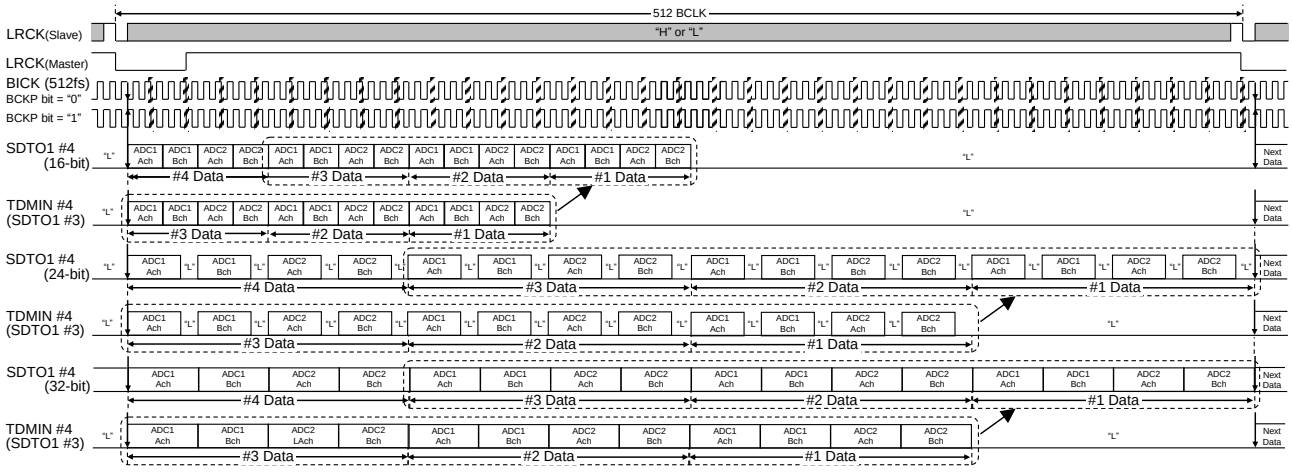


Figure 26. Mode24/28 Timing (TDM512 mode, I²S Compatible)

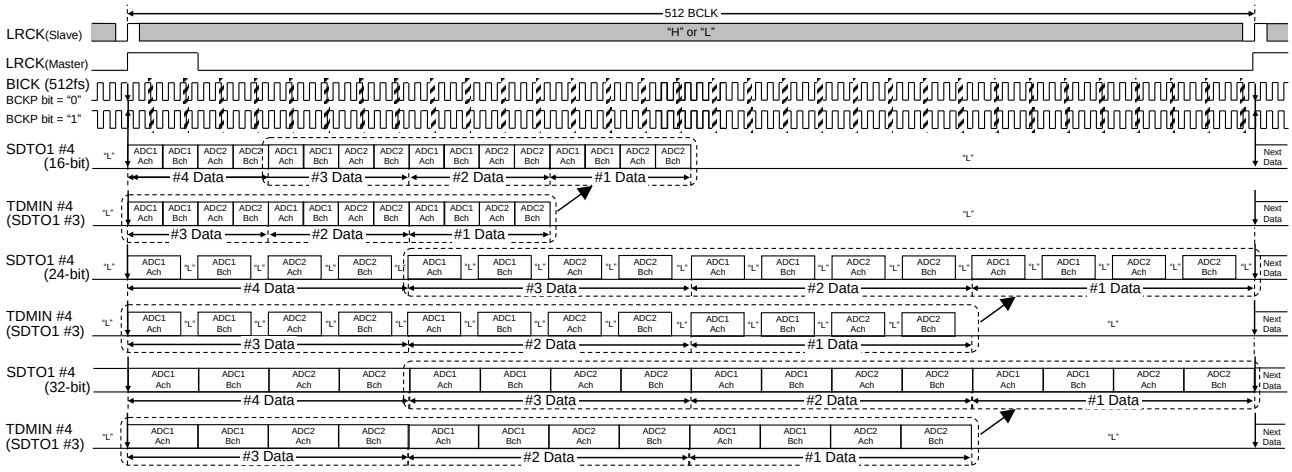


Figure 27. Mode 25/29 Timing (TDM512 mode, MSB Justified)

Cascade Connection in TDM Mode

The AK5704 supports a cascade connection of four devices in TDM modes. Figure 28 shows a connection example. All A/D converted data of connected AK5704's is output from the SDTO1 pin of the last AK5704 via cascade connection.

When the data length is 24-bits (DLC[1:0] bits = "00") or 32-bits (DLC[1:0] bits = "10"), the AK5704 supports up to 4ch outputs in TDM128 mode, 8ch outputs in TDM256 mode and 16ch outputs in TDM512 mode (Figure 28).
When DLC[1:0] bits = "01"(16-bits), the AK5704 supports up to 8ch outputs in TDM128 mode, 16ch outputs in TDM256 mode and 16ch outputs in TDM512 mode.

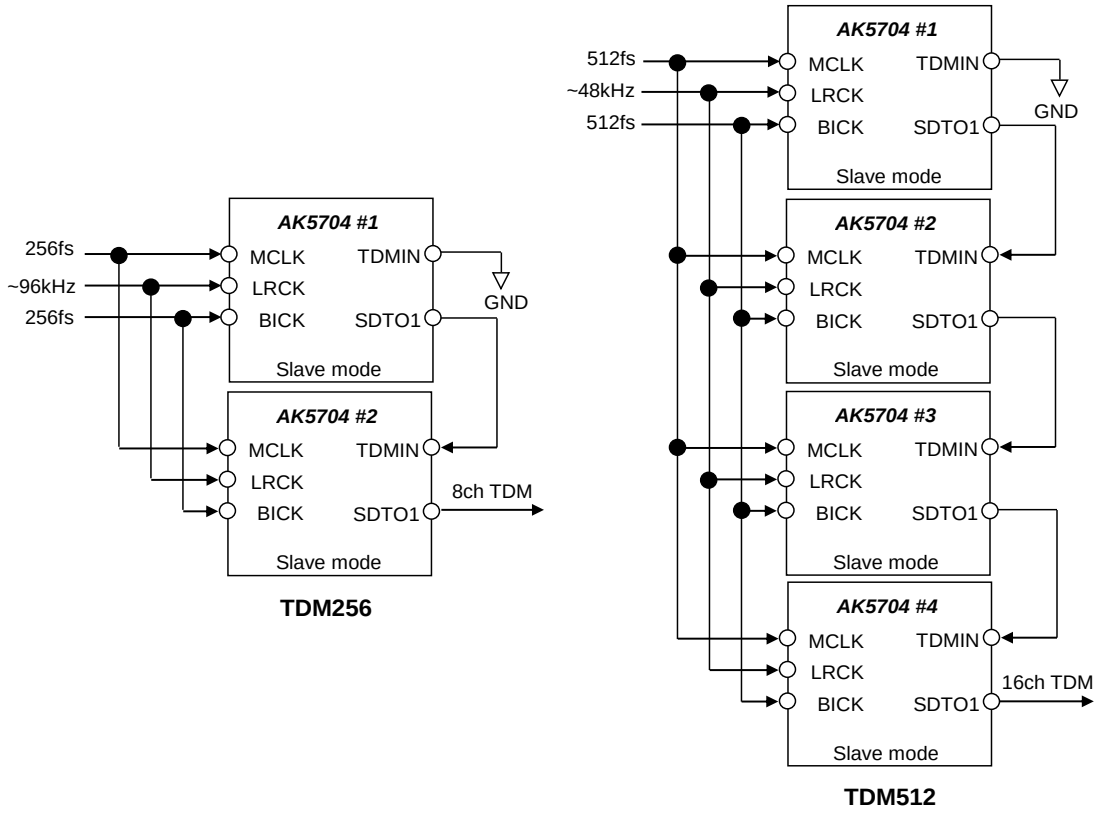


Figure 28. Cascade Connection

9.6. Synchronization with audio system (SYNCDET)

The AK5704 has a SYNCDET circuit for phase synchronization of the data output since it is assumed that multiple AK5704's will be used in TDM mode.

When the clock frequency is changed during operation, phase mismatch may occur between external LRCK and data transferring clock that has the same frequency as the internal LRCK generated from external LRCK. The SYNCDET circuit resets the internal counter and adjusts the phase between LRCK and FsCLK automatically. Therefore, there's a possibility that pop noise occurs.

To prevent pop noise, the following methods are recommended:

(1) Clock mode must be changed when PMAD1A/B = PMAD2A/B = PMDM1A/B = PMDM2A/B = PMPFIL1 = PMPFIL2 bits = "0".
(2) Stable clock must be supplied during operation (PDN pin = "H").

9.7. MIC/LINE Input

The AK5704 supports both single-ended (Pseudo-Differential) and full-differential modes for analog input. When MDIF1A, MDIF1B, MDIF2A, MDIF2B bits = "0" (default), each input pin is in single-ended mode. When MDIF1A, MDIF1B, MDIF2A, MDIF2B bits = "1", each input pin is in full-differential mode. In single-ended mode, the signal should be input to the AINxA/B+ pins and the AINxA/B- pins should be connected to the ground via a capacitor in series (Figure 29). All input pins are in single-ended mode (MDIF1A = MDIF1B = MDIF2A = MDIF2B bits = "0") and AINCOM bit = "1", only one capacitor is connected to the ground. AINxA/B- pins should be shorted all and connected to the ground via a capacitor in series (Figure 31).

Table 22. AIN1 Input Select

MDIF1A bit	MDIF1B bit	AIN1A	AIN1B	
0	0	AIN1A+ pin (Single-ended)	AIN1B+ pin (Single-ended)	(default)
0	1	AIN1A+ pin (Single-ended)	AIN1B+/- pins (Full-differential)	
1	0	AIN1A+/- pins (Full-differential)	AIN1B+ pin (Single-ended)	
1	1	AIN1A+/- pins (Full-differential)	AIN1B+/- pins (Full-differential)	

Table 23. AIN2 Input Select

MDIF2A bit	MDIF2B bit	AIN2A	AIN2B	
0	0	AIN2A+ pin (Single-ended)	AIN2B+ pin (Single-ended)	(default)
0	1	AIN2A+ pin (Single-ended)	AIN2B+/- pins (Full-differential)	
1	0	AIN2A+/- pins (Full-differential)	AIN2B+ pin (Single-ended)	
1	1	AIN2A+/- pins (Full-differential)	AIN2B+/- pins (Full-differential)	

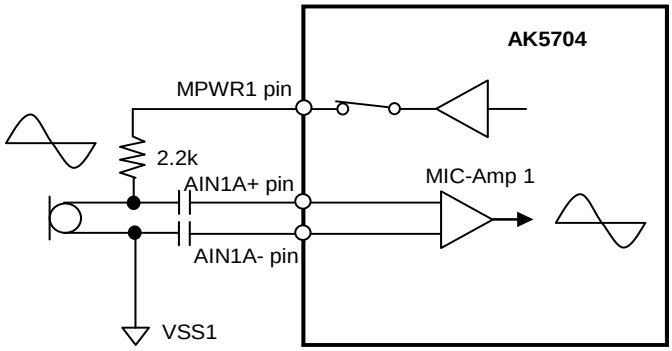


Figure 29. Connection Example for Single-ended Microphone Input (AINCOM bit = "0")

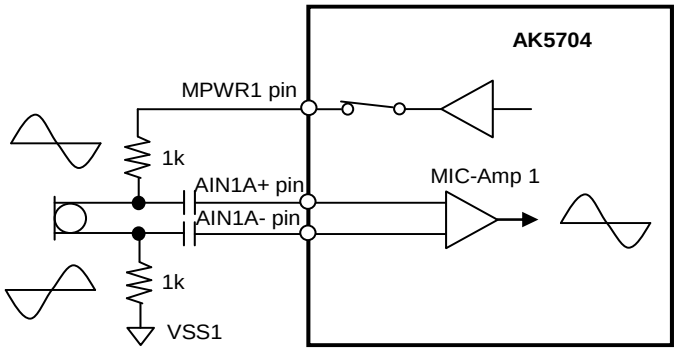


Figure 30. Connection Example for Full-differential Microphone Input

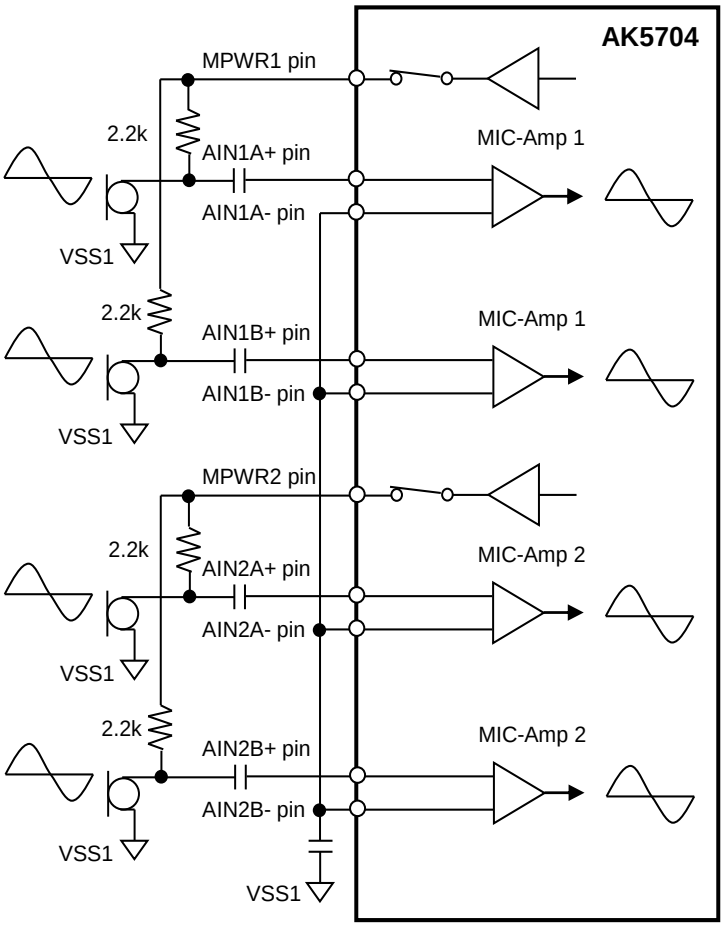


Figure 31. Connection Example for Single-ended Microphone Input (AINCOM bit = “1”)

9.8. Microphone Amplifier Gain

The AK5704 has gain amplifiers for microphone input. The gain of four microphone amplifiers can be independently selected by MG1A[3:0], MG1B[3:0], MG2A[3:0] and MG2B[3:0] bits. The volume is changed immediately by setting these bits.

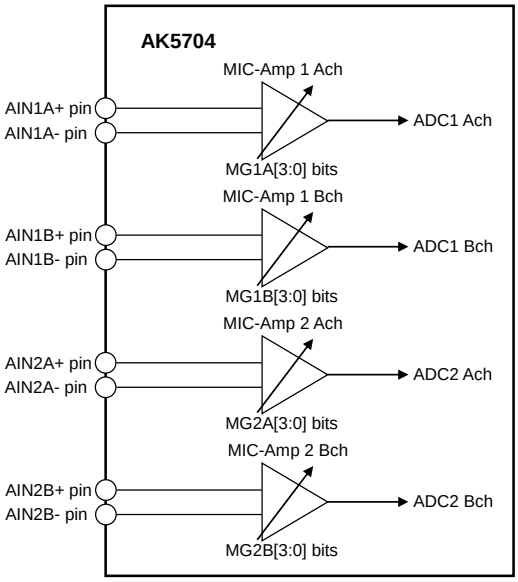


Figure 32. MIC Input Volume Setting

Table 24. MIC Amplifier 1/2 Gain (N/A: Not available)

MG1A3 bit MG1B3 bit MG2A3 bit MG2B3 bit	MG1A2 bit MG1B2 bit MG2A2 bit MG2B2 bit	MG1A1 bit MG1B1 bit MG2A1 bit MG2B1 bit	MG1A0 bit MG1B0 bit MG2A0 bit MG2B0 bit	Gain	
0	0	0	0	0 dB	
0	0	0	1	+3 dB	
0	0	1	0	+6 dB	
0	0	1	1	+9 dB	
0	1	0	0	+12 dB	
0	1	0	1	+15 dB	
0	1	1	0	+18 dB	(default)
0	1	1	1	+21 dB	
1	0	0	0	+24 dB	
1	0	0	1	+27 dB	
1	0	1	0	+30 dB	
Others				N/A	

9.9. Microphone Power

The AK5704 has two microphone power supplies. They can be powered up at the same time. Output voltage of MPWR1/2 are common setting by MICL[1:0] bits. PMMPx bit controls output status. When PMMPx bit is “1”, microphone power is output. When PMMPx bit is “0”, the MPWRx pin becomes power-down state (Hi-Z). The load resistance is minimum 650Ω for each MPWR1/2 pin. Any capacitor must not be connected directly to the MPWR1/2 pins. The AK5704 has a MIC power direct mode for the MPWR1/2 pins. The AVDD voltage is directly output from the MPWR1/2 pin via the internal switch (ON resistance: typ. 37Ω, max. 62Ω) by setting MICL[1:0] bits = “11”. In MIC power direct mode (MICL[1:0] bits = “11”), PMMP1/2 bit controls ON/OFF of the internal switch. This power-up timer will not work in MIC power direct mode.

Set MICL[1:0] bits before power-on of the corresponding MPWR pin (there is no time limitation). When a MPWR pin is ON, the setting of corresponding MICL[1:0] bits should not be changed.

When using a microphone power, the power-up sequence below should be followed to reduce DC offset (pop noise).

1. MIC Power ON
2. MIC Amplifier/ADC ON

Table 25. MIC Power Output Voltage

MICL[1:0] bits	MPWR1/2 Output Level (Typ.)	
00	2.8 V	(default)
01	2.5 V	
10	1.8 V	
11	Direct Mode (AVDD)	

Note 50. When AVDD=1.7~1.9V, the setting of MICL[1:0] bits = "11" is only available.

Table 26. MIC Power Output Status

PMMP1/2 bits	MPWR1/2 pins	
0	Hi-z	(default)
1	Output	

9.10. MIC Input Start-Up Time

The microphone input circuit can be powered-up/down by PMAIN1A/B and PMAIN2A/B bits. The initialization cycle starts by setting PMAINxA/B bit to "1". An acceleration circuit, which shortens the charging time of an input capacitor, starts operation when the microphone input circuit is powered up. The initialization cycle can be set by AIRST[2:0] bits (Table 27) and this setting is common for all channels. Although it depends on the condition of microphone characteristic and external circuit, the initialization cycle should be set to longer than 13.7 ms when a capacitor for AC-coupling is 1 µF ± 50%. The initialization cycle should be set to longer than 6.8 ms when a capacitor for AC-coupling is 0.47 µF ± 50%.

Table 27. AINxA/B Start-Up Time (N/A: Not available)

AIRST[2:0] bits	Start-Up Time					
	Cycle	fs = 16 kHz	fs = 48 kHz	fs = 96 kHz	fs = 192 kHz	
000	656/fs	41.0ms	13.7ms	6.8ms	3.4ms	(default)
001	164/fs	10.3ms	3.4ms	1.7ms	0.9ms	
010	1312/fs	82.0ms	27.3ms	13.7ms	6.8ms	
011	328/fs	20.5ms	6.8ms	3.4ms	1.7ms	
100	2624/fs	164ms	54.7ms	27.3ms	13.7ms	
101	128/fs	8.0ms	N/A			
110	256/fs	16.0ms	N/A			
111	512/fs	32.0ms	N/A			

9.11. ADC1/2 Initialization Cycle

The ADC1/2 enters an initialization cycle after PMAD1A, PMAD1B, PMAD2A or PMAD2B bit is changed from "0" to "1" when all of these bits are "0". The initialization cycle time is set by ADRST[2:0] bits (Table 28). During the initialization cycle, the ADC1/2 digital data output of both channels are forced to "0" in 2's complement. The ADC output reflects the analog input signal after the initialization cycle is complete. When using a digital microphone, the initialization cycle is the same as ADC's.

Note 51. The initial data of ADC1/2 has offset data that depends on the condition of the microphone and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer or do not use the initial data of ADC1/2.

Table 28. ADC1/2 Initialization Cycle (N/A: Not available)

ADRST[2:0] bits	Initialization Cycle					
	Cycle	fs = 16 kHz	fs = 48 kHz	fs = 96 kHz	fs = 192 kHz	
000	1059/fs	66.2ms	22.1ms	11.0ms	5.5ms	(default)
001	267/fs	16.7ms	5.6ms	2.8ms	1.4ms	
010	2115/fs	132.2ms	44.1ms	22.0ms	11.0ms	
011	531/fs	33.2ms	11.1ms	5.5ms	2.8ms	
100	4230/fs	528.8ms	88.1ms	44.1ms	22.0ms	
101	8/fs	0.5ms	N/A			
110	16/fs	1.0ms	N/A			
111	32/fs	2.0ms	N/A			

Note 52. When ADRST[2:0] bits = "101" and "110", the initial data includes unstable data. The initial data of ADC1/2 (the length of Group Delay of ADC Digital Filter) should not be used.

9.12. Mono/Stereo Mode

MONON bit and PMAD1A/B bits set mono/stereo operation of the ADC1. MONON bit and PMAD2A/B bits set mono/stereo operation of the ADC2. When changing ADC operation and analog/digital microphone, PMAD1A/B (PMAD2A/B) and PMDM1A/B (PMDM2A/B) bits must be set "0" at first. When DMIC1 bit is = "0", PMDM1A/B bit settings are ignored. When DMIC2 bit = "0", PMDM2A/B bits setting are ignored. When DMIC1 bit is = "1", PMAD1A/B bit settings are ignored. When DMIC2 bit = "1", PMAD2A/B bits setting are ignored.

Table 29. ADC1 Mono/Stereo Select (Analog Microphone) (x: Do not care)

MONON bit	PMAD1A bit	PMAD1B bit	ADC1 Ach data	ADC1 Bch data	
x	0	0	"0" data	"0" data	(default)
0	0	1	"0" data	AIN1B Input Signal	
0	1	0	AIN1A Input Signal	"0" data	
1	0	1	AIN1B Input Signal	AIN1B Input Signal	
1	1	0	AIN1A Input Signal	AIN1A Input Signal	
x	1	1	AIN1A Input Signal	AIN1B Input Signal	

Table 30. ADC2 Mono/Stereo Select (Analog Microphone) (x: Do not care)

MONON bit	PMAD2A bit	PMAD2B bit	ADC2 Ach data	ADC2 Bch data	
x	0	0	"0" data	"0" data	(default)
0	0	1	"0" data	AIN2B Input Signal	
0	1	0	AIN2A Input Signal	"0" data	
1	0	1	AIN2B Input Signal	AIN2B Input Signal	
1	1	0	AIN2A Input Signal	AIN2A Input Signal	
x	1	1	AIN2A Input Signal	AIN2B Input Signal	

Table 31. DMIC1 Mono/Stereo Select (Digital Microphone) (x: Do not care)

MONON bit	PMDM1A bit	PMDM1B bit	ADC1 Ach data	ADC1 Bch data	
x	0	0	"0" data	"0" data	(default)
0	0	1	"0" data	DMIC1 Bch Input Signal	
0	1	0	DMIC1 Ach Input Signal	"0" data	
1	0	1	DMIC1 Bch Input Signal	DMIC1 Bch Input Signal	
1	1	0	DMIC1 Ach Input Signal	DMIC1 Ach Input Signal	
x	1	1	DMIC1 Ach Input Signal	DMIC1 Bch Input Signal	

Table 32. DMIC2 Mono/Stereo Select (Digital Microphone) (x: Do not care)

MONON bit	PMDM2A bit	PMDM2B bit	ADC2 Ach data	ADC2 Bch data	
x	0	0	"0" data	"0" data	(default)
0	0	1	"0" data	DMIC2 Bch Input Signal	
0	1	0	DMIC2 Ach Input Signal	"0" data	
1	0	1	DMIC2 Bch Input Signal	DMIC2 Bch Input Signal	
1	1	0	DMIC2 Ach Input Signal	DMIC2 Ach Input Signal	
x	1	1	DMIC2 Ach Input Signal	DMIC2 Bch Input Signal	

9.13. Digital Microphone

1. Connection to Digital Microphone

When DMIC1 bit is set to “1”, the AIN1A+ pin and the AIN1B+ pin become the DMDAT1 (digital microphone data input) pin and the DMCLK1 (digital microphone clock supply) pin, respectively. When DMIC2 bit is set to “1”, the AIN2A+ pin and the AIN2B+ pin become the DMDAT2 (digital microphone data input) pin and the DMCLK2 (digital microphone clock supply) pin, respectively. DMCLK2 is the same clock (64fs) as DMCLK1.

The same power supply as AVDD must be provided to the digital microphone. The Figure 33 and Figure 34 show stereo/mono connection examples. By dividing the master clock to 64fs with divider, the DMCLK1 (DMCLK2) signal is output from the AK5704, and the digital microphone outputs 1bit data, which is generated by ΔΣModulator, to DMDAT1 (DMDAT2). PMDM1A/B (PMDM2A/B) bits control power up/down of the digital block (Decimation Filter and HPF). PMAD1A/B (PMDM2A/B) bits settings do not affect the digital microphone power management. The DCLKE1 (DCLKE2) bit controls ON/OFF of the output clock from the DMCLK1 (DMCLK2) pin. When the AK5704 is power-up (PDN pin = “H”), external pull-down resistor (R) should be connected to the DMDAT1 (DMDAT2) pin to avoid floating state. Note that when using the digital microphone it does not support quad speed mode (fs ≥ 128 kHz).

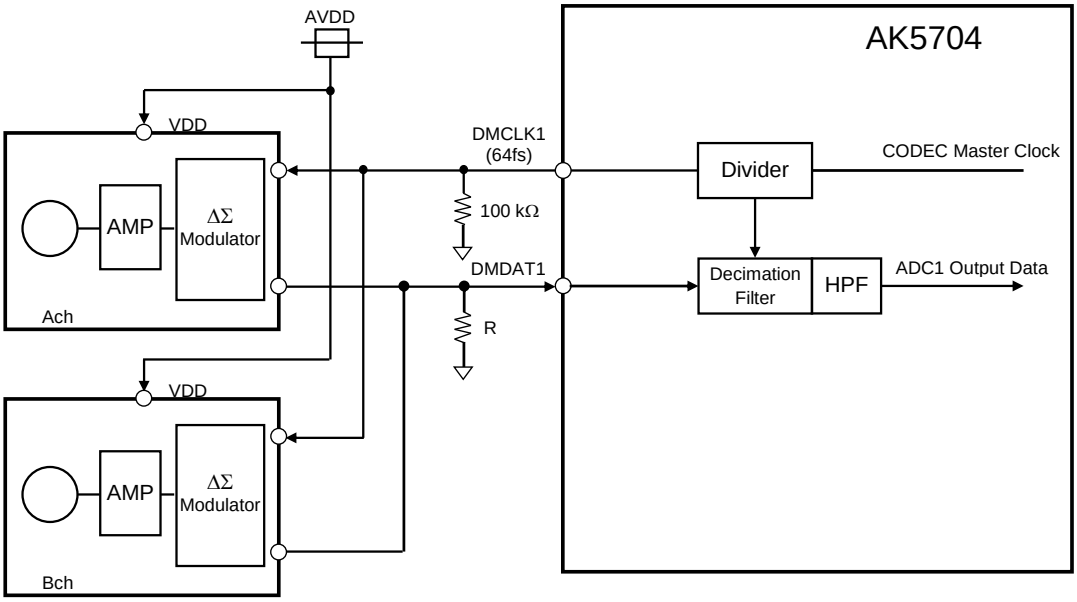


Figure 33. Connection Example of Stereo Digital Microphone (DMIC1 bit = “1”)

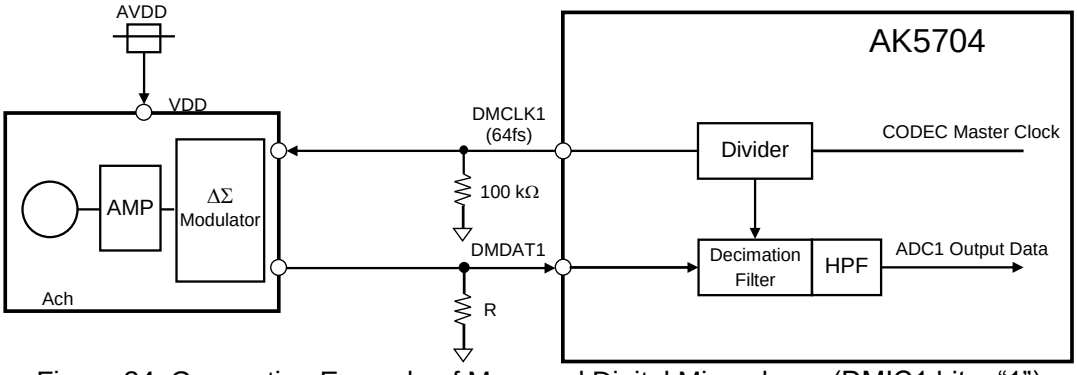


Figure 34. Connection Example of Monaural Digital Microphone (DMIC1 bit = “1”)

2. Interface

The input data channel of the DMDAT1 (DMDAT2) pin is set by DCLKP1 (DCLKP2) bit. When DCLKP1 (DCLKP2) bit = “0”, Ach data is input to the Decimation Filter if DMCLK1 (DMCLK2) signal = “L”, Bch data is input if DMCLK1 (DMCLK2) signal = “H”. When DCLKP1 (DCLKP2) bit = “1”, Bch data is input to the Decimation Filter if DMCLK1 (DMCLK2) signal = “L”, Ach data is input if DMCLK1 (DMCLK2) signal = “H”.

The DMCLK1 (DMCLK2) pin outputs “L” when DCLKE1 (DCLKE2) bit = “0”. DMCLK supports only 64fs and outputs same frequency. The DMCLK1 (DMCLK2) pin outputs 64fs clock when DCLKE1 (DCLKE2) bit = “1”. In this case, necessary clocks must be supplied to the AK5704 for ADC operation. The output data through “the Decimation and Digital Filters” is the negative full-scale with 0% 1’s density of 1bit output data and positive full-scale with the 100% 1’s density of 1bit output data.

Table 33. Digital MIC Data Input/Output Timing

DCLKP1/2 bit	DMCLK1/2 pin= “H”	DMCLK1/2 pin= “L”	
0	B ch	A ch	(default)
1	A ch	B ch	

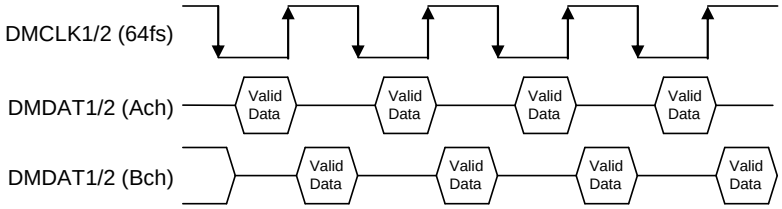


Figure 35. Digital MIC Data Input/Output Timing (DCLKP1/2 bit = “0”)

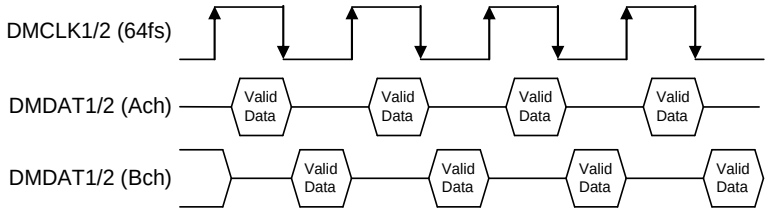
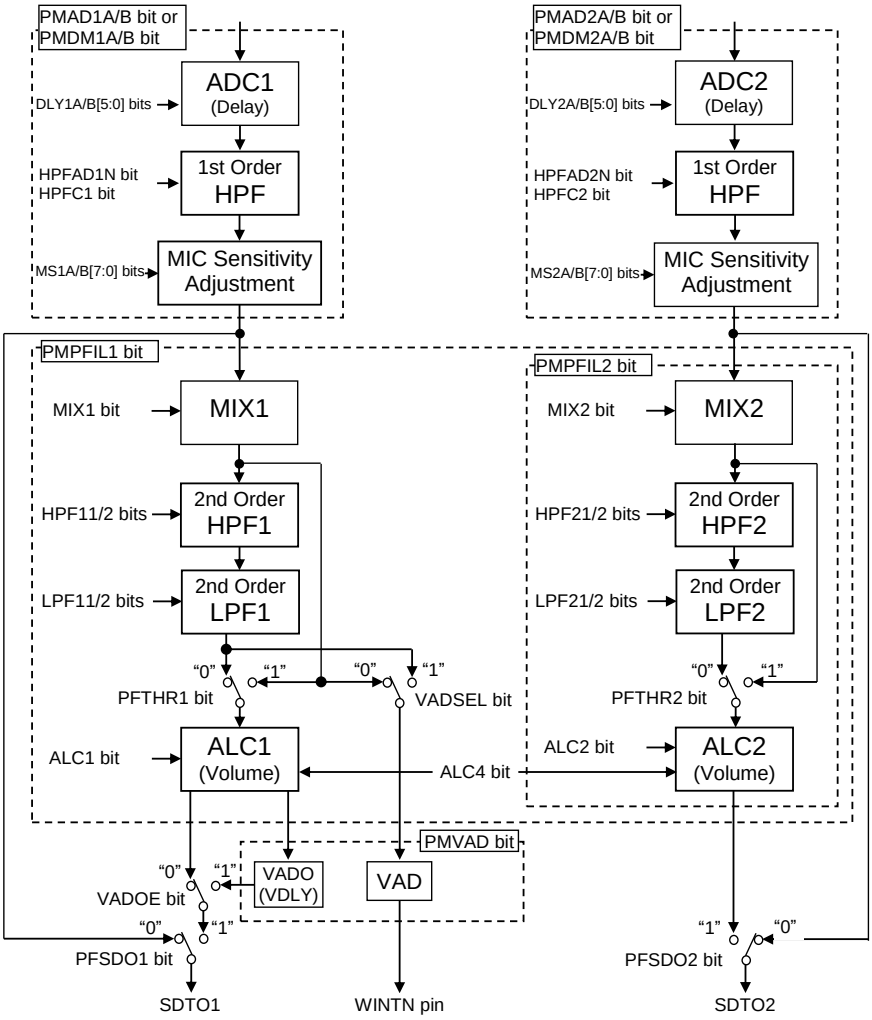


Figure 36. Digital MIC Data Input/Output Timing (DCLKP1/2 bit = “1”)

9.14. Digital Block

The digital block consists of the blocks shown in Figure 37. When PMPFIL1 bit = “1”, the programmable filter 1 consisting of MIX1, HPF1, LPF1 and ALC1 is powered up. When PMPFIL1 and PMPFIL2 bits = “1”, the programmable filter 2 consisting of MIX2, HPF2, LPF2 and ALC2 is powered up. When PFTHR1, PFTHR2 bit = “1”, the MIX1/2 output data bypasses HPF1/2 and LPF1/2 and is input to ALC1/2. When PFSDO1, PFSDO2 bit = “0”, the output data of MIC sensitivity Adjustment bypasses programmable filter 1/2 and outputs to SDTO1/2.



(1) ADC1/2: Includes the Digital Filter (LPF) and the Programmable Phase Adjustment.
(2) HPF: High Pass Filter for ADC.
(3) MIC Sensitivity Adjustment: Microphone Sensitivity Adjustment.
(4) MIX1/2: Mixer for Monaural Selection.
(5) HPF1/2: 2nd order High Pass Filter.
(6) LPF1/2: 2nd order Low Pass Filter.
(7) ALC1/2(Volume): Digital Volume with ALC Function.

Figure 37. Digital Block Path Select

9.14.1. Programmable Phase Adjustment

Output data is independently delayed in state of 64/fs (1/32fs) before the Decimation Filter to adjust the phase shift of each 4ch analog inputs into 4ch ADC. Setting resolution of delay amount is 1/64fs (1/32fs) and setting range is from 1/64fs (1/32fs) to 64/64fs (32/32fs). Delay function of AIN1A channel, AIN1B channel, AIN2A channel and AIN2B channel are independently controlled ON/OFF by DLY1AE bit, DLY1BE bit, DLY2AE bit and DLY2BE bits, respectively. When DLYxxE bit = "0", data delay is disable. When DLYxxE bit = "1", data data delay is enable.

DLY1A[5:0] bits: Setting the amount of delay for AIN1A channel.
DLY1B[5:0] bits: Setting the amount of delay for AIN1B channel.
DLY2A[5:0] bits: Setting the amount of delay for AIN2A channel.
DLY2B[5:0] bits: Setting the amount of delay for AIN2B channel.

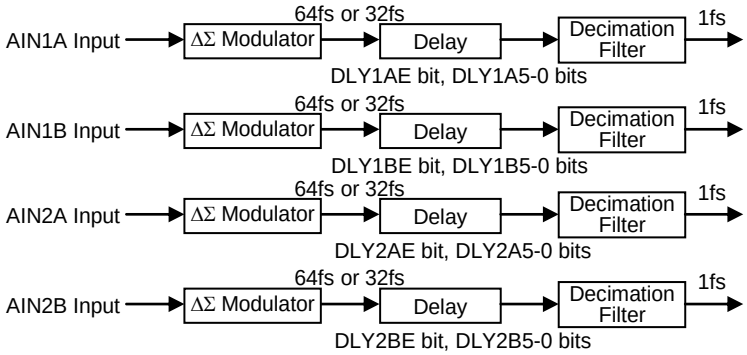


Figure 38. Programmable Phase Adjustment

Table 34. Programmable Phase Adjustment Setting (N/A: Not available)

DLY1A[5:0] bits DLY1B[5:0] bits DLY2A[5:0] bits DLY2B[5:0] bits	Delay		
	Except fs=176.4kHz, 192kHz	fs=176.4kHz, 192kHz	
00H	1/64fs	1/32fs	(default)
01H	2/64fs	2/32fs	
02H	3/64fs	3/32fs	
:	:	:	
1FH	32/64fs	32/32fs	
:	:	:	
3DH	62/64fs	N/A	
3EH	63/64fs	N/A	
3FH	64/64fs	N/A	

9.14.2. High Pass Filter (ADC1/2)

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies (fc) of the HPF are set by HPF1C[1:0] bits (ADC1), HPF2C[1:0] bits (ADC2). HPFAD1N, HPFAD2N bit controls the ON/OFF of the each HPF (HPF ON is recommended). It is proportional to the sampling frequency (fs) and the default value is 3.7Hz (@fs = 48kHz).

Table 35. ADC1/2 HPF Cut-off Frequency

HPF1C[1:0] bits HPF2C[1:0] bits	fc				
	fs = 16 kHz	fs = 48 kHz	fs = 96 kHz	fs = 192 kHz	
00	1.2 Hz	3.7 Hz	7.4 Hz	14.8 Hz	(default)
01	4.9 Hz	14.8 Hz	29.6 Hz	59.2 Hz	
10	19.7 Hz	59.2 Hz	118.4 Hz	236.8 Hz	
11	0.31 Hz	0.93 Hz	1.85 Hz	3.7 Hz	

The cut-off frequencies during initialization cycle will be high (Table 36) at FSTHPFAD1N = FSTHPFAD2N bit = “0” (default). When FSTHPFAD1N = FSTHPFAD2N bit = “1”, the setting of HPF1C[1:0] and HPF2C[1:0] bits are valid.

Table 36. ADC1/2 HPF Cut-off Frequency at Initialization Cycle (x: Do not care)

FSTHPFAD1N bit FSTHPFAD2N bit	HPF1C[1:0] bits HPF2C[1:0] bits	fs = 16 kHz	fs = 48 kHz	fs = 96 kHz	fs = 192 kHz	
0	xx	59.2 Hz	118.4 Hz	236.8 Hz	473.6 Hz	(default)
1	00	1.2 Hz	3.7 Hz	7.4 Hz	14.8 Hz	
	01	4.9 Hz	14.8 Hz	29.6 Hz	59.2 Hz	
	10	19.7 Hz	59.2 Hz	118.4 Hz	236.8 Hz	
	11	0.31 Hz	0.93 Hz	1.85 Hz	3.7 Hz	

9.14.3. ADC1/2 Digital Filter

The AK5704 has two types digital filter for ADC1/2 (Table 37). Short delay sharp roll-off filter or voice filter of ADC1/2 can be selected by ADVF bit. When voice filter is selected by ADVF bit = “1”, the maximum sampling frequency (fs) is 48kHz. If ADVF bit = “1” and the sampling frequency of ADC1/2 is 96kHz or 192kHz, the short delay sharp roll-off filter is selected automatically.

Table 37. ADC1/2 Digital Filter Selection

ADVF bit	Digital Filter	
0	Short Delay Sharp Roll-Off Filter	(default)
1	Voice Filter	

9.14.4. Microphone Sensitivity Adjustment

The AK5704 has linear microphone sensitivity adjustment function including mute controlled by MS1A/B[7:0], MS2A/B[7:0] bits to adjust the variation of the microphone sensitivity input to the AIN1A/B and AIN2A/B pins. MS1A/B[7:0], MS2A/B[7:0] bits must be set when PMAD1A/B, PMAD2A/B bits = "0".

MS1A[7:0] bits: Adjusting the microphone sensitivity for AIN1A channel.
MS1B[7:0] bits: Adjusting the microphone sensitivity for AIN1B channel.
MS2A[7:0] bits: Adjusting the microphone sensitivity for AIN2A channel.
MS2B[7:0] bits: Adjusting the microphone sensitivity for AIN2B channel.

Table 38. Microphone Sensitivity Adjustment

MS1A[7:0] bits MS1B[7:0] bits MS2A[7:0] bits MS2B[7:0] bits	MS_DATA	GAIN (dB)	Calculation	
00H	0	Mute	-	
01H	1	-42.144	$20 \log_{10}(MS\_DATA/128)$	(default)
02H	2	-36.124		
:	:	:		
7EH	126	-0.137		
7FH	127	-0.068		
80H	128	0.000		
81H	129	+0.068		
82H	130	+0.135		
:	:	:		
FDH	253	+5.918		
FEH	254	+5.952		
FFH	255	+5.987		

9.14.5. Monaural (MIX) Selection

ADC1/2 output data can be mixed to monaural by controlling MIX1/2 bits. ALC (ALC1/2 or ALC4 bit = "1") or digital volume (ALC1/2 = ALC4 bits = "0") operates for the data in Table 39.

Table 39. ADCx Monaural (MIX) Selection (x=1, 2)

MIXx bit	MONON bit	Ach Output Data	Bch Output Data	
0	0	ADCx Ach	ADCx Bch	(default)
	1	ADCx Ach	ADCx Bch	
1	0	(ADCx Ach+ADCx Bch)/2	"0" data	
	1	(ADCx Ach+ADCx Bch)/2	(ADCx Ach+ADCx Bch)/2	

9.14.6. High Pass Filter (HPF1/2)

This is composed with double 1st order HPF. The coefficient of HPF11/2 (HPF21/2) is set by FH1A[15:0], FH1B[15:0] bits (FH2A[15:0], FH2B[15:0] bits). HPF11/2 bits (HPF21/2 bits) control ON/OFF of the HPF11/2 (HPF21/2). When the HPF11/2 (HPF21/2) is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when HPF11/2 = HPF21/2 bits = "0". The HPF11/2 (HPF21/2) starts operation 4/fs (max) after when HPF11/2 = HPF21/2 bits = "1" is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 53)
HPF: FHxA[15:0] bits =A, FHxB[15:0] bits =B
(MSB=FHxA15, FxB15; LSB=FHxA0, FHxB0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as bellow.
$fc/fs \geq 0.000029$ (fc min = 5.6Hz at 192kHz)

9.14.7. Low Pass Filter (LPF1/2)

This is composed with double 1st order LPF. The coefficient of LPF11/2 (LPF21/2) is set by FL1A[15:0], FL1B[15:0] bits (FL2A[15:0], FL2B[15:0] bits). LPF11/2 bits (LPF21/2 bits) control ON/OFF of the LPF11/2 (LPF21/2). When the LPF11/2 (LPF21/2) is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when LPF11/2 = LPF21/2 bits = "0". The LPF11/2 (LPF21/2) starts operation 4/fs (max) after when LPF11/2 = LPF21/2 bits = "1" is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 53)
LPF: FLxA[15:0] bits =A, FLxB[15:0] bits =B
(MSB=FLxA15, FLxB15; LSB=FLxA0, FLxB0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as bellow.
$0.0125 \leq fc/fs < 0.5$ (fc min = 2.4kHz at 192kHz)

Note 53. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{15}

9.14.8. ALC Operation

The ALC (Automatic Level Control) is operated by ALC1 (2ch) block when ALC1 bit is "1" and operated by ALC2 (2ch) block when ALC2 bit is "1". In this case, both Ach and Bch VOL values are changed together. When ALC4 bit = "0" and ALC1 = ALC2 bits = "1", ALC of ADC1 and ADC2 are independently operated. When ALC4 bit = "1" regardless of ALC1 and ALC2 bits, ALC is operated for all 4ch of the ADC1 and ADC2. In this case, the VOL value is always changed in common with all channels. 4ch Link ALC is operated by the register setting of ADC1 (LMTH1[1:0], RGAIN1[2:0], REF1[7:0], RFST1[1:0] and ATTLIM1 bits). In this case, ALC setting of ADC2 (LMTH2[1:0], RGAIN2[2:0], REF2[7:0] and RFST2[1:0] bits) is invalid, but ATTLIM2 bit should be set to "0".

The ALC block consists of these blocks shown below. ALC limiter detection level and ALC recovery wait counter reset level are monitored at Level Detection 2 block after EQ block. The Level Detection 1 block also monitors clipping detection level (+0.53dBFS). ALC limiter gives priority to Level Detection 1.

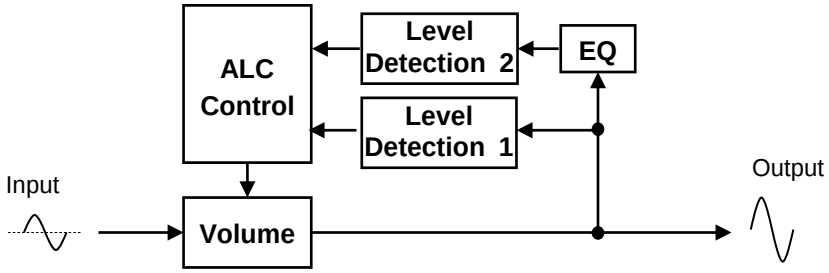


Figure 39. ALC Block

The polar (fc_1) and the zero-point (fs_2) frequencies of EQ block are dependent on the sampling frequency. The coefficient is changed automatically according to the sampling frequency range setting. When ALCEQ bit is OFF (ALCEQ bit = "1"), the level detection is not executed on EQ block.

Table 40. ALCEQ Frequency Setting

Sampling Frequency Range	Polar Frequency (fc1)	Zero-point Frequency (fc2)
8kHz ≤ fs ≤ 12kHz	150Hz @ fs=8kHz	100Hz @ fs=8kHz
12kHz < fs ≤ 24kHz	150Hz @ fs=16kHz	100Hz @ fs=16kHz
24kHz < fs ≤ 48kHz	150Hz @ fs=48kHz	100Hz @ fs=48kHz
48kHz < fs ≤ 96kHz	150Hz @ fs=96kHz	100Hz @ fs=96kHz
96kHz < fs ≤ 192kHz	150Hz @ fs=192kHz	100Hz @ fs=192kHz

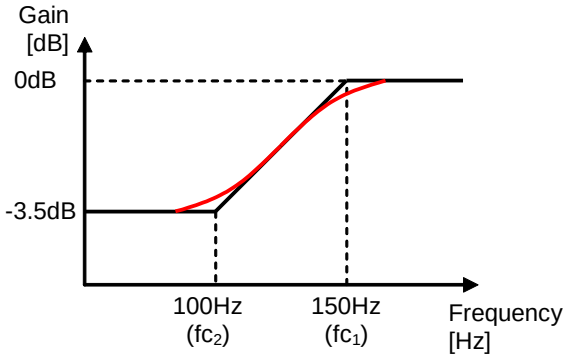
fs: Sampling frequency
fc_1: Polar frequency
fc_2: Zero-point frequency

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)},\quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)},\quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

[ALCEQ: First order zero pole high pass filter]



Note 54. Black: Diagrammatic Line, Red: Actual Line
Figure 40. ALCEQ Frequency Response (fs = 48kHz)

1. ALC Limiter Operation

During 2ch Link ALC limiter operation, when either A or B channel output level exceeds the ALC limiter detection level (Table 42), the VOL1/2 value (same value for both A and B) is attenuated automatically according to the output level (Table 43). During 4ch Link ALC limiter operation, when either A or B channel output level of ADC1 or ADC2 exceeds the ALC limiter detection level (Table 42), the VOL1/2 value (same value for both A and B) is attenuated automatically according to the output level (Table 43). This attenuation is repeated for sixteen times once ALC limiter operation is executed.

After completing the attenuate operation, unless ALC operation is changed to manual mode, the operation repeats when the input signal level exceeds ALC limiter detection level.

When ATTLMT1/2 bit = "1", VOL value is attenuated to 0dB if the volume is over ALC limiter detection level. In this case, attenuation under 0dB is not executed. The reference level and the input digital volume must be set to a value more than 0dB. When ATTLMT1/2 bit = "0" (default), normal attenuation is executed without volume limitation. When ALC 4ch Link Mode is selected (ALC4 bit = "1"), it is controlled by ATTLIM1 bit and ATTLIM2 bit should be set to "0".

Table 41. ALC Mode (x: Do not care)

Mode	ALC4 bit	ALC2 bit	ALC1 bit	ALC2 Operation	ALC1 Operation	
0	0	0	0	Manual	Manual	(default)
1	0	0	1	Manual	2ch Link	
2	0	1	0	2ch Link	Manual	
3	0	1	1	2ch Link	2ch Link	
4	1	x	x	4ch Link		

Note 55. ALC4 bit must be set when ALC1 = ALC2 bits = "0" or PMAD1A = PMAD1B = PMAD2A = PMAD2B bits = "0". When ALC4 bit = "1", only either ADC1 or ADC2 must not be power down.

Table 42. ALC Limiter Detection Level/ Recovery Counter Reset Level

LMTH1[1:0] bits LMTH2[1:0] bits	ALC Limiter Detection Level	ALC Recovery Counter Reset Level	
00	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	(default)
01	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	
10	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
11	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12dBFS	

Table 43. ALC Limiter ATT Step

Output Level	ATT Step [dB]
+0.53dBFS ≤ Output Level (Level Detection 1)	0.38148
–1.16dBFS ≤ EQ Output Level (Level Detection 2) < +0.53dBFS	0.06812
LM-LEVEL ≤ EQ Output Level (Level Detection 2) < –1.16dBFS	0.02548

2. ALC Recovery Operation

ALC recovery operation waits for the WTM[1:0] bits (Table 44) to be set after completing ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 42) during the wait time, ALC recovery operation is executed. The VOL value is automatically incremented by the setting value of RGAIN1/2[2:0] bits (Table 45) up to the set reference level (Table 46) in every sampling. When the VOL value exceeds the reference level (REF values), the VOL values are not increased. The recovery speed gets slower when the VOL peak level exceeds -12dBFS to make the recovery speed for low VOL level faster relatively.

When
"ALC recovery waiting counter reset level ≤ Output Signal < ALC limiter detection level"
during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level > Output Signal",
the waiting timer of ALC recovery operation starts.

ALC operations correspond to the impulse noise. When FRN bit = "0", the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to a microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1/2[1:0] bits (Table 47). Limiter amount of Fast recovery is set by FRATT[1:0] bits (Table 48). When FRN bit = "1", the fast recovery does not operate though the impulse noise is input.

Table 44. ALC Recovery Operation Waiting Period

WTM[1:0] bits	ALC Recovery Cycle	
00	128/fs	(default)
01	512/fs	
10	2048/fs	
11	8192/fs	

Table 45. ALC Recovery Gain Step

RGAIN1[2:0] bits RGAIN2[2:0] bits	GAIN Step [dB]	Gain Change Timing	
000	0.00212	1/fs	(default)
001	0.00106	1/fs	
010	0.00106	4/fs	
011	0.00106	8/fs	
100	0.00106	16/fs	
101	0.00106	32/fs	
110	0.00106	64/fs	
111	0.00106	128/fs	

Table 46. Reference Level of ALC Recovery Operation

REF1[7:0] bits REF2[7:0] bits	GAIN [dB]	Step	
F1H	+36.0	0.375 dB	
E0H	+35.625		
EFH	+35.25		
:	:		
E1H	+30.0		(default)
:	:		
92H	+0.375		
91H	0.0		
90H	–0.375		
:	:		
06H	–52.125		
05H	–52.5		
04H ~ 00H	MUTE		

Table 47. Fast Recovery Speed Setting (FRN bit = “0”)

RFST1[1:0] bits RFST2[1:0] bits	Fast Recovery Gain Step [dB]	
00	0.000265	(default)
01	0.00106	
10	0.00424	
11	0.01696	

Table 48. Fast Recovery Reference Volume Attenuation Step

FRATT[1:0] bits	ATT Step [dB]	ATT Switch Timing	
00	-0.00106	4/fs	(default)
01	-0.00106	16/fs	
10	-0.00106	64/fs	
11	-0.00106	256/fs	

3. Example of ALC Setting

Table 49 shows the examples of the ALC setting.

Table 49. Example of the ALC Setting

Register Name	Comment	fs=16kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH1/2[1:0]	Limiter detection Level	01	−4.1dBFS	01	−4.1dBFS
WTM[1:0]	Recovery waiting period	01	32ms	10	42.7ms
REF1/2[7:0]	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IV1A/B[7:0], IV2A/B[7:0]	Gain of IVOL	E1H	+30dB	E1H	+30dB
RGAIN1/2[2:0]	Recovery GAIN	001	0.00106dB	010	0.00106dB(4/fs)
RFST1/2[1:0]	Fast Recovery GAIN	11	0.01696dB	10	0.00424dB
ALCEQN	ALC EQ disable	0	Enable	0	Enable
ALC1/2	ALC enable	1	Enable	1	Enable

4. Example of registers set-up sequence of ALC operation

The following registers must not be changed during ALC operation. These bits must be changed after ALC operation is stopped by ALC1/2 = ALC4 bits = “0”.

・FRN, WTM[1:0], FRATT[1:0], ALCEQN, LMTH1/2[1:0], RFST1/2[1:0] and RGAIN1/2[2:0] bits

The reference level can be changed during ALC operation. If the reference level is reduced the volume level is changed by soft transition in 0.02548dB/fs step. The volume is also changed by soft transition to the IVOL setting value (IV1A/B[7:0], IV2A/B[7:0] bits) until manual mode starts after ALCx bit is set to “0”. Do not change the REF value during soft transition when REF1/2[7:0] bits are set to 00H (MUTE).

When changing ALC operation channels, finish all ALC operations at first (ALC4 = ALC2 = ALC1 bits= “0”) and write ALCx bit = “1”. In this case, ALCx bit writing must be made with an interval of 2/fs. It is recommended that ALC operation is enabled after transition time since the volume changes to the IVOL setting value by soft transition when ALC operation is finished.

The reference level and IVOL must be set to a value more than 0dB when ATTLMT1/2 bits = “1”.

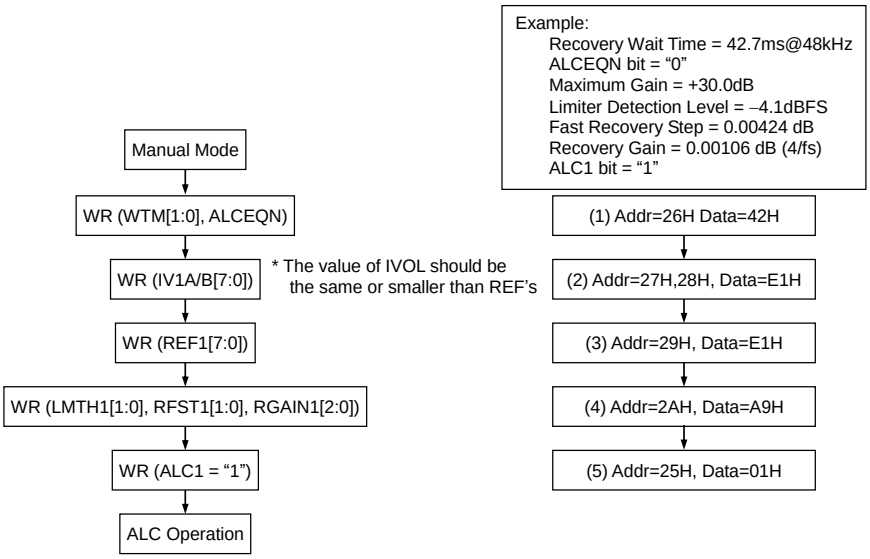


Figure 41. ALC Operation Setting Sequence

9.14.9. Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode when ALC4 = ALC2 = ALC1 bits= “0”. This mode is used in the cases shown below.

1. After exiting reset state, when setting up the registers for ALC operation (LMTH1/2 bits and etc.)
2. When the registers for ALC operation (Limiter period, Recovery period and etc.) are changed. For example; when the sampling frequency is changed.
3. When IVOL is used as a manual volume control.

IV1A/B[7:0] and IV2A/B[7:0] bits set the gain of the digital input volume (Table 50). 1Ach and 1Bch volumes are set individually by IV1A[7:0] and IV1B[7:0] bits when IVOL1C bit = “0”. IV1A[7:0] bits control both 1Ach and 1Bch volumes together when IVOL1C bit = “1”. 2Ach and 2Bch volumes are set individually by IV2A[7:0] and IV2B[7:0] bits when IVOL2C bit = “0”. IV2A[7:0] bits control both 2Ach and 2Bch volumes together when IVOL2C bit = “1”. This volume control has a soft transition function at 0.09375dB/fs (IVTM[1:0] bits = “01”). Therefore, no switching noise occurs during the transition. When IVTM[1:0] bits = “01”, it takes 944/fs from F1H(+36dB) to 05H(-52.5dB). The volume is muted after transitioned to -72dB (208/fs) in the period set by IVTM[1:0] bits when changing the volume from 05H (-52.5dB) to 00H (MUTE). When IV1A/B[7:0] bits and IV2A/B[7:0] bits are set in series, should be set at soft transition time interval.

If IV1A/B[7:0] or IV2A/B[7:0] bits are written during PMPFIL1/2 bits = “0”, IVOL operation starts with the written values after PMPFIL1/2 bits are changed to “1”.

Table 50. Input Digital Volume Setting

IV1A/B[7:0] bits IV2A/B[7:0] bits	GAIN [dB]	Step	
F1H	+36.0	0.375 dB	
E0H	+35.625		
EFH	+35.25		
:	:		
E1H	+30.0		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	–0.375		
:	:		
06H	–52.125		
05H	–52.5		
04H ~ 00H	MUTE		

Table 51. Transition Time Setting of Input Digital Volume

IVTM[1:0] bits	Transition Time from F1H to 05H (IV1A/B[7:0], IV2A/B[7:0] bits)					
	Setting	fs=16kHz	fs=48kHz	fs=96kHz	fs=192kHz	
00	236/fs	14.8ms	4.9ms	2.5ms	1.2ms	
01	944/fs	59ms	19.7ms	9.8ms	4.9ms	(default)
10	1888/fs	118ms	39.3ms	19.7ms	9.8ms	
11	3776/fs	236ms	78.7ms	39.3ms	19.7ms	

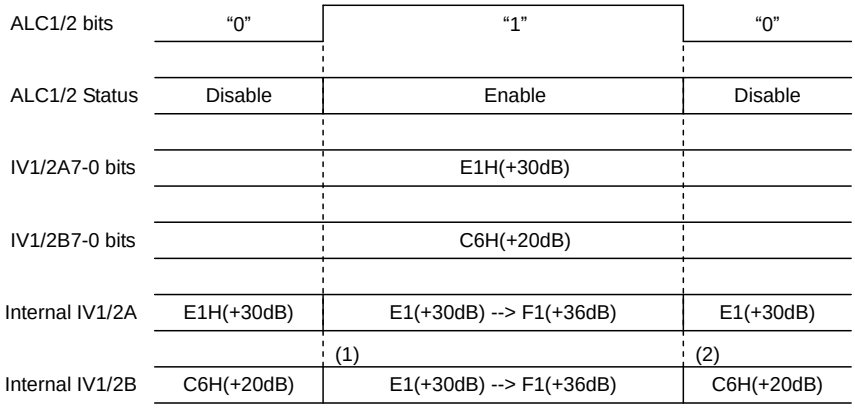


Figure 42. Example of IVOL value during 2ch ALC (ALC4 bit = "0")

(1) The IV1A and IV2A value becomes the start value if the IV1A and IV1B, IV2A and IV2B are different when an ALC operation starts. The wait time from ALC1/2 bits = "1" to ALC operation start by IV1/2A[7:0] bits is at most recovery time (WTM[1:0] bits).
(2) Writing to IV1A/B and IV2A/B registers is ignored during ALC operation. After ALC is disabled, the IVOL changes to each IV1A/B or IV2A/B value by soft transition. When ALC is enabled again, ALC1/2 bits should be set to "1" with an interval more than soft transition time after ALC1/2 bit = "0".

9.14.10. ALC 4ch Link Mode Sequence

Figure 43 shows the 4ch Link ALC Mode sequence at ALC1 = ALC2 bits = "0", when ALC4 bit = "0" → "1".

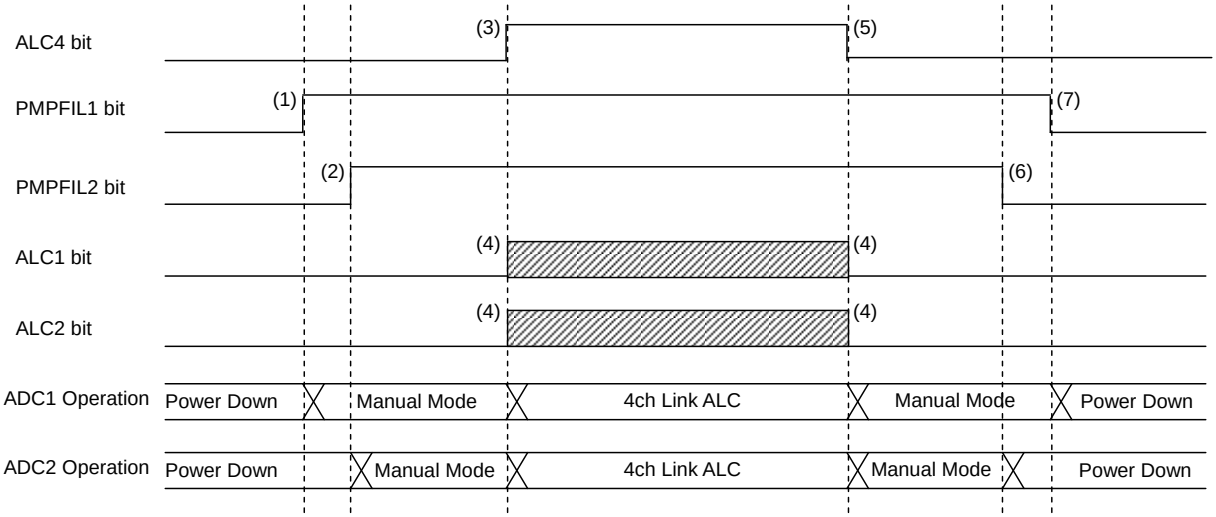


Figure 43. 4ch Link ALC Mode Sequence (ALC4 bit = "1")

(1) Programmable Filter 1 is powered up by PMPFIL1 bit is changed from "0" to "1".
(2) Programmable Filter 2 is powered up by PMPFIL2 bit is changed from "0" to "1".
(3) Both ADC1 and ADC2 start ALC operation together (4ch Link ALC) by changing ALC4 bit from "0" to "1". At this point the start value of ALC is Ach of ADC1 (IV1A[7:0] bits).
(4) When ALC4 bit = "1", ALC1 bit and ALC2 bit become invalid. But ALC1 and ALC2 bits should be "0", when ALC4 bit is changed.
(5) When ALC4 bit = "1" → "0", ADC1 and ADC2 become Manual Mode. 2ch link mode can also be set without stopping operation by setting ALC1 and ALC2 bits = "1".
(6) Programmable Filter 2 is powered down by PMPFIL2 bit is changed from "1" to "0".
(7) Programmable Filter 1 is powered down by PMPFIL1 bit is changed from "1" to "0".

9.15. Digital Voice Activity Detector

The AK5704 has a Voice Activity Detector (VAD) function. VAD operation requires to supply MCKI input and to operate an analog microphone and ADC or a digital microphone.

By setting each parameter, an interrupt signal is output to the WINTN pin for the external DSP (SoC) in response to the voice input from MIC. Then, the voice input from MIC is output to the SDTO1 pin.

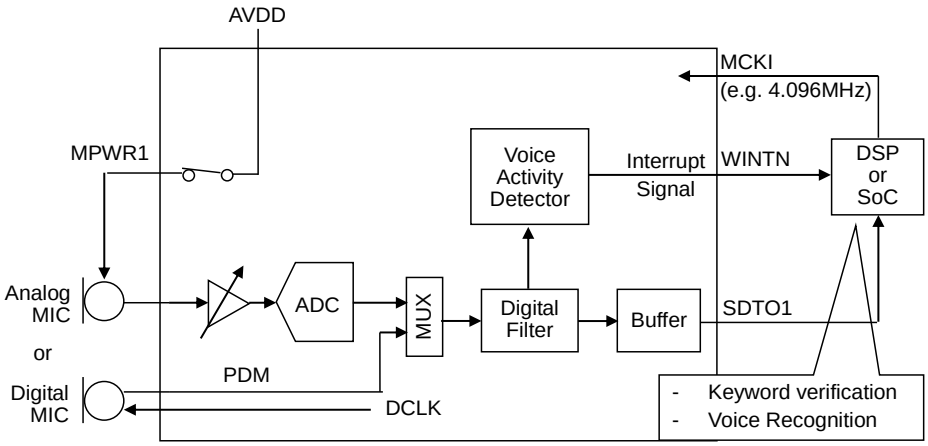


Figure 44. Voice Activity Detector System Block Diagram

VAD is a function to detect a large sound in ambient noise. VAD has a delay circuit to save speech data prior to the point which the voice is detected.

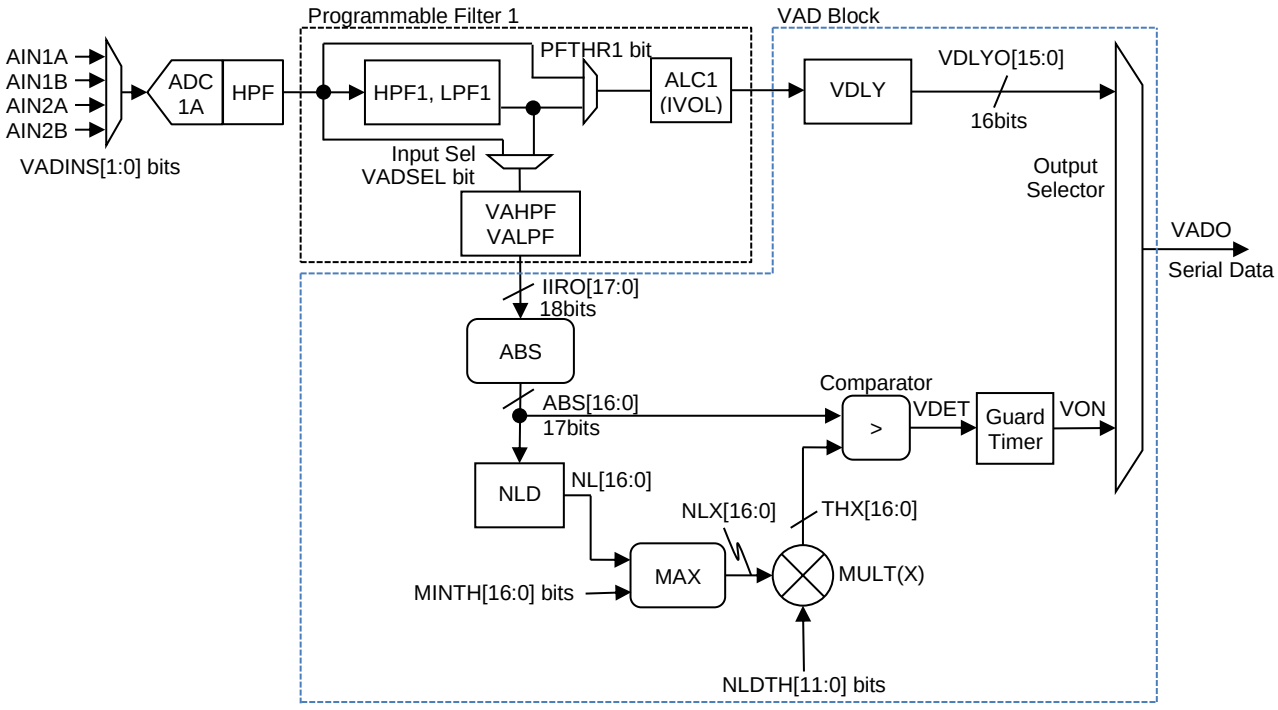


Figure 45. Voice Activity Detector Block Diagram

Input signal to ADC1 is selected by VADINS[1:0] bits, and the corresponding microphone input circuit is powered up by setting PMAINx bit = “1”. When the ADC1 and the Programmable Filter 1 are powered up by setting PMAD1A = PMPFIL1 bits = “1”, a signal is input to the VAD circuit.

Table 52. ADC1 Input Signal Select

VADINS[1:0] bits	ADC1 Input Signal	
00	AIN1A	(default)
01	AIN1B	
10	AIN2A	
11	AIN2B	

VAD circuit is powered up by setting PMVAD bit = “1”. When the VAD is powered down, NLD (Noise Level Detector) is also reset the leaning data by resetting the VAD circuit. The default value of NLD part is zero. Each register related to VAD should be set during PMVAD bit = “0” (Do not change the set value during operation.)

Table 53. Voice Activity Detector Power Management

PMVAD bit	VAD Operation	
0	Power down (Reset)	(default)
1	Normal operation	

Input signal to VAD circuit is selected by VADSEL bit.

Table 54. Select Input Signal for VAD

VADSEL bit	Input Signal for VAD	
0	ADC output	(default)
1	HPF/LPF output	

9.15.1. VDLY

VDLY block outputs the signal according to VDLYO[15:0] bits which is delayed input data. These data are used when the speech data which is before voice detection is necessary for subsequent process. SRAM is used to create delay. SRAM size is 2048word x 16bit. The ON/OFF control of VDLY block is selectable by DLYE bit. Non-delay data is output when this function is disabled. SRAM is initialized when the reset is released.

Table 55. VAD Delay Setting

DLYE bit	Amount of Delay	
0	No-delay	(default)
1	2048 sample (128ms @ fs=16kHz)	

9.15.2. HPF, LPF

In addition to 2nd order HPF and LPF of Programmable Filter 1, 2nd order HPF and LPF are built in for VAD. After passing through HPF and LPF, the output value IIRO [17: 0] is input to the ABS section of the next stage.

High Pass Filter (VAHPF)

This is composed with double 1st order HPF. The coefficient of VAHPF1/2 is set by VFHA[15:0], VFHB[15:0] bits. VAHPF1 bit (VAHPF2 bit) control ON/OFF of the VAHPF1 (VAHPF2). When the VAHPF1 (VAHPF2) is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when VAHPF1 = VAHPF2 bits = “0”. The VAHPF1 (VAHPF2) starts operation 4/fs (max) after when VAHPF1 = VAHPF2 bits = “1” is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 56)
VAHPF: VFHA[15:0] bits =A, VFHB[15:0] bits =B
(MSB=VFHA15, VFHB15; LSB=VFHA0, VFHB0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as bellow.
$fc/fs \geq 0.000029$ (fc min = 5.6Hz at 192kHz)

Low Pass Filter (VALPF)

This is composed with double 1st order LPF. The coefficient of VALPF1/2 is set by VFLA[15:0], VFLB[15:0] bits. VALPF1 bit (VALPF2 bit) control ON/OFF of the VALPF1 (VALPF2). When the VALPF1 (VALPF2) is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when VALPF1 = VALPF2 bits = "0". The VALPF1 (VALPF2) starts operation 4/fs (max) after when VALPF1 = VALPF2 bits = "1" is set. When HPF3RD bit is set to "1", VALPF1 can be changed to HPF. In this case, the coefficient setting is followed VFHA[15:0] and VFHB[15:0] bits.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 56)
VALPF: VFLA[15:0] bits =A, VFLB[15:0] bits =B
(MSB=VFLA15, VFLB15; LSB=VFLA0, VFLB0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as bellow.
$0.0125 \leq fc/fs < 0.5$ (fc min = 2.4kHz at 192kHz)

Note 56. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{15}

9.15.3. ABS

ABS simply calculates an absolute value.

1. If most significant bit of sign bit is 0, all bit except for most significant bit will be directly output.
2. If most significant bit of sign bit is 1, all bit except for most significant bit will be added +1 after bit inverting and output.

9.15.4. NLD (Noise Level Detector)

NLD (Noise Level Detector) detects a noise level of the input signal.

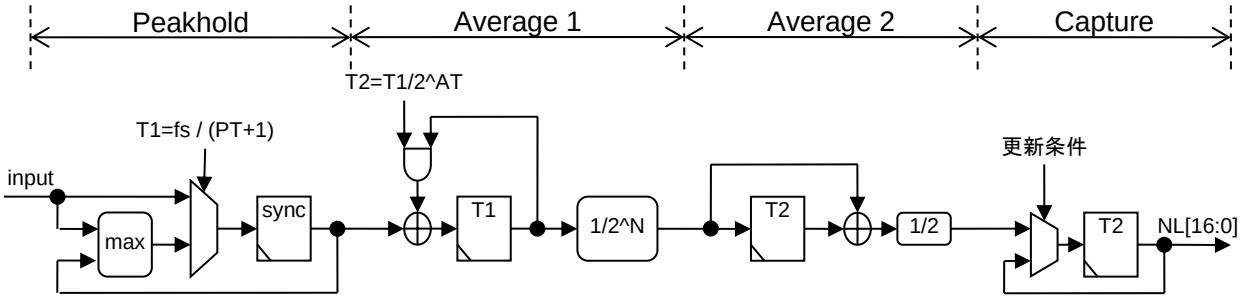


Figure 46. Noise Level Detector Block Diagram

The peak value is calculated according to the setting of PT[7:0] bits in the Peak-hold stage.

Table 56. Peak Value Setting

PT[7:0] bits	Number of Samples	Update Rate T1 [Hz]	Calculating Period [μs] @ fs=16kHz	
N	N+1	fs/(N+1)	62.5 * (N+1)	
00H	1	fs	62.5	
:	:	:	:	
07H	8	fs/8	500	(default)
:	:	:	:	
1FH	32	fs/32	2,000	
:	:	:	:	
FFH	256	fs/256	16,000	

The peak value is calculated according to the setting of AT[3:0] bits in the Average1 and Average2 stage.

Table 57. Average of Peak Value Setting

AT[3:0] bits	Average1 Number of Samples	Average 1 Shift Amount N	Average 2 Number of Samples	Total Number of Samples	Update Rate T2 [Hz]	
0000	1	0	2	2	T1/1	
0001	2	1	2	4	T1/2	
0010	4	2	2	8	T1/4	
0011	8	3	2	16	T1/8	
0100	16	4	2	32	T1/16	
0101	32	5	2	64	T1/32	
0110	64	6	2	128	T1/64	
0111	128	7	2	256	T1/128	(default)
1000	256	0	2	512	T1/256	
1001	512	1	2	1024	T1/512	
1010	1024	2	2	2048	T1/1024	
1011	2048	3	2	4096	T1/2048	
1100	4096	4	2	8192	T1/4096	
1101	8192	5	2	16384	T1/8192	
1110	16384	6	2	32768	T1/16384	
1111	32768	7	2	65536	T1/32768	

NL (Noise Level) update execution is determined in the Capture stage. In the following condition, NL is updated.

<VON = “0”>
(Noise level reaches to the voice level unless stopping NLD during speech detection. To prevent this, noise level is updated in this condition.)

<VON = "1" lasts for 0XFFFF samples (4.096s@16kHz)>
(When VON becomes “1” due to a false detection by sudden increase of noise level, NLD stops updating. To prevent this, noise level is updated in this condition.)

* 0xFFFF samples is default setting (VONT bit = “0”). When VONT bit is set to “1”, the number of samples is changed to 0x7FFF (2.048s@16kHz).

NL Limiter Function

When NL increases following the input signal, there is a possibility that voice activity cannot be detected depending on the setting of NLDTH[11:0] bits. It is an optional function considering such a situation. It can prevent a sudden increase of noise level according to the data limit by NLLIM[1:0] bits at the next NL update.

Table 58. Noise Level Limiter Value Setting

NLLIM[1:0] bits	Noise Level Limiter Value at Next NL Update	
00	No-limit	(default)
01	+2dB	
10	+3dB	
11	+4dB	

9.15.5. MAX

The minimum noise level is set to MINTH[16:0] bits (unsigned). A larger value of MINTH[16:0] bits (unsigned) and NL[16:0] bits (output level of NLD block, unsigned) is output to NLX[16:0] bits. This setting can prevent the NLD reacts sensitively in a quiet environment.

Table 59. Minimum Noise Level Setting

MINTH[16:0] bits	Minimum Noise Level [dBFS]	
N	20*log(N/2^17)	
00000H	-∞	
:	:	
0001FH	-72.2	(default)
:	:	
00048H	-65.2	
:	:	
10000H	-6.0	
:	:	
1FFFFH	0	

9.15.6. MULT (X)

The speech detection threshold level (THX[16:0] bits) is calculated by multiplying noise level threshold (NLDTH[11:0] bits) by ambient noise level (NLX[16:0] bits) which is determined according to NLD and MAX blocks. Multiplication result outputs 17-bit data. If multiplication result is greater than 17-bit full scale, output data is saturated to 0x1FFFF.

Table 60. Noise Level Threshold

NLDTH[11:0] bits	Noise Level Threshold [dB]	
N	20*log(N/2^7)	
000H	-∞	
:	:	
080H	+0.0	
:	:	
200H	+12.0	(default)
:	:	
7EDH	+24.0	
:	:	
FFFH	+30.1	

9.15.7. Comparator (>)

In case of output value of ABS block > THX[16:0] bits, the comparator outputs VDET = “H”.
In case of output value of ABS block ≤ THX[16:0] bits, the comparator outputs VDET = “L”.

9.15.8. Guard Timer

<On guard Timer>
The output condition of VON = "H" can be limited by ONGT[7:0] bits which define a number of continuous detection times of VDET = "H".

<Off guard Timer>
OFFGT[7:0] bits which define a number of continuous detection times of VDET = “L” can set a determined period that keeps VON = "H" after VON = "L" detection.

Table 61. On Guard Timer Setting

ONGT[7:0] bits	VON↑ Condition A Number of VDET= “H”	
N	N+1	
00H	1	
01H	2	(default)
02H	3	
:	:	
FFH	256	

Table 62. Off Guard Timer Setting

OFFGT[7:0] bits	VON↓ Condition A Number of VDET = “L”	Time @ fs = 16kHz [ms]	
N	(N+1)*2^8	0.0625 * (N+1)*2^8	
00H	256	16	
:	:	:	
0FH	4,096	256	(default)
:	:	:	
FFH	65,536	4096	

9.15.9. Interrupt Output (WINTN pin)

The WINTN pin holds “H” output when voice activity is not detected (VON = “L”). When the voice activity is detected (VON = “H”), the WINTN pin output is changed to “L”.

9.15.10. Output Selector

VADO output is selectable by setting VAS[2:0] bits or VBS[2:0] bits. VAS[2:0] bits determine Ach output, and VBS[2:0] bits determine Bch output.

When VADOE bit is set to “1”, VADO is started to output from the SDTO1 pin. (When VADOE bit = “0” (default), the data of ADC1 or Programmable Filter 1 is output from SDTO1 pin.)

Table 63. Output Selector Setting

VAS[2:0] bits VBS[2:0] bits	Ach Output [15:0] Bch Output [15:0]	
000	VDLYO[15:0]	(default)
001	VON=0: 0x0000 VON=1: VDLYO[15:0]	
010	VON=0: 0x0000 VON=1: 0x2710 (10000dec)	
011	NL[16:1]	
100	ABS[16:1]	
101	THX[16:1]	
110	IIRO[17:2]	
111	VDET=0: 0x0000 VDET=1: 0x2710 (10000dec)	

9.16. I2C-bus Control Interface

The AK5704 supports the fast-mode I²C Bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to (TVDD+0.3)V or less.

1. WRITE Operation

Figure 47 shows the data transfer sequence for the I²C Bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 53). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as “001000” (Figure 48). If the slave address matches that of the AK5704, the AK5704 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 54). A R/W bit value of “1” indicates that the read operation is to be executed, and “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK5704. The format is MSB first, and those most significant 1bit is fixed to zero (Figure 49). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 50). The AK5704 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 53).

The AK5704 can perform more than one byte write operation per sequence. After receipt of the third byte the AK5704 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. The address counter will “roll over” to 00H and the previous data will be overwritten if the address exceeds “46H” prior to generating a stop condition.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 55) except for the START and STOP conditions.

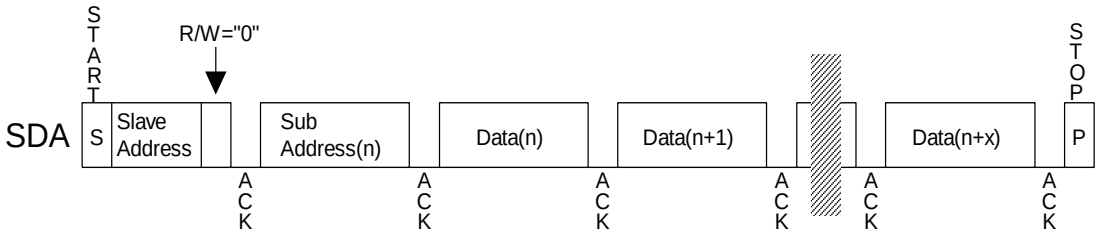


Figure 47. Data Transfer Sequence at I²C Bus Mode

0	0	1	0	0	0	CAD	R/W

(CAD must match with CAD pin.)
Figure 48. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 49. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 50. The Third Byte

2. READ Operation

Set the R/W bit = “1” for the READ operation of the AK5704. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. The address counter will “roll over” to 00H and the data of 00H will be read out if the address exceeds “46H” of Register map prior to generating a stop condition.

The AK5704 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK5704 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK5704 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK5704 ceases the transmission.

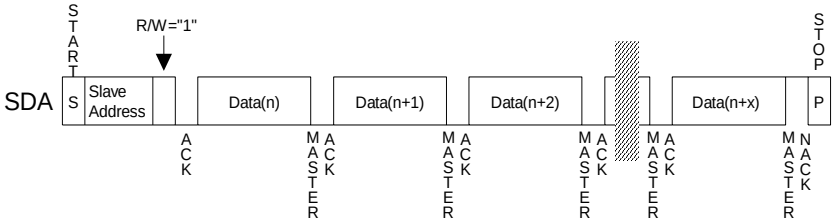


Figure 51. Current Address Read

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK5704 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK5704 ceases the transmission.

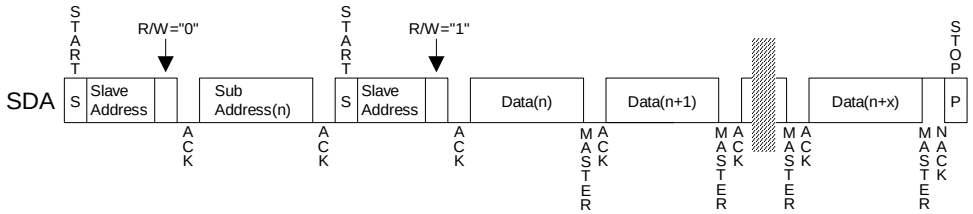


Figure 52. Random Address Read

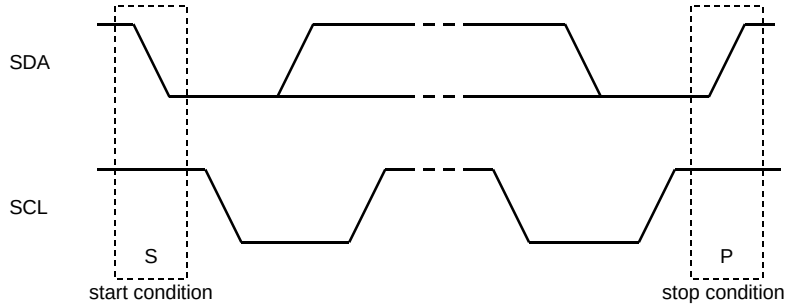


Figure 53. Start Condition and Stop Condition

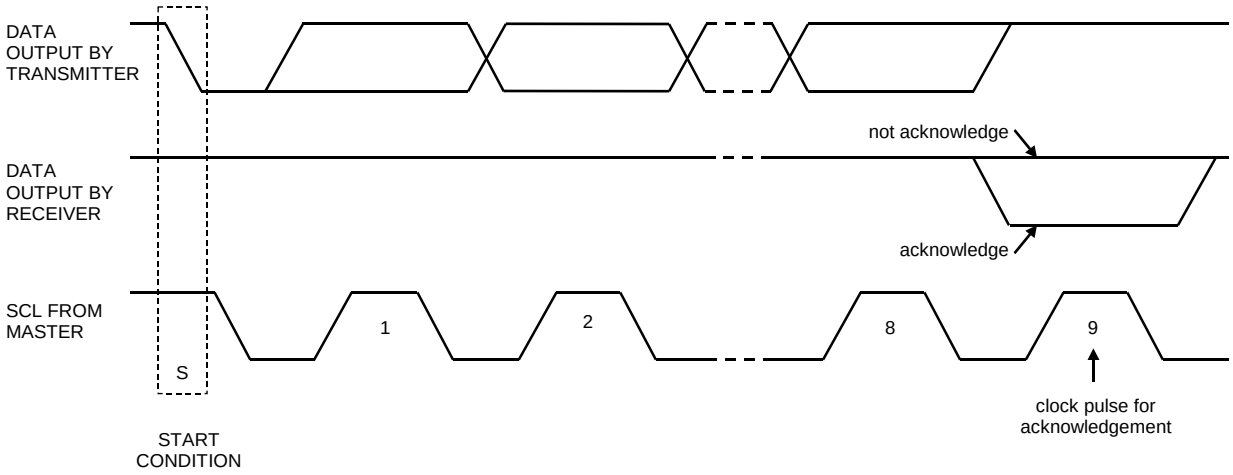


Figure 54. Acknowledge (I^2C Bus)

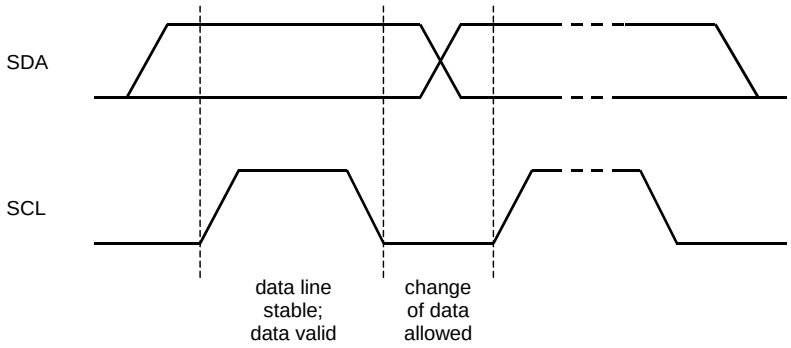


Figure 55. Bit Transfer (I^2C Bus)

9.17. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Flow Control	0	SDTO2E	MSN	AVDDL	0	PSW2N	PSW1N	PSW0N
01H	Power Management 1	PMVCM	PMPLL	PMMP2	PMMP1	PMAIN2B	PMAIN2A	PMAIN1B	PMAIN1A
02H	Power Management 2	PMDM2B	PMDM2A	PMDM1B	PMDM1A	PMAD2B	PMAD2A	PMAD1B	PMAD1A
03H	Power Management 3	AIRST[2:0]			PMVAD	PFSDO2	PFSDO1	PMPFIL2	PMPFIL1
04H	MIC Input & MIC Power Setting	MDIF2B	MDIF2A	MDIF1B	MDIF1A	AINCOM	MONON	MICL[1:0]	
05H	MIC Amplifier 1 Gain	MG1B[3:0]				MG1A[3:0]			
06H	MIC Amplifier 2 Gain	MG2B[3:0]				MG2A[3:0]			
07H	Digital MIC Setting	0	DCLKP2	DCLKE2	DMIC2	0	DCLKP1	DCLKE1	DMIC1
08H	Clock Mode Select	0	0	CM[1:0]		FS[3:0]			
09H	PLL CLK Source Select	0	0	BCKO	MCKOE	0	0	PLS	0
0AH	PLL Ref CLK Divider 1	PLD[15:8]							
0BH	PLL Ref CLK Divider 2	PLD[7:0]							
0CH	PLL FB CLK Divider 1	PLM[15:8]							
0DH	PLL FB CLK Divider 2	PLM[7:0]							
0EH	Audio I/F Format	0	BCKP	DLC[1:0]		TDM[1:0]		DIF[1:0]	
0FH	Phase Adjustment 1A	DLY1AE	0	DLY1A[5:0]					
10H	Phase Adjustment 1B	DLY1BE	0	DLY1B[5:0]					
11H	Phase Adjustment 2A	DLY2AE	0	DLY2A[5:0]					
12H	Phase Adjustment 2B	DLY2BE	0	DLY2B[5:0]					
13H	ADC High Pass Filter	0	ADRST[2:0]			HPF2C[1:0]		HPF1C[1:0]	
14H	Digital Filter Select	ADVF	0	0	FSTHPFAD2N	FSTHPFAD1N	VREFH	HPFAD2N	HPFAD1N
15H	MIC Sensitivity Adj. 1A	MS1A[7:0]							
16H	MIC Sensitivity Adj.1B	MS1B[7:0]							
17H	MIC Sensitivity Adj.2A	MS2A[7:0]							
18H	MIC Sensitivity Adj.2B	MS2B[7:0]							
19H	Filter 1 Select	PFTHR1	0	0	MIX1	LPF12	LPF11	HPF12	HPF11
1AH	Filter 2 Select	PFTHR2	0	0	MIX2	LPF22	LPF21	HPF22	HPF21
1BH	VAD Setting 1	VALPF2	VALPF1	VAHPF2	VAHPF1	HPF3RD	VADSEL	DLYE	VADOE
1CH	VAD Setting 2	PT[7:0]							
1DH	VAD Setting 3	VADINS[1:0]		NLLIM[1:0]		0	0	0	MINTH16
1EH	VAD Setting 4	MINTH[15:8]							
1FH	VAD Setting 5	MINTH[7:0]							
20H	VAD Setting 6	AT[3:0]				NLDTH[11:8]			
21H	VAD Setting 7	NLDTH[7:0]							
22H	VAD Setting 8	ONGT[7:0]							
23H	VAD Setting 9	OFFGT[7:0]							
24H	VAD Setting 10	VONT	VBS[2:0]			0	VAS[2:0]		

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
25H	ALC Select	FRN	ATTLIM2	ATTLIM1	0	0	ALC4	ALC2	ALC1
26H	ALC Control 1	IVTM[1:0]		0	ALCEQN	FRATT[1:0]		WTM[1:0]	
27H	Input Digital Volume 1A	IV1A[7:0]							
28H	Input Digital Volume 1B	IV1B[7:0]							
29H	ALC1 Reference Level	REF1[7:0]							
2AH	ALC1 Control	IVOL1C	RGAIN1[2:0]			RFST1[1:0]		LMTH1[1:0]	
2BH	Input Digital Volume 2A	IV2A[7:0]							
2CH	Input Digital Volume 2B	IV2B[7:0]							
2DH	ALC2 Reference Level	REF2[7:0]							
2EH	ALC2 Control	IVOL2C	RGAIN2[2:0]			RFST2[1:0]		LMTH2[1:0]	
2FH	HPF1 Coefficient A	FH1A[15:8]							
30H	HPF1 Coefficient A	FH1A[7:0]							
31H	HPF1 Coefficient B	FH1B[15:8]							
32H	HPF1 Coefficient B	FH1B[7:0]							
33H	LPF1 Coefficient A	FL1A[15:8]							
34H	LPF1 Coefficient A	FL1A[7:0]							
35H	LPF1 Coefficient B	FL1B[15:8]							
36H	LPF1 Coefficient B	FL1B[7:0]							
37H	HPF2 Coefficient A	FH2A[15:8]							
38H	HPF2 Coefficient A	FH2A[7:0]							
39H	HPF2 Coefficient B	FH2B[15:8]							
3AH	HPF2 Coefficient B	FH2B[7:0]							
3BH	LPF2 Coefficient A	FL2A[15:8]							
3CH	LPF2 Coefficient A	FL2A[7:0]							
3DH	LPF2 Coefficient B	FL2B[15:8]							
3EH	LPF2 Coefficient B	FL2B[7:0]							
3FH	VAHPF Coefficient A	VFHA[15:8]							
40H	VAHPF Coefficient A	VFHA[7:0]							
41H	VAHPF Coefficient B	VFHB[15:8]							
42H	VAHPF Coefficient B	VFHB[7:0]							
43H	VALPF Coefficient A	VFLA[15:8]							
44H	VALPF Coefficient A	VFLA[7:0]							
45H	VALPF Coefficient B	VFLB[15:8]							
46H	VALPF Coefficient B	VFLB[7:0]							

Note 57. Register values are initialized by setting the PDN pin to “L”.
Note 58. It is prohibited to write “1” to the bits indicated as “0“.
Note 59. Writing access to 47H ~ 7FH is prohibited.

9.18. Register Definition

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Flow Control	0	SDTO2E	MSN	AVDDL	0	PSW2N	PSW1N	PSW0N
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PSW2N/1N/0N: Pull-down Resistance Disable bits (Table 1)
0: Pull-down Enable (Typ. 49 kΩ) (default)
1: Pull-down Disable

AVDDL: AVDD Internal Operation Mode
0: 3.3V Operation (default)
1: 1.8V Operation

MSN: Master/Slave Setting (Table 16, Table 17, Table 18, Table 19)
0: Slave Mode (default)
1: Master Mode

SDTO2E: SDTO2 Enable
0: Disable (TDMIN pin: Default)
1: Enable (SDTO2 pin)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 1	PMVCM	PMPLL	PMMP2	PMMP1	PMAIN2B	PMAIN2A	PMAIN1B	PMAIN1A
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMAIN1A/B: Power Management of AIN1A/B Inputs
0: Power down (default)
1: Power up

PMAIN2A/B: Power Management of AIN2A/B Inputs
0: Power down (default)
1: Power up

PMMP1/2: Power Management of MPWR1/2 (Table 26)
0: Power down: Hi-Z (default)
1: Power up

PMPLL: Power Management of PLL
0: Power down (default)
1: Power up

PMVCM: Power Management of VCOM
0: Power down (default)
1: Power up
After setting AVDDL bit, VCOM must be powered up (PMVCM bit = “1”).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Power Management 2	PMDM2B	PMDM2A	PMDM1B	PMDM1A	PMAD2B	PMAD2A	PMAD1B	PMAD1A
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMAD1A/B: Power Management of MIC-Amp 1 & ADC1 Ach/Bch (Table 29)
0: Power down (default)
1: Power up

PMAD2A/B: Power Management of MIC-Amp 2 & ADC2 Ach/Bch (Table 30)
0: Power down (default)
1: Power up

PMDM1A/B: Input Signal Select with Digital Microphone 1 (Table 31)
0: Power Down (default)
1: Power Up
ADC1 digital block is powered-down by PMDM1A = PMDM1B bits = “0” when selecting a digital microphone input (DMIC1 bit = “1”).

PMDM2A/B: Input Signal Select with Digital Microphone 2 (Table 32)
0: Power Down (default)
1: Power Up
ADC2 digital block is powered-down by PMDM2A = PMDM2B bits = “0” when selecting a digital microphone input (DMIC2 bit = “1”).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Power Management 3	AIRST[2:0]			PMVAD	PFSDO2	PFSDO1	PMPFIL2	PMPFIL1
R/W		R/W			R/W	R/W	R/W	R/W	R/W
Default		000			0	0	0	0	0

PMPFIL1: Power Management of Programmable Filter 1
0: Power down (default)
1: Power up

PMPFIL2: Power Management of Programmable Filter 2
0: Power down (default)
1: Power up @ PMPFIL1 bit = “1” (PMPFIL2 does not power up, when PMPFIL1 bit = “0”.)

PFSDO1/2: SDTO1/2 Output Signal Select
0: ADC output (default)
1: Programmable Filter or VAD output

PMVAD: Power Management of Voice Activity Detector (Table 53)
0: Power down (default)
1: Power up

AIRST[2:0]: AIN1/2 Initialization Cycle Setting (Table 27)
Default: “000” (656/fs)
This is a common setting for AIN1A/B and AIN2A/B.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	MIC Input & MIC Power Setting	MDIF2B	MDIF2A	MDIF1B	MDIF1A	AINCOM	MONON	MICL[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Default		0	0	0	0	0	0	00	

MICL1[1:0]: MIC Power (MPWR1/2 pins) Output Voltage Setting (Table 25)
Default: “00” (Typ. 2.8 V)

MONON: ADC Digital Output Mode Setting (Table 29, Table 30, Table 31, Table 32, Table 39)
0: Ach or Bch output (Default)
1: Ach and Bch output

AINCOM: COM Input Setting for Single-ended Input Mode
0: COM Separation (Default)
1: COM Contact (AIN1A-, AIN1B-, AIN2A-, AIN2B- pins)

MDIF1A/B: AIN1A/B Input Setting (Table 22)
0: Single-ended Input (AIN1A+ pin, AIN1B+ pin: Default)
1: Full-differential Input (AIN1A+/- pins, AIN1B+/- pins)

MDIF2A/B: AIN2A/B Input Setting (Table 23)
0: Single-ended Input (AIN2A+ pin, AIN2B+ pin: Default)
1: Full-differential Input (AIN2A+/- pins, AIN2B+/- pins)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	MIC Amplifier 1 Gain	MG1B[3:0]				MG1A[3:0]			
R/W		R/W				R/W			
Default		0110				0110			

MG1A/B[3:0]: MIC-Amp 1 Ach/Bch Analog Volume (Table 24)
Default: “0110” (+18 dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	MIC Amplifier 2 Gain	MG2B[3:0]				MG2A[3:0]			
R/W		R/W				R/W			
Default		0110				0110			

MG2A/B[3:0]: MIC-Amp 2 Ach/Bch Analog Volume (Table 24)
Default: “0110” (+18 dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Digital MIC Setting	0	DCLKP2	DCLKE2	DMIC2	0	DCLKP1	DCLKE1	DMIC1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DMIC1: Digital Microphone 1 Connection Select
0: Analog Microphone (default)
1: Digital Microphone (DMCLK1, DMDAT1 pins)

DCLKE1: DMCLK1 pin Output Clock Control
0: “L” Output (default)
1: 64fs Output

DCLKP1: DMDAT1 pin Data Latching Edge Select (Table 33)
0: Ach data is latched on the DMCLK1 rising edge (“↑”). (default)
1: Ach data is latched on the DMCLK1 falling edge (“↓”).

DMIC2: Digital Microphone 2 Connection Select
0: Analog Microphone (default)
1: Digital Microphone (DMCLK2, DMDAT2 pins)

DCLKE2: DMCLK2 pin Output Clock Control
0: “L” Output (default)
1: 64fs Output

DCLKP2: DMDAT2 pin Data Latching Edge Select
0: Ach data is latched on the DMCLK2 falling edge (“↑”). (default)
1: Ach data is latched on the DMCLK2 falling edge (“↓”).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Clock Mode Select	0	0	CM[1:0]		FS[3:0]			
R/W		R/W	R/W	R/W		R/W			
Default		0	0	00		1010			

FS[3:0]: Sampling Frequency Setting
(Table 4, Table 10, Table 11, Table 12, Table 13, Table 14, Table 15)
Default: “1010” (fs = 48kHz)

CM[1:0]: CODEC Master Clock Select
(Table 3, Table 5, Table 10, Table 11, Table 12, Table 13, Table 14, Table 15)
Default: “00” (256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	PLL CLK Source Select	0	0	BCKO	MCKOE	0	0	PLS	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PLS: PLL Clock Source Select (Table 7)
0: MCKI pin (default)
1: BCLK pin

MCKOE: Master Clock Output Enable (Table 5)
0: Disable (“L” output: Default)
1: Enable

BCKO: BCLK Output Frequency Select at Master Mode (Table 6, Table 14)
0: 32fs (default)
1: 64fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	PLL Ref CLK Divider 1	PLD[15:8]							
0BH	PLL Ref CLK Divider 2	PLD[7:0]							
R/W		R/W							
Default		00H							

PLD[15:0]: PLL Reference Clock Divider Setting (Table 8)
Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	PLL FB CLK Divider 1	PLM[15:8]							
0DH	PLL FB CLK Divider 2	PLM[7:0]							
R/W		R/W							
Default		00H							

PLM[15:0]: PLL Feedback Clock Divider Setting (Table 9)
Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Audio I/F Format	0	BCKP	DLC[1:0]		TDM[1:0]		DIF[1:0]	
R/W		R/W	R/W	R/W		R/W		R/W	
Default		0	0	00		00		00	

DIF[1:0]: Audio I/F Format Setting (Table 16, Table 17, Table 18, Table 19)
Default: “00” (I^2S compatible)

TDM[1:0]: TDM Mode Setting (Table 6, Table 16, Table 17, Table 18, Table 19)
Default: “00” (Stereo Mode)

DLC[1:0]: Data Length Setting (Table 21)
Default: “00” (24-bit Linear)

BCKP: BCLK Edge Setting (Table 20)
0: Falling (default)
1: Rising

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Phase Adjustment 1A	DLY1AE	0	DLY1A[5:0]					
10H	Phase Adjustment 1B	DLY1BE	0	DLY1B[5:0]					
11H	Phase Adjustment 2A	DLY2AE	0	DLY2A[5:0]					
12H	Phase Adjustment 2B	DLY2BE	0	DLY2B[5:0]					
R/W		R/W	R/W	R/W					
Default		0	0	000000					

DLYxA/B[5:0]: Programmable Phase Adjustment Setting (x=1, 2) (Table 34Table 21)
Default: “00H” (1/64fs)

DLYxA/BE: Programmable Phase Adjustment Enable (x=1, 2)
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	ADC high Pass Filter	0	ADRST[2:0]			HPF2C[1:0]		HPF1C[1:0]	
R/W		R/W	R/W			R/W		R/W	
Default		0	000			00		00	

HPF1/2C[1:0]: HPF1/2 Cut-off Frequency Setting (Table 35)
Default: “00” (3.7Hz @ fs = 48kHz)

ADRST[2:0]: ADC1/2 Initialization Cycle Setting (Table 28)
Default: “000” (1059/fs)
This is a common setting for ADC1 and ADC2.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	Digital Filter Select	ADVF	0	0	FSTHPFAD2N	FSTHPFAD1N	VREFH	HPFAD2N	HPFAD1N
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

HPFAD1N: HPF Control for ADC1
0: ON (default)
1: OFF
When HPFAD1N bit is "0", the settings of HPF1C[1:0] bits are enabled. When HPFAD1N bit is "1", the audio data passes the HPFAD1 block by 0dB gain.
When PMAD1A bit = "1" or PMAD1B bit = "1" (PMDM1A bit = "1" or PMDM1B bit = "1"), set HPFAD1N bit to "0".

HPFAD2N: HPF Control for ADC2
0: ON (default)
1: OFF
When HPFAD2N bit is "0", the settings of HPF2C[1:0] bits are enabled. When HPFAD2N bit is "1", the audio data passes the HPFAD2 block by 0dB gain.
When PMAD2A bit = "1" or PMAD2B bit = "1" (PMDM2A bit = "1" or PMDM2B bit = "1"), set HPFAD2N bit to "0".

VREFH: VREF Mode Setting
0: Normal Operation (default)
1: Provide the same power supply as AVDD to VREF pin
When the clock is stopped during normal operation, set VREFH bit to "1".

FSTHPFADxN: ADCx HPF Cut-off Frequency Setting during Initialization Cycle (x=1, 2) (Table 36)
0: The cut-off frequencies during initialization cycle will be high. (default)
1: The setting of HPFxC[1:0] bits are valid.

ADVF: ADC1/2 Digital Filter Mode Select (Table 37)
0: Short Delay Sharp Roll-Off Filter (default)
1: Voice Filter
This is a common setting for ADC1 and ADC2.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	MIC Sensitivity Adj.1A	MS1A[7:0]							
16H	MIC Sensitivity Adj.1B	MS1B[7:0]							
17H	MIC Sensitivity Adj.2A	MS2A[7:0]							
18H	MIC Sensitivity Adj.2B	MS2B[7:0]							
R/W		R/W							
Default		80H							

MSxA/B[7:0]: ADCx Ach/Bch Microphone Sensitivity Adjustment (x=1, 2) (Table 38)
Default: "80H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
19H	Filter 1 Select	PFTHR1	0	0	MIX1	LPF12	LPF11	HPF12	HPF11
1AH	Filter 2 Select	PFTHR2	0	0	MIX2	LPF22	LPF21	HPF22	HPF21
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

HPFx1/2: HPFx Control (x=1, 2)
0: Disable (default)
1: Enable
When HPFx1/2 bit is “1”, the settings of FHxA[15:0] and FHxB[15:0] bits are enabled. When HPFx1/2 bit is “0”, the audio data passes the HPFx1/2 block by is 0dB gain. (x=1, 2)

LPFx1/2: LPFx Control (x=1, 2)
0: Disable (default)
1: Enable
When LPFx1/2 bit is “1”, the settings of FLxA[15:0] and FlxB[15:0] bits are enabled. When LPFx1/2 bit is “0”, the audio data passes the LPFx1/2 block by is 0dB gain. (x=1, 2)

MIXx: ADCx Mixer Setting (x=1, 2) (Table 39)
0: Through (default)
1: Mix ((Ach + Bch)/2)

PFTHRx: HPFx, LPFx Through Select (x=1, 2)
0: HPFx, LPFx Path (default)
1: Through Path

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1BH	VAD Setting 1	VALPF2	VALPF1	VAHPF2	VAHPF1	HPF3RD	VADSEL	DLYE	VADOE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

VADOE: VADO Output Signal Select
0: ADC1 or Programmable Filter 1 output (default)
1: VADO output

DLYE: VAD Input Data Delay Setting (Table 55)
0: No Delay (default)
1: 2048 Samples (128ms @ fs=16kHz)

VADSEL: Input signal Select for VAD (Table 54)
0: ADC output (default)
1: HPF/LPF output

HPF3RD: HPF Setting for VALPF1
0: Use VALPF1 as LPF (default)
1: Use VALPF1 as HPF (3rd order HPF combined with VAHPF1/2)

VAHPF1/2: VAHPF1/2 Control
0: Disable (default)
1: Enable
When VAHPF1, VAHPF2 and HPF3RD bit = “1”, the settings of VFHA[15:0] and VFHB[15:0] bits are enabled. When VAHPF1 bit is “0” (VAHPF2 bit = “0”), the audio data passes the VAHPF1 (VAHPF2) block by is 0dB gain.

VALPF1/2: VALPF1/2 Control
0: Disable (default)
1: Enable
When VALPF1/2 bit is “1”, the settings of VAFLA[15:0] and VAFLB[15:0] bits are enabled. When VALPF1 bit is “0” (VALPF2 bit = “0”), the audio data passes the VALPF1 (VALPF2) block by is 0dB gain.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	VAD Setting 2	PT[7:0]							
R/W		R/W							
Default		07H							

PT[7:0]: Noise Level Detector Peak Value Setting (Table 56)
Default: 07H, Number of Sample = 8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	VAD Setting 3	VADINS[1:0]		NLLIM[1:0]		0	0	0	MINTH16
1EH	VAD Setting 4	MINTH[15:8]							
1FH	VAD Setting 5	MINTH[7:0]							
R/W		R/W							
Default		00001FH							

MINTH[16:0]: Minimum Noise Level Setting (Table 59)
Default: 0001FH, -72.2dB

NLLIM[1:0]: Rising Limit Select at NL Update (Table 58)
Default: 00, No limit

VADINS[1:0]: VAD Input Path Select (Table 54)
Default: 00 (AIN1A)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
20H	VAD Setting 6	AT[3:0]				NLDTH[11:8]			
21H	VAD Setting 7	NLDTH[7:0]							
R/W		R/W							
Default		7200H							

AT[3:0]: Noise Level Detector Average Value Setting (Table 57)
Default: “0111”, Number of Sample = 256

NLDTH[11:0]: Noise Level Threshold (Table 60)
Default: 200H, +12.0dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
22H	VAD Setting 8	ONGT[7:0]							
23H	VAD Setting 9	OFFGT[7:0]							
R/W		R/W							
Default		010FH							

ONGT[7:0]: On Guard Timer Setting (Table 61)
Default: 01H, 2 times

OFFGT[7:0]: Off Guard Timer Setting (Table 62)
Default: 0FH, 4096/fs (256ms)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
24H	VAD Setting 10	VONT	VBS[2:0]			0	VAS[2:0]		
R/W		R/W	R/W			R/W	R/W		
Default		0	000			0	000		

VAS[2:0], VBS[2:0]: Output Selector Setting (Table 63)
Default: “000”, VDLYO[15:0]

VONT: NL Non-updated Time Setting at VON Detection
Default: “0”, 4s@fs=16kHz
“1”, 2s@fs=16kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
25H	ALC Select	FRN	ATTLIM2	ATTLIM1	0	0	ALC4	ALC2	ALC1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ALCx: ALCx Enable (x=1, 2) (Table 41)
0: ALCx Disable (default)
1: ALCx Enable

ALC4: ALC 4ch Link Enable (Table 41)
0: ALC 4ch Link Disable (default)
1: ALC 4ch Link Enable

ATTLIMx: ALCx ATT Limiter Enable (x=1, 2)
0: ATT Limiter Disable (default)
1: ATT Limiter Enable
When ALC 4ch Link Mode is selected (ALC4 bit = “1”), it is controlled by ATTLIM1 bit and ATTLIM2 bit should be set to “0”.

FRN: Fast Recovery Disable
0: Fast Recovery Enable (default)
1: Fast Recovery Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
26H	ALC Control 1	IVTM[1:0]		0	ALCEQN	FRATT[1:0]		WTM[1:0]	
R/W		R/W		R/W	R/W	R/W		R/W	
Default		01		0	0	00		00	

WTM[1:0]: ALC Recovery Waiting Period (Table 44)
Default: 00 (128fs)

FRATT[1:0]: Fast Recovery Reference Volume Attenuation Step (Table 48)
Default: 00 (-0.00106dB: 4/fs)

ALCEQN: ALCEQ Disable
0: ALCEQ Enable (default)
1: ALCEQ Disable

IVTM[1:0]: Input Digital Volume Soft Transition Time Setting (Table 51)
Default: 01 (944/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
27H	Input Digital Volume 1A	IV1A[7:0]							
28H	Input Digital Volume 1B	IV1B[7:0]							
R/W		R/W							
Default		91H							

IVxA/B[7:0]: Digital Input Volume (x=1, 2) (Table 50)
Default: “91H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
29H	ALC1 Reference Level	REF1[7:0]							
R/W		R/W							
Default		E1H							

REF1[7:0]: Reference Value at ALC Recovery Operation (Table 46)
Default: “E1H” (+30dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2AH	ALC1 Control	IVOL1C	RGAIN1[2:0]			RFST1[1:0]		LMTH1[1:0]	
R/W		R/W	R/W			R/W		R/W	
Default		1	000			00		00	

LMTH1[1:0]: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 42)
Default: 00

RFST1[1:0]: ALC Fast Recovery Speed (Table 47)
Default: 00 (0.000265dB)

RGAIN1[2:0]: ALC Recovery Gain Step (Table 45)
Default: 000 (0.00212dB)

IVOL1C: Input Digital Volume Control Mode
0: Independent
1: Dependent (default)
When IVOL1C bit = "1", IV1A[7:0] bits control both Ach and Bch volume levels, while register values of IV1A[7:0] bits are not written to IV1B[7:0] bits.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2BH	Input Digital Volume 2A	IV2A[7:0]							
2CH	Input Digital Volume 2B	IV2B[7:0]							
R/W		R/W							
Default		91H							

IV2A/B[7:0]: Digital Input Volume (Table 50)
Default: "91H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2DH	ALC2 Reference Level	REF2[7:0]							
R/W		R/W							
Default		E1H							

REF2[7:0]: Reference Value at ALC Recovery Operation (Table 46)
Default: "E1H" (+30dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2EH	ALC2 Control	IVOL2C	RGAIN2[2:0]			RFST2[1:0]		LMTH2[1:0]	
R/W		R/W	R/W			R/W		R/W	
Default		1	000			00		00	

LMTH2[1:0]: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 42)
Default: 00

RFST2[1:0]: ALC Fast Recovery Speed (Table 47)
Default: 00 (0.000265dB)

RGAIN2[2:0]: ALC Recovery Gain Step (Table 45)
Default: 000 (0.00212dB)

IVOL2C: Input Digital Volume Control Mode
0: Independent
1: Dependent (default)
When IVOL2C bit = "1", IV2A[7:0] bits control both Ach and Bch volume levels, while register values of IV2A[7:0] bits are not written to IV2B[7:0] bits.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2FH	HPF1 Coefficient A	FH1A[15:8]							
30H	HPF1 Coefficient A	FH1A[7:0]							
31H	HPF1 Coefficient B	FH1B[15:8]							
32H	HPF1 Coefficient B	FH1B[7:0]							
R/W		R/W							
Default		FH1A[15:0] bits = 7EC1H, FH1B[15:0] bits = 827DH							

FH1A[15:0], FH1B[15:0]: HPF1 Coefficient
Default: FH1A[15:0] bits = 7EC1H, FH1B[15:0] bits = 827DH (fc=150Hz@fs=48kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
33H	LPF1 Coefficient A	FL1A[15:8]							
34H	LPF1 Coefficient A	FL1A[7:0]							
35H	LPF1 Coefficient B	FL1B[15:8]							
36H	LPF1 Coefficient B	FL1B[7:0]							
R/W		R/W							
Default		00H							

FL1A[15:0], FL1B[15:0]: LPF1 Coefficient
Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
37H	HPF2 Coefficient A	FH2A[15:8]							
38H	HPF2 Coefficient A	FH2A[7:0]							
39H	HPF2 Coefficient B	FH2B[15:8]							
3AH	HPF2 Coefficient B	FH2B[7:0]							
R/W		R/W							
Default		FH2A[15:0] bits = 7EC1H, FH2B[15:0] bits = 827DH							

FH2A[15:0], FH2B[15:0]: HPF2 Coefficient
Default: FH2A[15:0] bits = 7EC1H, FH2B[15:0] bits = 827DH (fc=150Hz@fs=48kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
3BH	LPF2 Coefficient A	FL2A[15:8]							
3CH	LPF2 Coefficient A	FL2A[7:0]							
3DH	LPF2 Coefficient B	FL2B[15:8]							
3EH	LPF2 Coefficient B	FL2B[7:0]							
R/W		R/W							
Default		00H							

FL2A[15:0], FL2B[15:0]: LPF2 Coefficient
Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
3FH	VAHPF Coefficient A	VFHA[15:8]							
40H	VAHPF Coefficient A	VFHA[7:0]							
41H	VAHPF Coefficient B	VFHB[15:8]							
42H	VAHPF Coefficient B	VFHB[7:0]							
R/W		R/W							
Default		VFHA[15:0] bits = 78DFH, VFHB[15:0] bits = 8E42H							

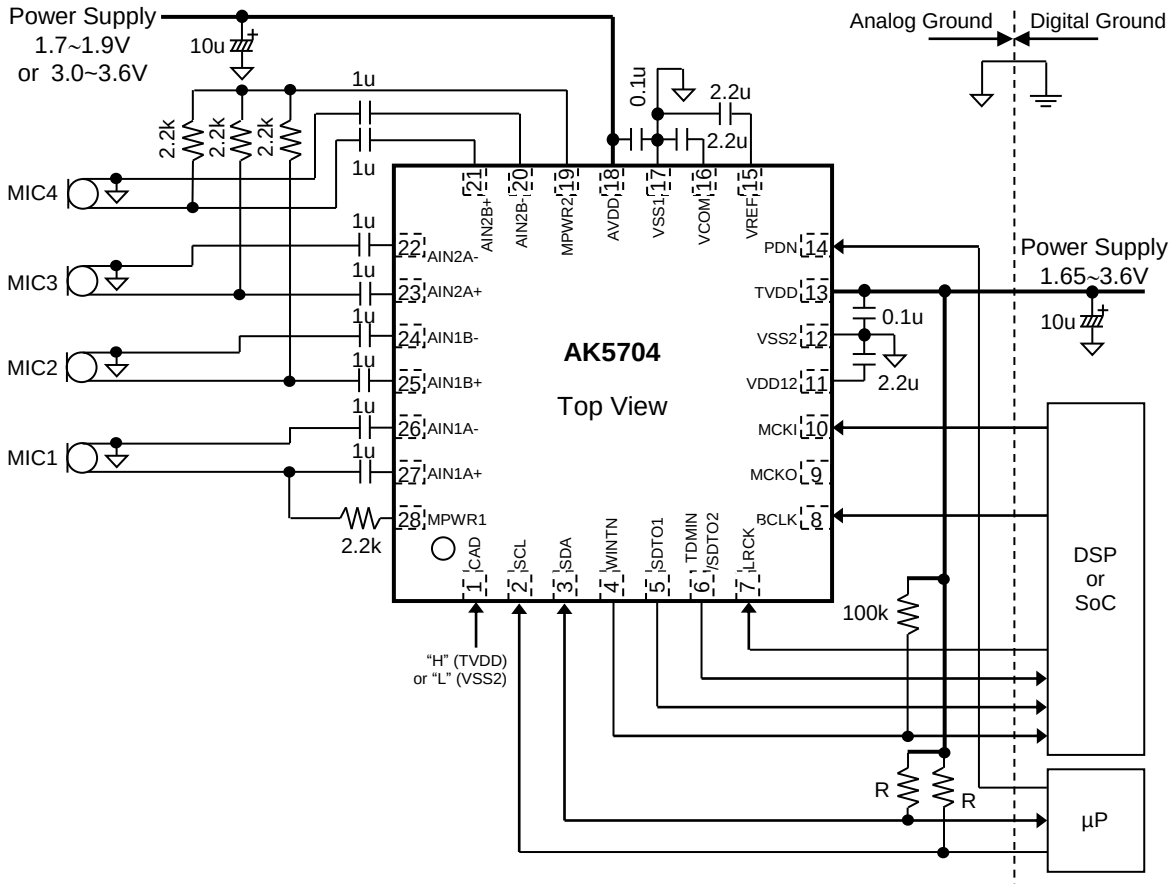
VFHA[15:0], VFHB[15:0]: VAHPF Coefficient
Default: VFHA[15:0] bits = 78DFH, VFHB[15:0] bits = 8E42H (fc=300Hz@fs=16kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
43H	VAPF Coefficient A	VFLA[15:8]							
44H	VAHF Coefficient A	VFLA[7:0]							
45H	VAPF Coefficient B	VFLB[15:8]							
46H	VAPF Coefficient B	VFLB[7:0]							
R/W		R/W							
Default		00H							

VFLA[15:0], VFLB[15:0]: VALPF Coefficient
Default: 0000H

10. Recommended External Circuits

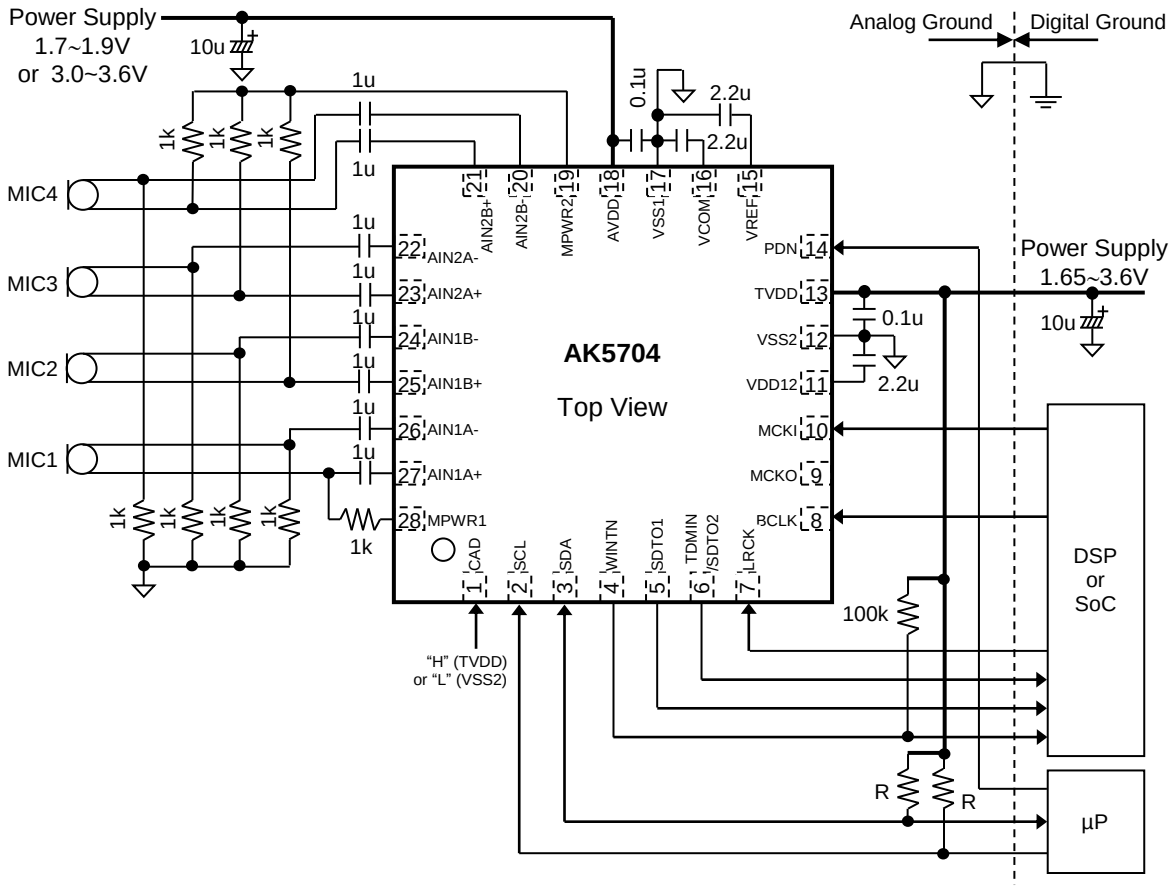
Figure 56 and Figure 57 show the system connection diagrams. An evaluation board (AKD5704) is available for fast evaluation as well as suggestions for peripheral circuitry.



Note:

- VSS1 and VSS2 of the AK5704 must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- Negative input pins must be connected to VSS1 with same value capacitor in series.
- SCL, SDA pins must be pulled-up by the resistor (R).
- If WINTN pin is used, WINTN pin is a Hi-Z state at power-down. WINTN pin should be pulled-up to TVDD by the resistor (about 100kΩ) externally to avoid the floating state.

Figure 56. System Connection Diagram (Single-ended Input, EXT Slave Mode)



Note:
- VSS1 and VSS2 of the AK5704 must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- SCL, SDA pins must be pulled-up by the resistor (R).
- If WINTN pin is used, WINTN pin is a Hi-Z state at power-down. WINTN pin should be pulled-up to TVDD by the resistor (about 100kΩ) externally to avoid the floating state.

Figure 57. System Connection Diagram (Full-differential Input, EXT Slave Mode)

1. Grounding and Power Supply Decoupling

The AK5704 requires careful attention to power supply and grounding arrangements. AVDD is usually supplied from the system's analog supply, and TVDD is supplied from the system's digital power supply. If AVDD and TVDD are supplied separately, the power-up sequence is not critical. The PDN pin should be held "L" when power supplies are tuning on. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

1) Power-up
- The PDN pin should be held "L" when power supplies are turning on. The AK5704 can be reset by keeping the PDN pin "L" for 1ms or longer after all power supplies are applied and settled. When the PDN pin = "H", LDO12 powers up and outputs a regulated voltage (typ. 1.2V) from the VDD12 pin. LDO12 is supplied to the digital core. The VDD12 pin must be connected to the VSS2 pin with a 2.2μF ±50% ceramic capacitor in series. No load current may be drawn from the VDD12 pin.

2) Power-down
- Each of power supplies can be powered OFF after the PDN pin is set to "L".

VSS1 and VSS2 of the AK5703 should be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close the power supply pins as possible. Especially, the small value ceramic capacitor is to be closest.

2. Reference Voltage

VREF is an analog reference voltage output from the VREF pin. This pin must be connected to the VSS1 pin with a 2.2μF ±50% ceramic capacitor in series. VCOM is a signal ground of this chip. A 2.2μF ±50% capacitor attached to the VSS1 pin eliminates the effects of high frequency noise. This capacitor should be placed as near as possible to the AK5704. No load current may be drawn from the VREF pin and the VCOM pin. All signals, especially clocks, should be kept away from the VREF pin and the VCOM pin in order to avoid unwanted coupling into the AK5704.

3. Analog Inputs

The analog inputs are single-ended or full-differential and input resistance is 200kΩ (typ). The input signal range scales with nominally 2.02 x AVDD/3.3 Vpp (typ) (@ MIC-Amp Gain = 0dB), centered around the internal signal ground (0.5 x AVDD). Usually the input signal is AC coupled with a capacitor. The cut-off frequency is $fc = 1/(2\pi RC)$. The ADC output data format is 2's complement. The DC offset including the ADC's own DC offset is removed by the internal HPF (fc=1.23Hz@ HPF1/2C[1:0] bits = "00", fs=16kHz). An AINx- pin must be connected to VSS1 via a capacitor with the same capacitance as the AINx+ pin when single-ended input.

11. Control Sequence

11.1. Clock Set Up

When the AK5704 is in operation, the clocks must be supplied.

11.1.1. PLL Master Mode

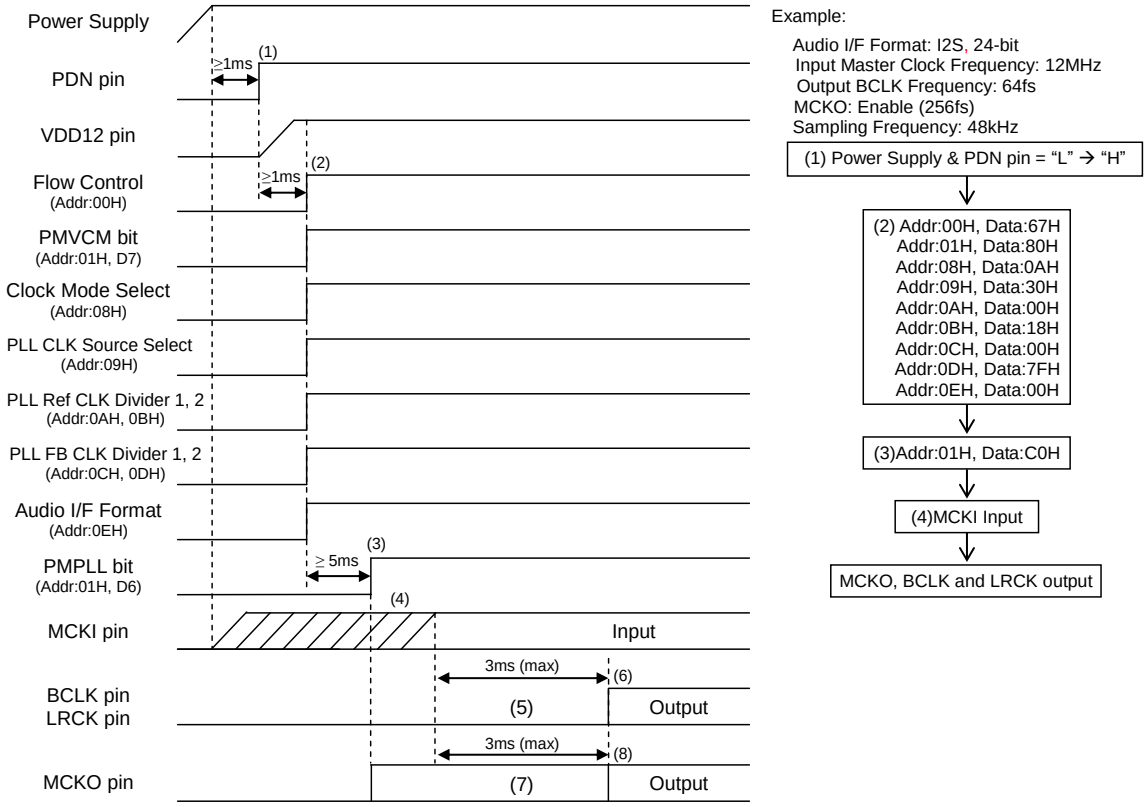


Figure 58. Clock Set Up Sequence (1)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 1ms or more is needed to reset the AK5704. After the PDN pin = "H", wait time of 1ms or more is needed to power up VDD12.

(2) Power Up VCOM and VREF: PMVCM bit = "0" → "1"
PSW0N, PSW1N, FS[3:0], CM[1:0], MSN, PLS, PLLMD, MCKOE, BCKO, PLD[15:0], PLM[15:0], DIF[1:0], TDM[1:0], DLC[1:0], BCKP and SDTO2E bits must be set during this period.
VCOM and VREF must first be powered-up before the other block operates. Power up time is 5.0ms (max) when the capacitance of an external capacitor for the VCOM and the VREF pin is 2.2μF ±50% each.
In case of using MCKO output: MCKOE bit = "1"
In case of not using MCKO output: MCKOE bit = "0"

(3) Power Up PLL: PMPLL bit = "0" → "1"

(4) PLL starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source, and PLL lock time is 3ms (max).

(5) BCLK pin and LRCK pin output "L" during this period.

(6) The AK5704 starts outputting BCLK and LRCK clocks after the PLL becomes stable. Then normal operation starts.

(7) The invalid frequency is output from the MCKO pin during this period if MCKO bit = "1".

(8) The normal clock is output from the MCKO pin after the PLL is locked if MCKO bit = "1".

11.1.2. PLL Slave Mode (BCLK pin)

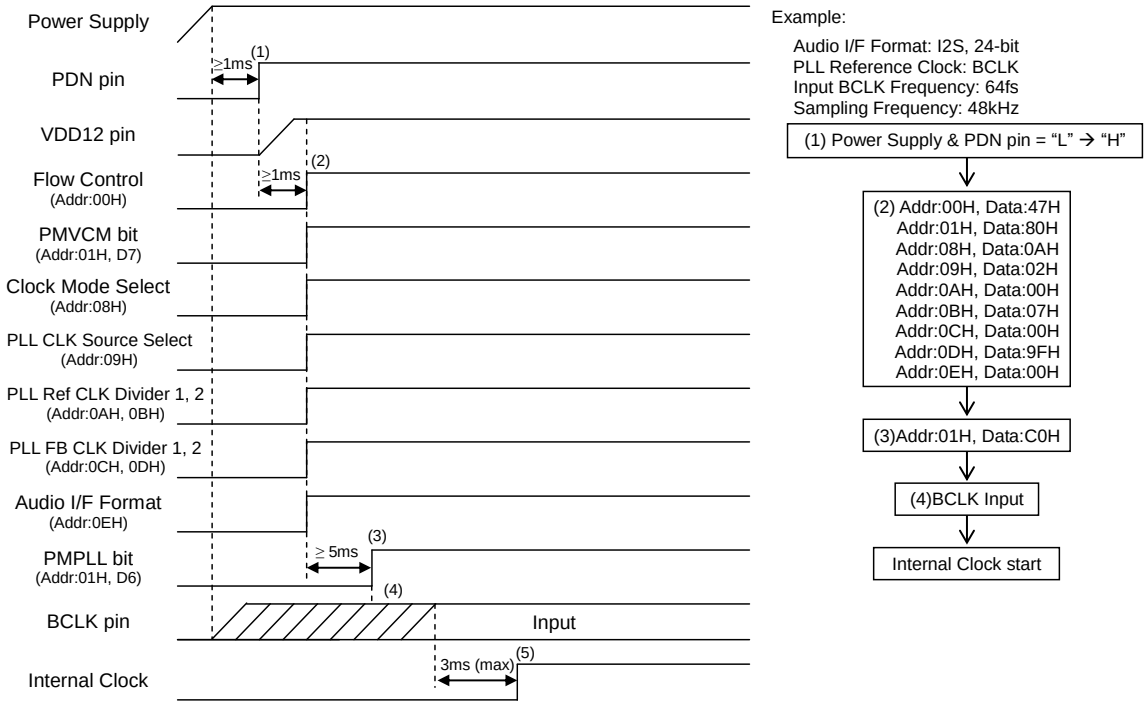


Figure 59. Clock Set Up Sequence (2)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 1ms or more is needed to reset the AK5704. After the PDN pin = "H", wait time of 1ms or more is needed to power up VDD12.

(2) Power Up VCOM and VREF: PMVCM bit = "0" → "1"
PSW0N, PSW1N, FS[3:0], CM[1:0], MSN, PLS, PLLMD, PLD[15:0], PLM[15:0], DIF[1:0], TDM[1:0], DLC[1:0], BCKP and SDTO2E bits must be set during this period.
VCOM and VREF must first be powered-up before the other block operates. Power up time is 5.0ms (max) when the capacitance of an external capacitor for the VCOM and the VREF pin is 2.2μF ±50% each.

(3) Power Up PLL: PMPLL bit = "0" → "1"

(4) PLL starts after PMPLL bit changes from "0" to "1" and PLL reference clock is supplied from BCLK pin. The time until PLL is locked and the clock is supplied to internal circuits is 3ms (max).

(5) The AK5704 starts normal operation after the PLL became stable and the internal clock is generated.

11.1.3. PLL Slave Mode (MCKI pin)

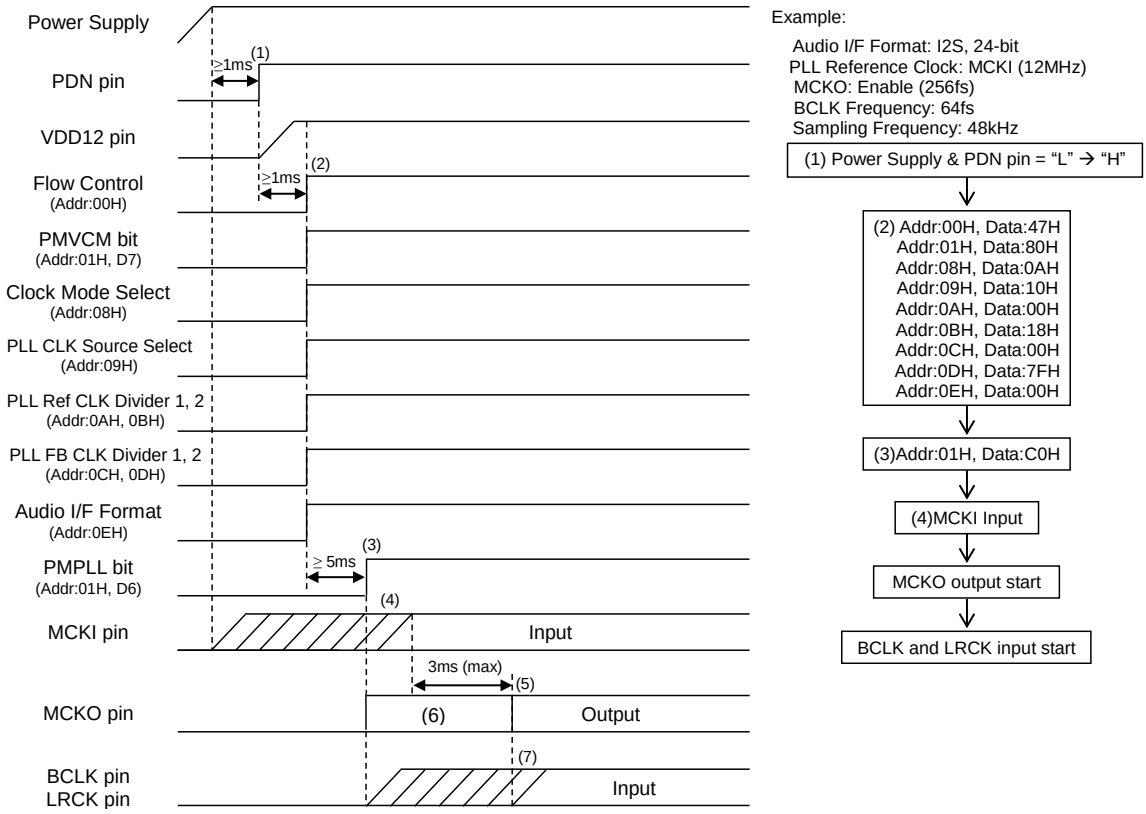


Figure 60. Clock Set Up Sequence (3)

<Sequence>

(1) After power Up: PDN pin "L" → "H"
"L" time of 1ms or more is needed to reset the AK5704. After the PDN pin = "H", wait time of 1ms or more is needed to power up VDD12.

(2) Power Up VCOM and VREF: PMVCM bit = "0" → "1"
PSW0N, PSW1N, FS[3:0], CM[1:0], MSN, PLS, PLLMD, MCKOE, PLD[15:0], PLM[15:0], DIF[1:0], TDM[1:0], DLC[1:0], BCKP and SDTO2E bits must be set during this period.
VCOM and VREF must first be powered-up before the other block operates. Power up time is 5.0ms (max) when the capacitance of an external capacitor for the VCOM and the VREF pin is 2.2μF ±50% each.

(3) Power Up PLL: PMPLL bit = "0" → "1"

(4) PLL starts after PMPLL bit changes from "0" to "1" and PLL reference clock is supplied from MCKI pin. The time until PLL is locked and starts normal output is 3ms (max).

(5) The normal clock is output from the MCKO pin after the PLL became stable.

(6) The invalid frequency is output from the MCKO pin during this period.

(7) BCLK and LRCK clocks must be synchronized with MCKO clock.

11.1.4. External Slave Mode

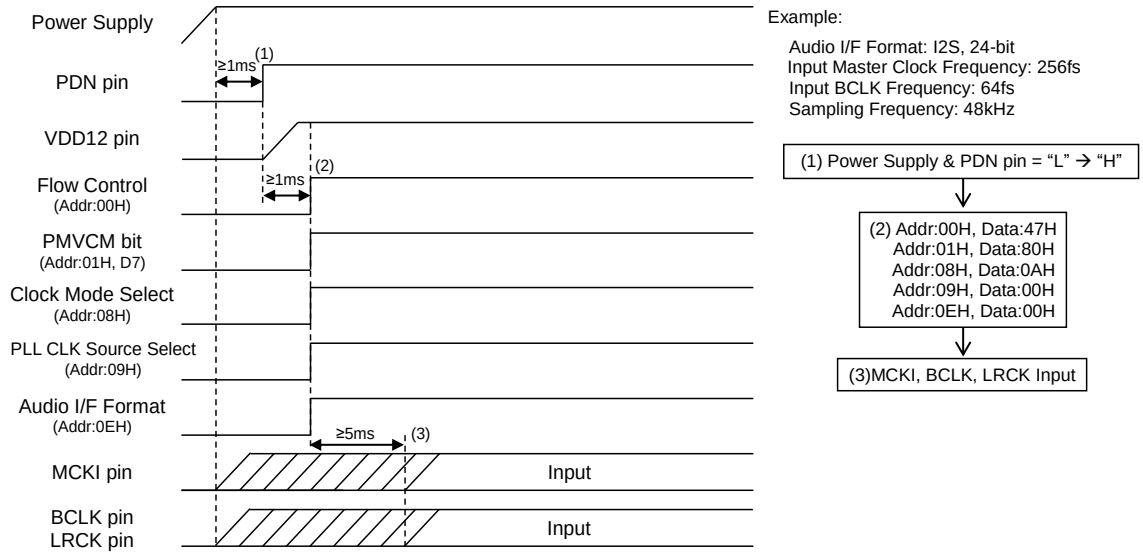


Figure 61. Clock Set Up Sequence (4)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 1ms or more is needed to reset the AK5704. After the PDN pin = "H", wait time of 1ms or more is needed to power up VDD12.

(2) Power Up VCOM and VREF: PMVCM bit = "0" → "1"
PSW0N, PSW1N, FS[3:0], CM[1:0], MSN, DIF[1:0], TDM[1:0], DLC[1:0], BCKP and SDTO2E bits must be set during this period.
VCOM and VREF must first be powered-up before the other block operates. Power up time is 5.0ms (max) when the capacitance of an external capacitor for the VCOM and the VREF pin is 2.2μF ±50% each.

(3) Normal operation starts after the MCKI, BCLK and LRCK are supplied.

11.1.5. External Master Mode

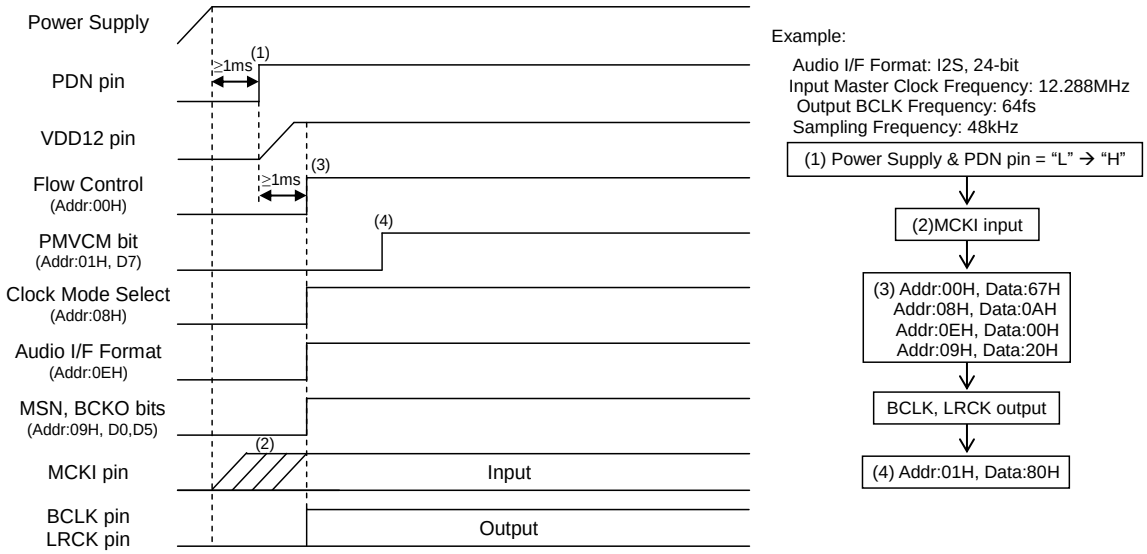


Figure 62. Clock Set Up Sequence (5)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 1ms or more is needed to reset the AK5704. After the PDN pin = "H", wait time of 1ms or more is needed to power up VDD12.

(2) MCKI is supplied.

(3) After SW0N, PSW1N, FS[3:0], CM[1:0], DIF[1:0], TDM[1:0], DLC[1:0], BCKP and SDTO2E bits are set, MSN and BCKO bits should be set to "1".
Then BCLK and LRCK are output.

(4) Power Up VCOM and VREF: PMVCM bit = "0" → "1"
VCOM and VREF must first be powered-up before the other block operates. Power up time is 5.0ms (max) when the capacitance of an external capacitor for the VCOM and the VREF pin is 2.2μF ±50% each.

11.2. Voice Activity Detection (1ch Mic)

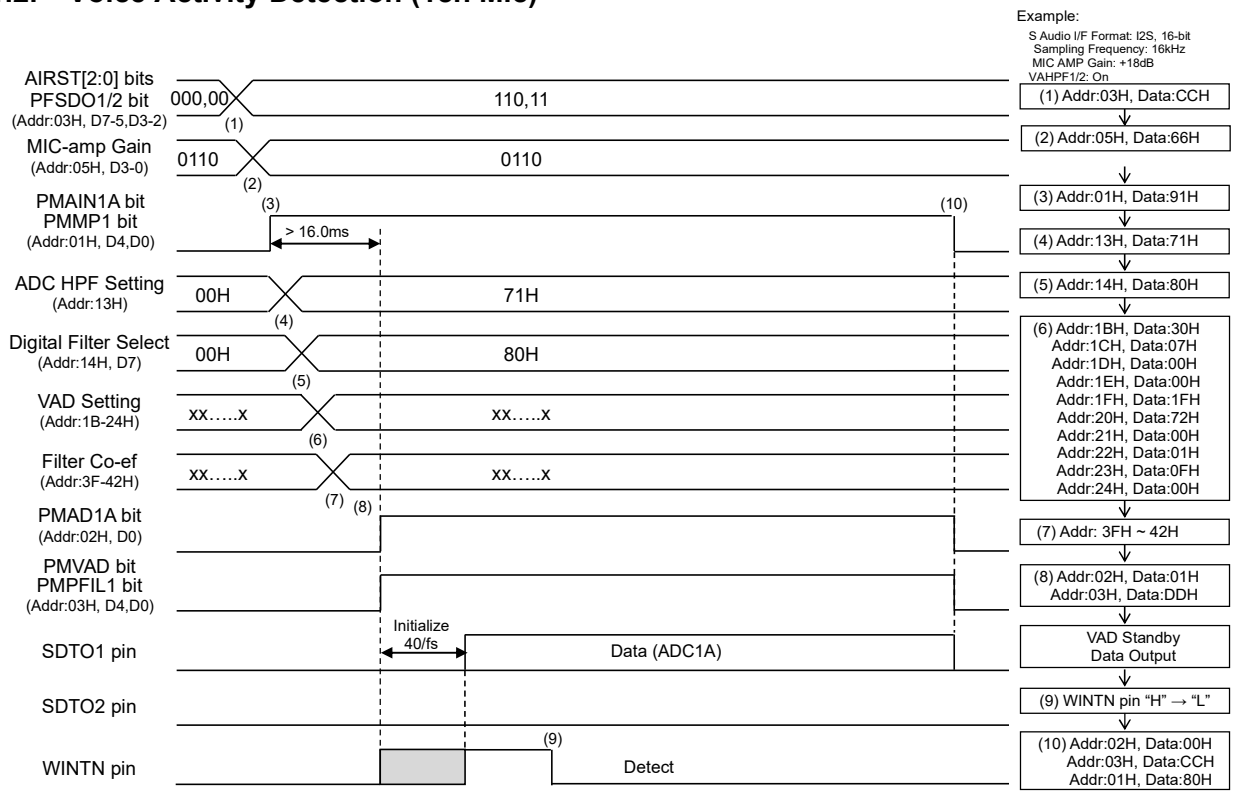


Figure 63. Voice Activity Detection (1ch Mic) Sequence

<Sequence>

This sequence is an example of VAD setting at fs=16kHz. At first, clocks should be supplied according to “Clock Set Up” sequence.

(1) Set Up AIN Initialization Cycle and Signal Path: AIRST[2:0] bits = “110” (256/fs), PFSDO1/2 bits = “1”
(2) Set Up Microphone Amp Gain: MG1A[3:0] bits = “0110” (+18dB)
(3) Power Up Microphone Power 1 and Microphone Amp 1A: PMAIN1A = PMMP1 bits = “1”
The initialization cycle time of AIN1A is 256/fs=16ms @ fs=16kHz.
(4) Set Up ADC1 Initialization Cycle: ADRST[2:0] bits = “111” (32/fs)
Set Up HPF1 Cut-off Frequency: HPF1C[1:0] bits = “01” (fc = 4.9Hz)
(5) Set Up ADC Digital Filter: ADVF bit = “1” (Voice Filter)
(6) Set Up VAD:
VAHPF1 = VAHPF2 bits = “1”, PT[7:0] bits = 07H, MINTH[16:0] bits = 0001FH, AT[3:0] bits = “0111”, NLDTH[11:0] bits = 200H, ONGT[7:0] bits = 01H, OFFGT[7:0] bits = 0FH, VAS[2:0] = VBS[2:0] bits = “000”
(7) Set Up Coefficient of VAHPF1/2 (Addr: 3FH ~ 42H)
(8) Power Up ADC1, VAD and Programmable Filter 1:
PMAD1A = PMVAD = PMPFIL1 bits = “0” → “1”
The initialization cycle time of ADC is 32/fs=2ms @ fs=16kHz.
(9) Voice Activity Detection: WINTN pin = “H” → “L”
When the voice activity is detected, the WINTN pin changes from “H” to “L”. The “L” period is 256/fs=16ms @fs = 16kHz(min.).
(10) Power Down ADC1, VAD and Programmable Filter 1:
PMAD1A = PMVAD = PMPFIL1 bits = “1” → “0”
Power Down Microphone Power 1 and Microphone 1A: PMAIN1A = PMMP1 bits = “1” → “0”

11.3. Voice Activity Detection (4ch Mic)

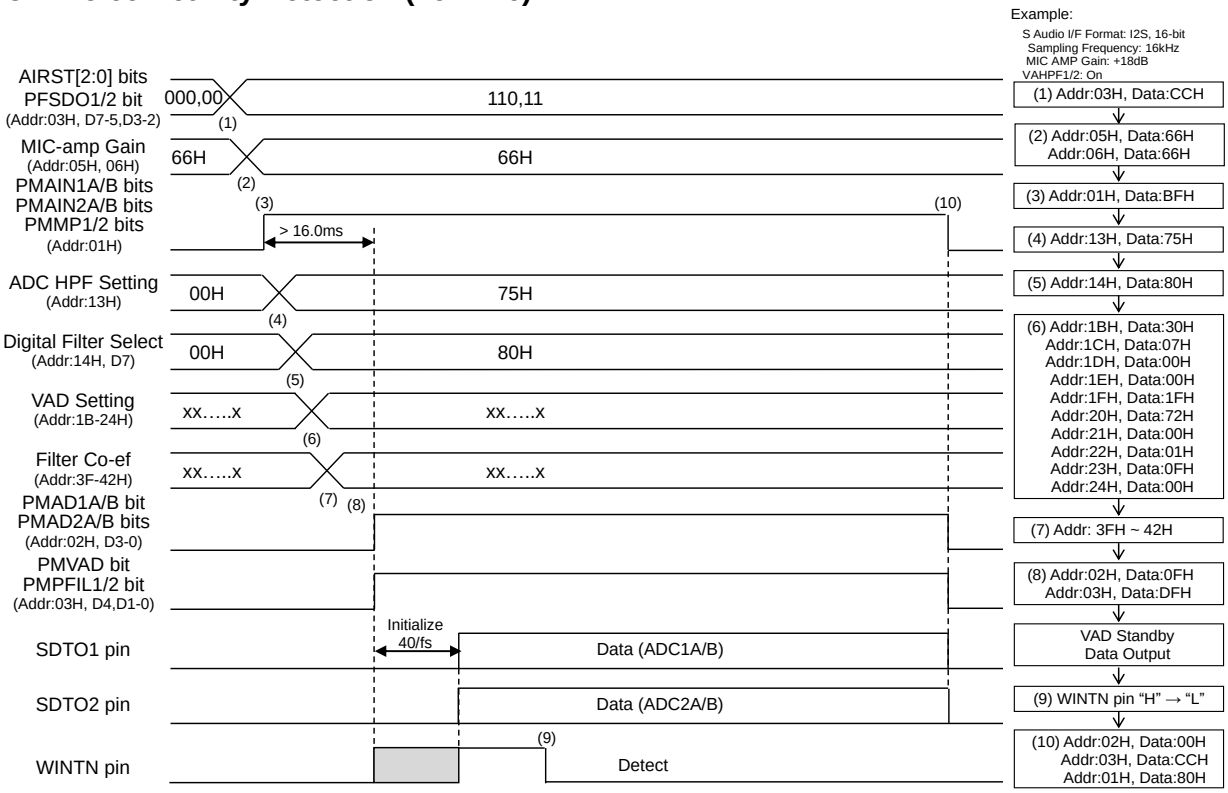


Figure 64. Voice Activity Detection (4ch Mic) Sequence

<Sequence>

This sequence is an example of VAD setting at fs=16kHz. At first, clocks should be supplied according to “Clock Set Up” sequence.

(1) Set Up AIN Initialization Cycle and Signal Path: AIRST[2:0] bits = “110” (256/fs), PFSDO1/2 bits = “1”
(2) Set Up Microphone Amp Gain (Addr = 05H, 06H)
(3) Power Up Microphone Power 1/2, Microphone Amp 1A/B and Microphone Amp 2A/B: PMAIN1A/B = PMAIN2A/B = PMMP1/2 bits = “1”
The initialization cycle time of AIN1/2 is 256/fs=16ms @ fs=16kHz.
(4) Set Up ADC1/2 Initialization Cycle: ADRST[2:0] bits = “111” (32/fs)
Set Up HPF1/2 Cut-off Frequency: HPF1/2C[1:0] bits = “01” (fc = 4.9Hz)
(5) Set Up ADC Digital Filter: ADVF bit = “1” (Voice Filter)
(6) Set Up VAD:
VAHPF1 = VAHPF2 bits = “1”, PT[7:0] bits = 07H, MINTH[16:0] bits = 0001FH, AT[3:0] bits = “0111”, NLDTH[11:0] bits = 200H, ONGT[7:0] bits = 01H, OFFGT[7:0] bits = 0FH, VAS[2:0] = VBS[2:0] bits = “000”
(7) Set Up Coefficient of VAHPF1/2 (Addr: 3FH ~ 42H)
(8) Power Up ADC1/2, VAD and Programmable Filter 1/2:
PMAD1A/B = PMAD2A/B = PMVAD = PMPFIL1/2 bits = “0” → “1”
The initialization cycle time of ADC is 32/fs=2ms @ fs=16kHz.
(9) Voice Activity Detection: WINTN pin = “H” → “L”
When the voice activity is detected, the WINTN pin changes from “H” to “L”. The “L” period is 256/fs=16ms @fs = 16kHz(min.).
(10) Power Down ADC1/2, VAD and Programmable Filter 1/2:
PMAD1A/B = PMAD2A/B = PMVAD = PMPFIL1/2 bits = “1” → “0”
Power Down Microphone Power 1/2, Microphone 1A/B and Microphone Amp 2A/B:
PMAIN1A/B = PMAIN2A/B = PMMP1/2 bits = “1” → “0”

11.4. Microphone Input Recording (4ch)

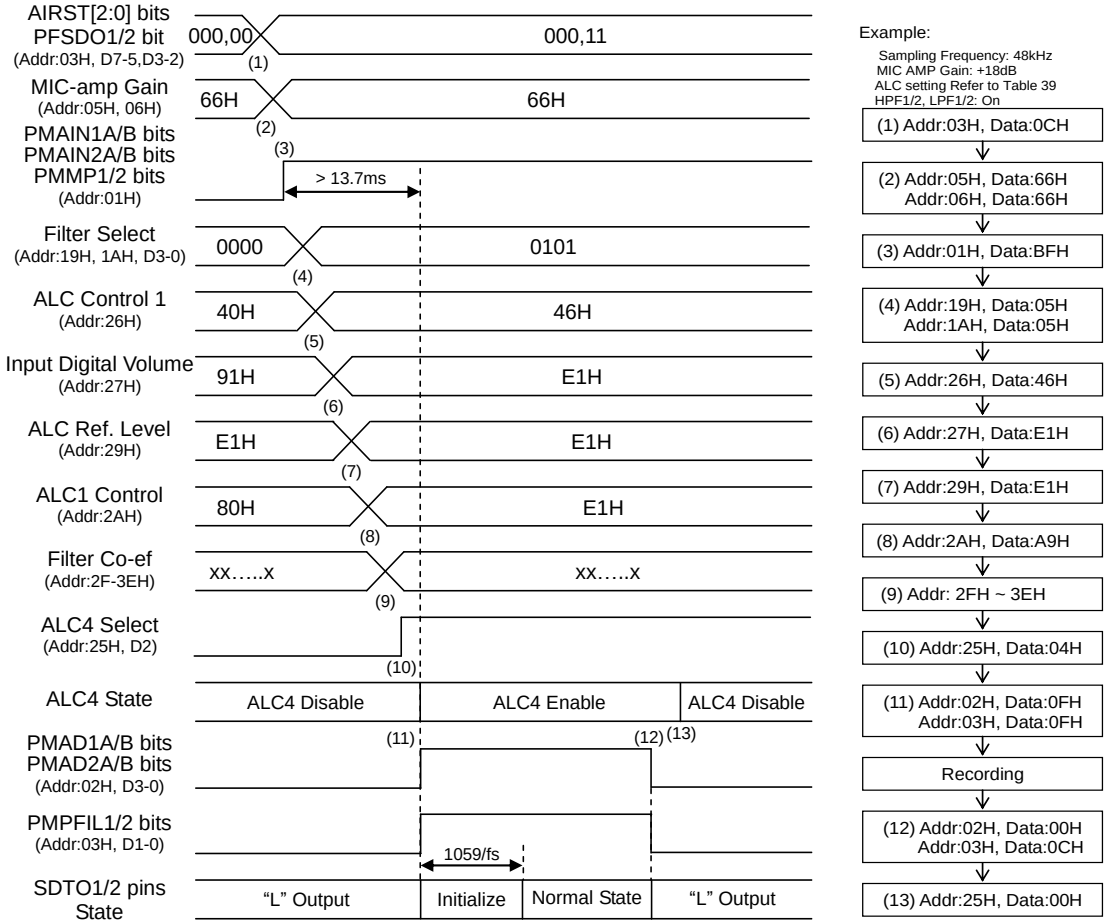


Figure 65. MIC Input Recording Sequence

<Sequence>

This sequence is an example of ALC setting at fs=48kHz. For changing the parameter of ALC, please refer to “Example of ALC Setting”. At first, clocks should be supplied according to “Clock Set Up”.

(1) Set Up AIN Initialization Cycle and Signal Path: AIRST[2:0] bits = “000” (656/fs), PFSDO1/2 bits = “1”
(2) Set Up Microphone Amp Gain (Addr = 05H, 06H)
(3) Power Up Microphone Power 1/2, Microphone Amp 1A/B and Microphone Amp 2A/B: PMAIN1A/B = PMAIN2A/B = PMMP1/2 bits = “1”
The initialization cycle time of AIN2A/B is 656/fs=13.7ms @ fs=48kHz.
(4) HPF1/2 and LPF1/2 ON/OFF Setting (Addr = 19H, 1AH)
(5) Set Up WTM[1:0], FRATT1[1:0] and ALCEQN bits (Addr = 26H)
(6) Set Up IVOL Value at ALC Operation start: IV1A[7:0] bits (Addr = 27H)
(7) Set Up REF Value: REF1[7:0] bits (Addtr = 29H)
(8) Set Up LMTH1[1:0], RFST1[1:0] and RGAIN1[2:0] bits (Addr = 29H)
(9) Set Up Coefficient of HPF1/2 and LPF1/2 (Addr: 2FH ~ 3EH)
(10) Set Up ALC4 and ATTLMT1 bits (Addr = 25H)
(11) Power Up ADC1/2: PMAD1A/B = PMAD2A/B bits = “0” → “1”
Power Up Programmable Filter 1/2: PMPFIL2 = PMPFIL2 bits = “0” → “1”
The initialization cycle time of ADC is 1059/fs=22.1ms @ fs=48kHz. ADC outputs “0” data during the initialization cycle. The ALC operation starts from IVOL value of (6).
(12) Power Down ADC1/2: PMAD1A/B = PMAD2A/B bits = “1” → “0”
Power Down Programmable Filter 1/2: PMPFIL2 = PMPFIL2 bits = “1” → “0”
(13) ALC4 Disable: ALC4 bit = “1” → “0”

11.5. Stop of Clock

11.5.1. PLL Master Mode

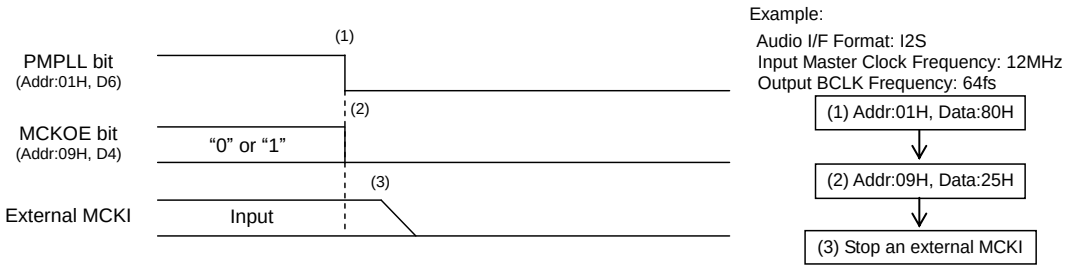


Figure 66. Clock Stopping Sequence (1)

<Sequence>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO output: MCKOE bit = "1" → "0"
(3) Stop an external master clock.

11.5.2. PLL Slave Mode (BCLK pin)

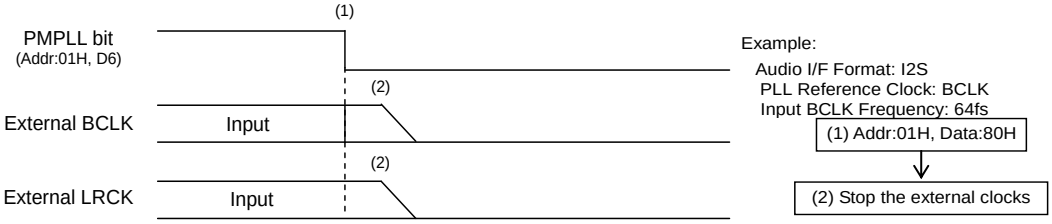


Figure 67. Clock Stopping Sequence (2)

<Sequence>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BCLK and LRCK clocks.

11.5.3. PLL Slave Mode (MCKI pin)

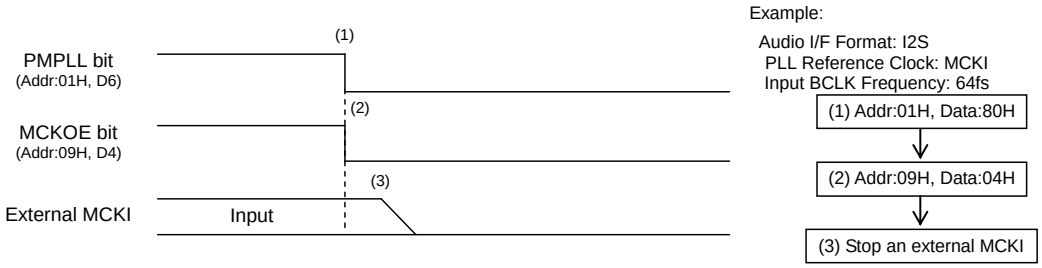


Figure 68. Clock Stopping Sequence (3)

<Sequence>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO output: MCKOE bit = "1" → "0"
(3) Stop an external master clock.

11.5.4. External Slave Mode

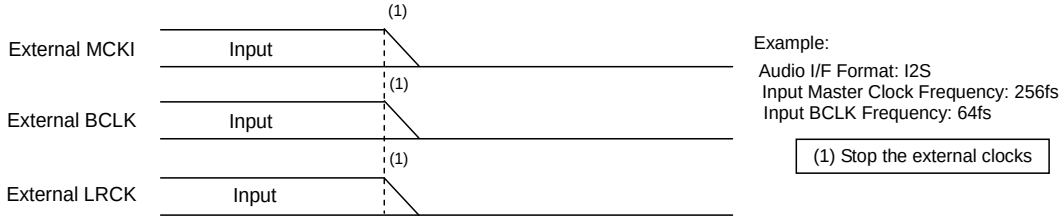


Figure 69. Clock Stopping Sequence (4)

<Sequence>
(1) Stop the external MCKI, BCLK and LRCK clocks.

11.5.5. External Master Mode

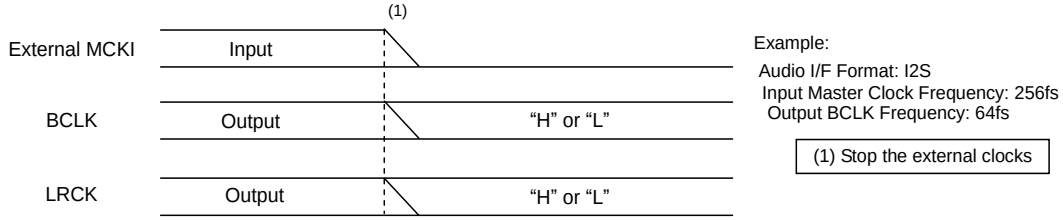


Figure 70. Clock Stopping Sequence (5)

<Sequence>
(1) Stop an external master clock. BCLK and LRCK are fixed to "H" or "L".

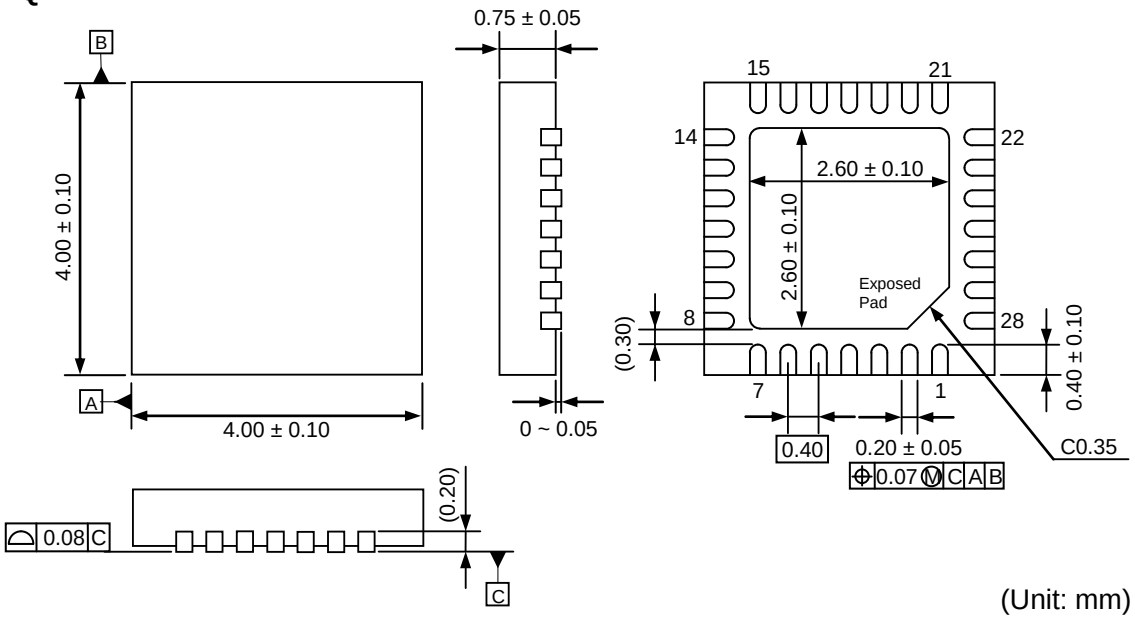
11.6. Power Down

Power supply current cannot be shut down by stopping clocks and setting PMVCM bit = "0". Power supply current can be shut down (typ. 4μA) by stopping clocks and setting the PDN pin = "L". When the PDN pin = "L", all registers are initialized.

12. Package

12.1. Outline Dimensions

28-pin QFN



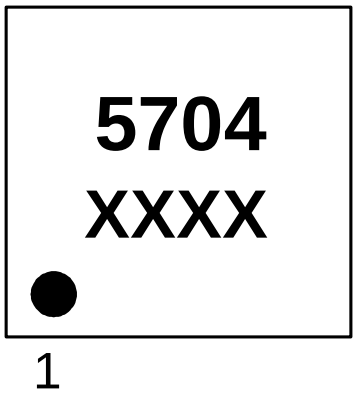
(Unit: mm)

* The exposed pad on the bottom surface of the package should be connected to the ground.

12.2. Material & Lead finish

Package molding compound: Epoxy Resin, Halogen (Br and Cl) free
Lead frame material: Cu Alloy
Pin surface treatment: Solder (Pb free) plate

12.3. Marking



XXXX: Date code (4 digits)
Pin #1 indication

13. Ordering Guide

AK5704EN −40 ~ +85°C 28-pin QFN (0.4mm pitch)
AKD5704 AK5704 Evaluation Board

14. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
19/02/20	00	First Edition		
22/01/31	01	Error Correction	102	Control Sequence Voice Activity Detection (1ch Mic) sequence and figure were changed.
		Description Addition	103	Control Sequence Voice Activity Detection (4ch Mic) sequence was added.

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