

## CHANGE NOTIFICATION



Linear Technology Corporation  
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February 06, 2017

Dear Sir/Madam:

PCN#020617

### **Subject: Notification of Change to LTC4015 Die and Datasheet**

Please be advised that Linear Technology Corporation has made a change to the LTC4015 die to correct errata that was previously reported as shown on the following page. The internal timing conflict that could cause a watchdog timeout has been corrected with logic routing. Also, an optional Packet Error Checking (PEC) feature has been enabled by logic routing changes. No other functional or parametric specifications are affected. The datasheet will be modified to explain the optional PEC feature.

This die change has been qualified by performing extensive engineering evaluation and test characterization over the full operating junction temperature range. In addition, the revised product will have successfully completed 1000 hours of High Temperature Operating Life (HTOL) prior to production release.

Linear Technology will accept requests for revised samples within 30 days of the date of this notification. If we do not hear back from your company within this 30 day period, we will consider of this Change Notice accepted by April 06, 2017.

Should you have any questions or concerns please contact your local Linear Technology Sales person or you may contact me at 408-432-1900 ext. 2077, or by e-mail at [JASON.HU@LINEAR.COM](mailto:JASON.HU@LINEAR.COM).

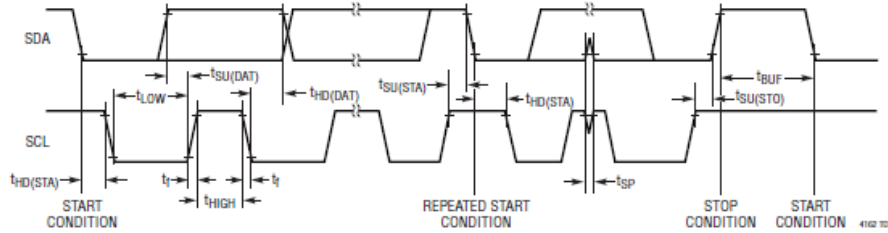
Sincerely,

Jason Hu  
Quality Assurance Engineer

New I2C timing diagram,  
Added PEC functionality(use is optional).



For Improved clarity  
Added: Legend, Read/Write protocol w&w/o PEC,  
SMBus Alert Response Protocol w&w/o PEC  
Corrected Repeated Start condition S=> Sr

## I<sup>2</sup>C TIMING DIAGRAM



### I<sup>2</sup>C SMBus Legend

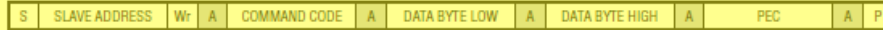
S START CONDITION  
Sr REPEATED START CONDITION  
Rd READ (BIT VALUE OF 1)  
Wr WRITE (BIT VALUE OF 0)  
A ACKNOWLEDGE  
N NACK  
P STOP CONDITION

PEC: PACKET ERROR CODE\*  
 MASTER TO SLAVE  
 SLAVE TO MASTER

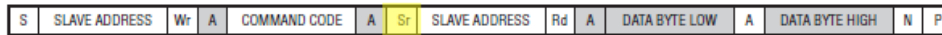
### SMBus WRITE WORD PROTOCOL



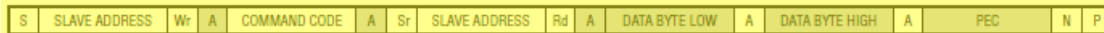
### SMBus WRITE WORD WITH PEC PROTOCOL\*



### SMBus READ WORD PROTOCOL



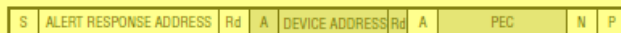
### SMBus READ WORD WITH PEC PROTOCOL\*



### SMBus ALERT RESPONSE ADDRESS PROTOCOL



### SMBus ALERT RESPONSE ADDRESS PROTOCOL WITH PEC\*



\* Use of PEC (PACKET ERROR CODE) PROTOCOL is optional



**LTC4015 ERRATA**

The errata below describes conditions that may cause an LTC<sup>®</sup>4015 to operate differently than expected or described in the data sheet.

**ERRATA SUMMARY**

ERRATA NUMBER	DESCRIPTION	PAGE
1	Device Resets, Losing Settings and Data	1

**ERRATA #1: DEVICE MAY RESET**

The device may reset itself resulting in loss of data and configuration settings. This can only occur in one specific use case detailed below. All other operating states are immune to this issue.

**Conditions:**

All of the following conditions must be present at the same time to expose this problem:

1. Battery Only Operation:  $V_{IN} < V_{BAT}$ ;  
 AND
2. Telemetry is not on. (Default setting in battery only – non-charging, force\_meas\_sys\_on = 0, sub-address 0x14, bit 4);  
 AND
3. I<sup>2</sup>C communications with idle time longer than 20ms;  
 AND
4. I<sup>2</sup>C port programmed (e.g., charger settings or alerts have been configured or coulomb counter has been enabled). If the I<sup>2</sup>C port is not programmed, this error has no impact.

Even with the above conditions, the issue only presents infrequently. All other use cases are immune to the issue.

**Impact:**

The device can reset itself, returning all registers to factory defaults. If this type of self-reset occurs, it will be indicated by the single bit flag at register 0x39, bit 12.

**Root Cause:**

An internal timing conflict exposed after watchdog timeout.

**Workarounds:**

Two workarounds are possible. These workarounds will wake the logic system before the watchdog can time out.

1. Use continuous I<sup>2</sup>C polling and ensure a polling rate greater than 50Hz.
2. Force the telemetry system on using the force\_meas\_sys\_on bit at register 0x14, bit 4. This will result in increased battery-only mode quiescent current by 2mA – 3mA.

**DEVICE FIX PLANNED:**

The internal timing conflict will be corrected. A PCN will be issued as soon as revised devices are available to sample, which is expected within Q1, CY 2017.

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