Keywords: 3V DACs, level shifting, +/-10V, 10V, 3V output, industrial DAC, bipolar, resistor networks, gain setting resistor, amplifier, op amp, digital pot

REFERENCE DESIGN 2398 INCLUDES: √Tested Circuit √Schematic √Description √Test Data

3V DACs Used in ±10V Applications

Sep 29, 2003

Abstract: Many modern systems have the majority of their electronics powered by 3.3V or lower, but must drive external loads with ±10V, a range that is still very common in industrial applications. There are digital to analog converters (DACs) available that can drive loads with ±10V swings, but there are reasons to use a 3.3V DAC and amplify the output voltage up to ±10V.

Introduction

Modern logic systems that use 3.3V supplies must sometimes run industrial applications which require voltages of ±10V, such as PLC, transmitters, and motor control. One solution is to choose a digital to analog converter (DAC) that can deliver ±10V swings, but an alternative is to use a 3.3V DAC and amplify the output voltage up to ±10V. Examples:

- 3.3V DACs may have higher levels of desired logic integration than their ±10V counterparts.
- 3.3V DACs tend to have higher speed logic interfaces, freeing the microcontroller for other tasks.
- The DAC may be integrated into a larger chip, powered from 3.3V (such as a microcontroller) and not capable of ±10V output swings.
- The external loads may have output current drive requirements or capacitive loads that cannot be handled by the 3.3V ±10V DAC.

Circuit Overview

The circuit's block diagram is shown in **Figure 1a**. It consists of five main blocks: DAC, Reference, Offset Adjust, Reference Buffer, and Output Buffer.

The DAC provides the digital-code-to-voltage translation, relative to the Reference. Offset Adjust provides the ability to offset the DAC's unipolar transfer function to create a bipolar output and the ability to calibrate the 0V output point. The Reference Buffer provides load isolation for the Reference and the Offset Adjust. The Output Buffer sums in the offset adjustments and provides the required gain to increase the output swing to the desired magnitude. Additionally the Output Buffer provides the ability to drive a load.

Circuit Description

The circuit in **Figure 1** and Figure 1a illustrates how a 3.3V powered 16-bit DAC can be buffered to achieve output swings of ±10V. The DAC (U2) has a 0 to 2.5V output range and is connected to the non-inverting input of op amp U3. This input has a non-inverting gain of (1 + 26.25k / 3.75k) or 8. The inverting input of the op amp is connected to +1.429V created by the reference and the resistor divider network.

This input has a gain of -(26.25k / 3.75k) or -7. The output of this circuit with the DAC programmed to minus full scale (0V) is = (0 x 8) - (7 x 1.429) = -10V. With the DAC programmed to full scale (2.5V), the final output is = (2.5 x 8) - (7 x 1.429) = +10V.

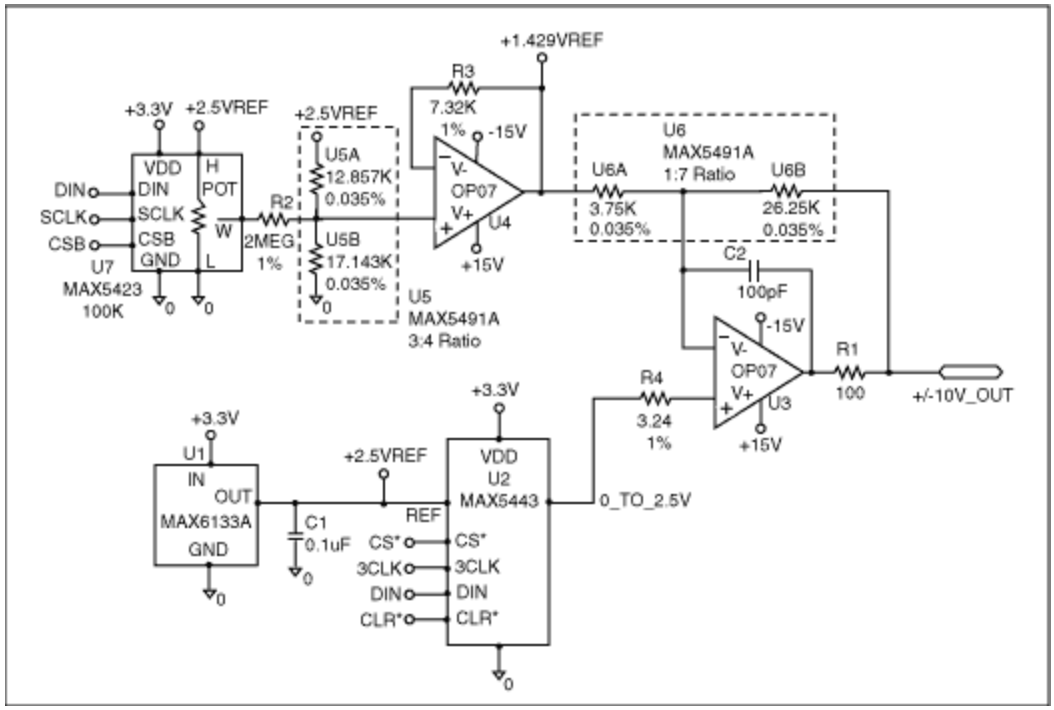

Figure 1.

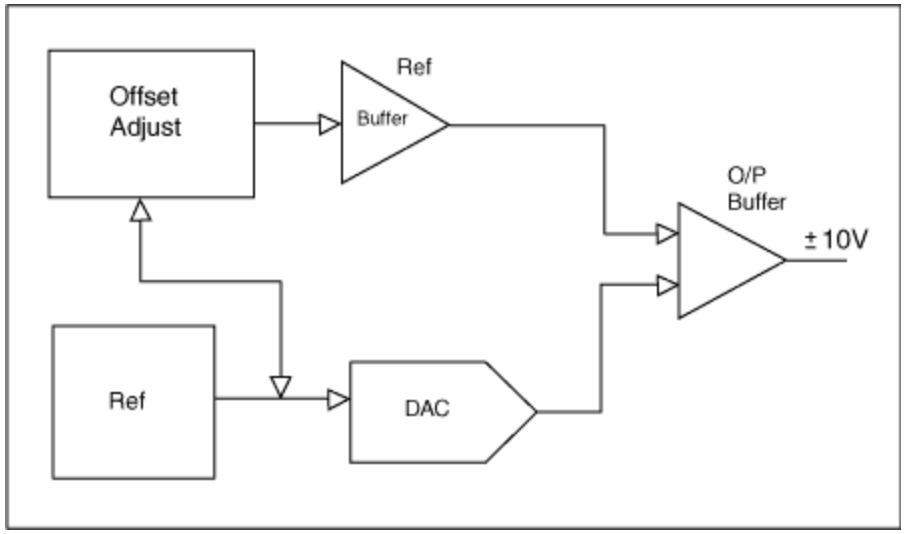

Figure 1a.

The circuit consists of the following parts:

- U1: MAX6133A, 2.5V Reference
- U2: MAX5443, 16 bit, 3.3V Supply, Serial DAC
- U3 & U4: OP07A, Precision Op Amp, ±15V supplies
- U5: MAX5491A, Precision Resistor Network with ESD Protection, 3:4 Ratio

- U6: MAX5491A, Precision Resistor Network with ESD Protection, 1:7 Ratio
- U7: MAX5423, 100K, 256 Tap, Nonvolatile, Digital Potentiometer

Reference

The 2.5V reference voltage is used by the DAC as its reference voltage and to generate the +1.429V. It is important that both these functions use the same reference voltage. Any error in the tracking between these two voltages will affect the outputs zero offset voltage. A common error will only affect the outputs full-scale gain, which is usually a much less critical parameter. 2.5V was chosen for the main reference voltage since it is a very common value and will work with both 3.3V and 5V power supplies. The MAX6133A was chosen because it has very good performance in a small µMAX® package. The critical parameters for this part are Output Voltage Accuracy (±0.06%), Temperature Coefficient (7ppm / °C), and Long Term Stability (145ppm / 1kHrs).

DAC

The most critical parameter in industrial control applications is zero offset error. The unipolar output MAX5443 in the example has ±2 LSBs of offset error and ±10 LSBs of gain error. This is more than adequate for most applications. In order to translate the DAC's output to bipolar offset circuitry is used do to shift the DACs zero code (minus full scale) to -10V and its mid scale code to 0V. Instead of getting less than ±2 LSB of zero code error specified at 0V the DAC's mid-scale code error is the sum of the zero code error and the gain error at mid-scale. This may not be acceptable so the example features a digital potentiometer to recalibrate the zero output.

Op Amp

Op amp U4 is used as a reference buffer between the reference divider resistors (U5) and op amp U3's gain resistors. If more than one DAC is in the system they can all share this buffered output. Op amp U3 provides the amplification and offsetting of the DAC voltage. Selection of the op amp and configuration of this stage will depend on the requirements of the load. The following load specifications need to be considered:

- Maximum voltage swing
- Maximum drive current
- Capacitance loading
- Short circuit protection
- ESD protection

The OP07A in the example can supply ±10V at 10mA to the load. The R1 and C2 network allows the op amp to drive large capacitive loads.

The op amp parameters that will affect system accuracy are V_{OS} (25µV) and I_{OS} (2nA). The effects of I_B (2nA) are negated by R3 and R4. By making the equivalent resistance in each input of the op amp the same, the effects of I_B cancel out. The slew rate of the system will be limited by the 0.1V/µS slew rate of the OP07A. This is usually not a problem in industrial control applications.

Resistor Networks

The U5 resistor network (3:4 ratio) divides the +2.5V reference down to +1.429V and the U6 resistor network (1:7 ratio) sets op amp U3's gain. The critical parameters here are initial ratio error (0.035%) and ratio temperature coefficient (5ppm / °C). The MAX5491 was chosen over conventional networks because of its ±2kV of ESD protection. This is important since one side of U6 may go off board and be subjected to ESD discharges.

Digital Potentiometer

The MAX5423 256 tap digital potentiometer is used to adjust the systems zero offset error. This part has a nonvolatile memory so offset values are retained even with the power shut off. The resistor network formed by U7, U5, and R2 were chosen to provide approximately ±100 LSBs of adjustment at 0V.

Analysis

A PSPICE sensitivity analysis was performed on this circuit. The results show the initial zero output error of 13 LSBs max. This error source can be calibrated out using the Digital Pot. The temperature analysis shows a total offset error of 0.126 LSBs / °C. With a 100 deg temp variation this would be 12.6 LSBs of offset error. This is adequate for most applications.

Table 1. Sensitivity Analysis, Zero Output, Intitial Tolerance Errors In LSBs at output

Ref Design	Component	Description	Error Source	Error Value	Error Units	Sensitivity	Sensitivity Units	Output Error (LSBs)
U1	MAX6133A	2.5V Ref	Output Accuracy	0.06	%	-2.74E - 04	LSBs/%	0.00
U2	MAX5443	16 bit DAC	Gain Error	5	LSBs	1.00E + 00	LSB/LSB	5.00
U3	OP07A	OpAMp	V_{OS}	25	µV	-2.62E + 04	LSB/V	0.66
U3	OP07A	OpAMp	I_{OS}	2	nA	8.55E + 07	LSB/A	0.17
U3	OP07A	OpAMp	I_B	2	nA	1.08E + 06	LSB/A	0.00
U4	OP07A	OpAMp	V_{OS}	25	µV	-2.29E + 04	LSB/V	0.57
U4	OP07A	OpAMp	I_{OS}	2	nA	1.68E + 08	LSB/A	0.34
U4	OP07A	OpAMp	I_B	2	nA	8.10E + 03	LSB/A	0.00
U5	MAX5491A	Res Network	Ratio Tolerance	0.035	%	1.40E + 02	LSB/%	4.90
U6	MAX5491A	Res Network	Ratio Tolerance	0.035	%	4.09E + 01	LSB/%	1.43
			Total					13.07

Table 2. Sensitivity Analysis, Zero Output, Temperature Errors In LSBs / Deg C at output

Ref Design	Component	Description	Error Source	Error Value	Error Units	Sensitivity	Sensitivity Units	Output Error (LSB / °C)
U1	MAX6133A	2.5V Ref	Output Temp Co	7	ppm/°C	2.74E - 04	LSBs/%	1.92E - 07
U2	MAX5443	16 bit DAC	Gain Temp Co	0.1	ppm/°C	5.00E - 02	LSB/%	5.00E - 07
U3	OP07A	OpAMp	V_{OS} Temp Co	0.6	µV/°C	-2.62E + 04	LSB/V	1.57E - 02
U3	OP07A	OpAMp	I_{OS} Temp Co	25	pA/°C	8.55E + 07	LSB/A	2.14E-03
U3	OP07A	OpAMp	I_B Temp Co	25	pA/°C	1.08E + 06	LSB/A	2.70E - 05
U4	OP07A	OpAMp	V_{OS} Temp Co	0.6	µV/°C	-2.29E + 04	LSB/V	1.38E - 02

U4	OP07A	OpAMp	I_B Temp Co	25	pA/°C	1.68E + 08	LSB/A	4.20E - 03
U4	OP07A	OpAMp	I_B Temp Co	25	pA/°C	8.10E + 03	LSB/A	2.02E - 07
U5	MAX5491A	Res Network	Ratio Temp Co	5	ppm/°C	1.40E + 02	LSB/%	7.00E - 02
U6	MAX5491A	Res Network	Ratio Tamp Co	5	ppm/°C	4.09E + 01	LSB/%	2.05E - 02
			Total					1.26E-01

Related Parts		
MAX5423	256-Tap, Nonvolatile, SPI-Interface, Digital Potentiometers	Free Samples
MAX5443	+3V/+5V, Serial-Input, Voltage-Output, 16-Bit DACs	Free Samples
MAX5491	Precision-Matched Resistor-Divider in SOT23	Free Samples
MAX6133	3ppm/°C, Low-Power, Low-Dropout Voltage Reference	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 2398: http://www.maximintegrated.com/an2398
REFERENCE DESIGN 2398, AN2398, AN 2398, APP2398, Appnote2398, Appnote 2398