# Process Change Notification

**PCN Number:** PCN-2016-63 **PCN Notification Date:** 09/30/2016

## Initial PCN

## STATS ChipPAC* Assembly Site Transfer from Shanghai to Jiangyin CHINA and Bill of Materials Substrate Core Change

Dear Customer,

This is notification of the STATS ChipPAC* Assembly Site Transfer from Shanghai to Jiangyin CHINA and Bill of Materials Substrate Core Change. STATS ChipPAC* was acquired by Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) in 2015. All assets will be consolidating to the JCET site location in Jiangyin CHINA targeted for the end of Q1_2017.

The described change(s) within this PCN will not take effect (i.e. Shipped) any earlier than **90** days from Initial PCN notification or the successful completion of the Cirrus Logic qualification, unless a customer agreement has been reached on an earlier implementation of the identified process change.

Cirrus Logic requests acknowledgement of receipt for this Initial PCN notification within 30 calendar days and acceptance of the identified change(s) within 90 days from receipt. Shipment of said material will commence after the 90 day period or upon successful completion of the Cirrus Logic defined qualification; lack of acknowledgement / communication is considered as acceptance.

Cirrus Logic would like to take this opportunity to thank our customers for their cooperation and assistance in this respective matter. Any specific or immediate inquiries should be directed to your local Field Sales Representative.

Sincerely,

Quality Systems Administrator
Cirrus Logic Corporate Quality
Phone: +1(512) 851-4000

* - STATS ChipPAC was acquired by Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) in 2015.

# Process Change Notification

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**Products Affected:**

The devices listed on this page are the complete list of affected devices. According to our records, one or more of these devices have been purchased by your organization within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

Technical details of this Process / Product Change follow on the next page(s).

| | | | | | | |
|---|---|---|---|---|---|---|
| **Title:** | STATS ChipPAC* Assembly Site Transfer from Shanghai to Jiangyin CHINA and Bill Of Materials Substrate Core Change | | | | | |
| **Customer Contact:** | Local Field Sales Representative | | **Phone:** | (512) 851-4000 | **Dept:** | Corporate Quality |
| **Proposed 1st Ship Date:** | Q1_2017 | | **Estimated Sample Availability Date:** | | Q1_2017 | |
| **Change Type:** | Site Transfer: Change Type = Major, but considered Minor; as the subcontractor (STATS ChipPAC*) is an existing qualified supplier for Cirrus Logic and there are no changes to the equipment or material. | | | | | |
| X | Assembly Site | | Assembly Process | | Assembly Materials | |
| | Wafer Fab Site | | Wafer Fab Process | | Wafer Fab Materials | |
| | Wafer Bump Site | | Wafer Bump Process | | Wafer Bump Material | |
| | Test Site | | Test Process | | Design | |
| | Electrical Specification | | Mechanical Specification | | Part Number | |
| | Packing/Shipping/Labeling | X | Other | | | |
| **Comments:** | Substrate Core Material Change | | | | | |

## PCN Details

**Description of Change:**

Cirrus Logic is qualifying the STATS ChipPAC* Assembly Site Transfer from Shanghai to Jiangyin CHINA and Bill Of Materials Substrate Core Change.

Below you will find an outline of the described changes for these components:

**Special Note:** Change Type = Major, but considered Minor.
The subcontractor (STATS ChipPAC*) is an existing qualified supplier.

- **BOM Change:**
  Substrate Core Material

  From: **CCL-HL832 Series** (Halogenated)
  To: **CCL-HL832NXA Series** (Non-Halogenated)
  **Reference**: Appendix A – Substrate Material Comparison Information

- **Assembly Site Change:**

  From: **STATS ChipPAC* site location in Shanghai CHINA**
  To: **STATS ChipPAC* site location in Jiangyin CHINA**
  Note: All equipment associated with the Assembly processes will remain the same

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**Reason for Change:**

STATS ChipPAC* was acquired by Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) in 2015. All assets will be consolidating to the JCET site location in Jiangyin CHINA targeted for the end of Q1_2017.

**Special Note:**

Earlier production level material may be available from the qualified Jiangyin CHINA site location, but shipment(s) from Cirrus Logic are contingent on successful qualification completion of the designated site transfer.

**Anticipated Impact on Form, Fit, Function, Quality or Reliability:**

No anticipated adverse impact to the Quality and/or Reliability of said product; as the transfer site is part of an already existing Cirrus Logic qualified subcontractor STATS ChipPAC* and there are no changes to the equipment or material.

**Product Affected:**

**Cirrus Logic Part Number(s):**

| |
|---|
| **EP9307-CRZ[R]/E2** |
| **EP9307-IRZ[R]/E2** |

**Changes To Product Identification Resulting From This PCN:**

The Cirrus Logic component symbolization on the external face of the device reflects the designated Assembly Site location. The Assembly Site Code on the external face of the designated components will change. Specifically, the 1st two characters of the PackMark will change:

From: **"BA"** To: **"BB"**
Note: All other symbolization will remain the same.

**Top Side Mark:**

| Mark Lay-out | Top Side Brand | STATS ChipPAC (Shanghai CHINA) | STATS ChipPAC (Jiangyin CHINA) | Comparison Results |
|---|---|---|---|---|
| See Below Illustration | **1st Line:** **Logo Line** | CIRRUS | CIRRUS | Same |
| | **2nd Line:** Cirrus Part Number | EP9307-xRZx | EP9307-xRZx | Same |
| | **3rd Line:** Package Mark | (FF**BA**RRLSYYWW**)**<br>FF = Foundry Code<br>AA = Assembly Site Code<br>RR = Die Rev<br>LS = Lot Sequence Code<br>YY = Year of Manufacture<br>WW = Work Week of Manufacture | (FF**BB**RRLSYYWW**)**<br>FF = Foundry Code<br>AA = Assembly Site Code<br>RR = Die Rev<br>LS = Lot Sequence Code<br>YY = Year of Manufacture<br>WW = Work Week of Manufacture | **Different** |

| | | | | |
|---|---|---|---|---|
| | **4th Line: ARM Logo** | ARM | ARM | Same |
| | **5th Line: Country of Origin** (COO) | CN | CN | Same |

**Note**: *Lot code and Date code characters vary according to the lot and timeframe of build

**Below is a 2D representative image of the Package: MF (Mark Format) = 242 Rev B**


## PACKAGE MARK FIELDS

12 character Package Mark appears on PO as
6 fields of 2 characters each in the following format:

FFAARRLSYYWW where,

FF = Foundry Code
AA = Assembly Site Code
RR = Die Rev Code
LS = Lot Sequence Code
YY = Year of Manufacture
WW = Work Week of Manufacture

## TOP SIDE BRAND

Line 1: Logo Line. Use CIRRUS LOGIC logo as shown.
Line 2: Part Number (12 spaces max.)
Line 3: Package Mark (12 spaces max.)
Line 4: ARM logo
Line 5: Country of Origin (COO).

## Family Qualification Data:

| This qualification has been specifically developed for the validation of this change. The qualification data validates that the proposed change meets the applicable released technical specifications. | | | | |
|---|---|---|---|---|
| **Qualification Schedule** | **Start:** | Sep 2016 | **End:** | Dec 2016 |

| Qualification Device Family Construction Details | | | |
|---|---|---|---|
| **Detail Description** | **Device 1** | **Device 2** | **Device 3** |
| **Part Number(s):** | EP9307-*RZ[R] | CS4208-CRZ[R] | JSCC Qual Vehicle |
| **Die Size:** | 41.73 $mm^2$ | 21.98 $mm^2$ | 22.21 $mm^2$ |
| **Package Type/Code:** | 272 TFBGA | 129 VFBGA | 285 TFBGA |
| **Mold Compound:** | Sumitomo EME-G770LC | Kyocera KE-G1250LKDS | Sumitomo EME-G750S-E |
| **Substrate Material:** | 2 layer, Substrate UMTC: 046043ESUB-A_00 | 2 layer, Substrate UMTC, 030848Jsub-A_07 | 4 layer, Substrate UMTC: 0.8P, 030356L_U2 |
| **Die Attach Material:** | Ablebond 2000 | Ablebond 2000 | Ablebond 2300 |
| **Wire Material:** | Au 2N | Cu Pd | EX1 Type (Cu Pd Coated) |
| **Wire Size:** | 1.0 mil | 0.8 mil | 0.8 mil |
| **Solder Ball Composition - Size:** | Sn / 4% Ag / 0.5% Cu – 400um | Sn / 3% Ag / 0.5% Cu – 250um | Sn / 3% Ag / 0.5% Cu – 300um |

The Qualification Plans are designed using JEDEC and other applicable industry standards. An overall summary of the Qualification results will be submitted upon completion.

## Device Package Level Qualification Plan

| **Purpose** |
|---|
| STATS ChipPAC* Package level Qualification for Assembly Site Transfer from Shanghai to Jiangyin CHINA |

| Stress Name | Stress Method | Conditions | # of Lots | Qty per Lot | Read Points | Failure Criteria | Results (PASS/FAIL) |
|---|---|---|---|---|---|---|---|
| **PC** (Pre-Condition) | JESD22-A113 Per component MSL classification per J-STD-020 | Bake: 24Hr +125'C; MSL 3 192Hr 30'C / 60% RH Soak, (Reflow 260'C x 3) | 5 | Sufficient for stress test coverage | Precon MSL3 | 0 fails | |
| **TC** (Temperature Cycle) | JEDEC JESD22-A104 | -40°C to +125°C for 850 cycles or -55°C to +125°C for 1000 cycles Post Precondition | 5 | 77 | 850 or 1000 Cycles | 0 fails | |
| **THB / BHAST** (Temperature- Humidity-Bias) | JEDEC JESD22-A101 and A110 | 85°C/85% RH/1000 Hrs / +110'C 85% RH 264 Hrs | 4 | 77 | 1000 / 264 Hrs | 0 fails | |
| **UHAST** (Unbiased HAST) | JEDEC JESD22-A118 | +110'C/85% RH, 17.7 PSIA, 264Hrs | 5 | 77 | 264 Hrs | 0 fails | |
| **HTSL** (High Temperature Storage Life) | JEDEC JESD22-A103 | +150°C for 1000Hrs | 3 | 45 | 1000 Hrs | 0 fails | |
| **WBP** (Wire Bond Pull) | MIL-STD-883 M2011 | Paragraph 3 of Reference Specification Table 1 Figure 2011-2 | | | | 0 fails | |
| **WBS** (Wire Bond Shear) | JESD22-B116 | | | | | 0 fails | |
| **PPD** (Package Physical Dimensions) | Case Outline Drawing | | | | Meet all case outline drawing tolerances | No deviations from package drawing | |

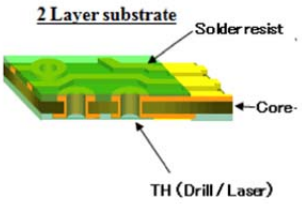
**Notes:**

- Qualification tests "pass" on zero fails for each test

## Appendix A - Substrate Material Comparison Information

### Nexus 2 Layer Substrate Cross Section

| Layer | Current | New | |
|---|---|---|---|
| Top Pad Finish | Ni 5um<br>Au 0.5 um (Min) | Ni 5um<br>Au 0.5 um (Min) | No Change |
| Solder Mask | AUS303 | AUS303 | No Change |
| Copper Trace | Cu Foil 12 um<br>Cu Plating 15 um | Cu Foil 12 um<br>Cu Plating 15 um | No Change |
| Core Material | HL832 | HL832NXA-EX | Changed |
| Copper Trace | Cu Foil 12 um<br>Cu Plating 15 um | Cu Foil 12 um<br>Cu Plating 15 um | No Change |
| Solder Mask | AUS303 | AUS303 | No Change |
| Bottom Pad Finish | Ni 5um<br>Au 0.5 – 1.0 um | Ni 5um<br>Au 0.5 – 1.0 um | No Change |




**Note:** There are no changes to the Top/Bottom Pad, Solder Mask or Copper Trace material

### Existing Non-NXA material versus NXA Core Material Comparison

| Item | Condition | | Unit | HL832 | HL832NX type A |
|---|---|---|---|---|---|
| Tg | DMA | | degC | 210 | 230 |
| | TMA | | degC | 180 | 200 |
| CTE | XY | < Tg | ppm/degC | 15 | 14 |
| | | > Tg | ppm/degC | 5 | 5 |
| | Z | < Tg | ppm/degC | 55 | 30 |
| | | > Tg | ppm/degC | 220 | 140 |
| Cu peel strength | 12um Cu (LP) | | kN/m | 0.9 | 0.85 |
| Flexural strength | 25degC | | MPa | 550 | 450 |
| Flexural modulus | 25degC | | GPa | 24 | 28 |
| Tensile strength | 25degC | | MPa | 320 | 270 |
| Youngs modulus | 25degC | | GPa | 24 | 28 |
| Poisson ratio | 25degC | | - | 0.18 | 0.19 |
| Thermal conductivity | 25degC | | W/mK | 0.30 | 0.80 |
| Moisture absorption | C168/85/85 | | wt% | 0.42 | 0.44 |
| Dielectric constant | 1 GHz | | - | 4.3 | 4.9 |
| Dissipation factor | 1 GHz | | - | 0.016 | 0.011 |
| Flame resistance (Green) | E-168 / 70 | | UL94 | V-0 *Halogenated* | V-0 *Non Halogenated* |

**Note:** NXA material has a higher Tg, lower CTE and is Non-Halogenated