

Vishay Siliconix

N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) ^a	Q _g (TYP.)			
100	0.026 at V _{GS} = 10 V	10.3	5.8 nC			
100	0.033 at V _{GS} = 4.5 V	9.2	3.6110			



Ordering Information:

Si4058DY-T1-GE3 (lead (Pb)-free and halogen-free)

FEATURES

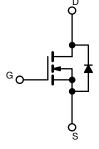
- ThunderFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- DC/DC primary side switch
- Synchronous rectification
- · Fast charger
- Industrial



N-Channel MOSFET

ABSOLUTE MAXIMUM RATING	$13 (1_A = 25 \text{ G}, t)$	inless otherv	vise noted)		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V _{DS}	100	V	
Gate-Source Voltage		V _{GS}	± 20	v	
	T _C = 25 °C		10.3		
Continuous Drain Comment /T 150 °C	T _C = 70 °C	1	8.3		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	l _D	7 b, c		
	T _A = 70 °C	1	5.5 ^{b, c}	A	
Pulsed Drain Current (t = 300 μs)		I _{DM}	50		
Continuous Source-Drain Diode Current T _C = 25 °C		I _S	5		
Single Pulse Avalanche Current	l 0.1 mall	I _{AS}	15		
Avalanche Energy	L = 0.1 mH	E _{AS}	11.2	mJ	
	T _C = 25 °C		5.6		
Maniana Danian Dispiration	T _C = 70 °C	P _D	3.6	14/	
Maximum Power Dissipation	T _A = 25 °C		2.6 ^{b, c}	W	
	T _A = 70 °C	1	1.6 ^{b, c}		
Operating Junction and Storage Temperature	T _J , T _{stg}	-55 to +150	°C		

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT			
Maximum Junction-to-Ambient b, d	t ≤ 10 s	R _{thJA}	39	48	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	18	22	6/ ۷۷		

Notes

- a. Based on $T_C = 25$ °C.
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s.
- d. Maximum under steady state conditions is 90 °C/W.

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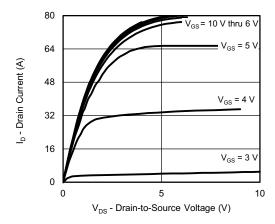
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$			61	-	m\//°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-3.8	-	mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.2	-	2.8	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
Zara Cata Valtaga Drain Current	1	V _{DS} = 100 V, V _{GS} = 0 V	-	-	1	μA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V, T _J = 70 °C	-	-	10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20	-	-	Α	
Dunin Course On Otata Besistance 3	_	V _{GS} = 10 V, I _D = 10 A	-	0.0217	0.0260	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 8 A	-	0.0266	0.0330		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 10 A	-	31	-	S	
Dynamic ^b				•			
Input Capacitance	C _{iss}		-	690	-	рF	
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	280	-		
Reverse Transfer Capacitance	C _{rss}		-	11	-		
	0	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 10 A	-	12	18		
Total Gate Charge	Q _g		-	5.8	9	nC	
Gate-Source Charge	Q _{gs}	$V_{DS} = 50 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$	-	2.1	-		
Gate-Drain Charge	Q _{gd}		-	2.2	-		
Output Charge	Q _{oss}	V _{DS} = 50 V, V _{GS} = 0 V	-	22.5	35		
Gate Resistance	R_g	f = 1 MHz	0.8	2.2	4.0	Ω	
Turn-On Delay Time	t _{d(on)}		-	8	16		
Rise Time	t _r	$V_{DD} = 50 \text{ V}, R_{L} = 5 \Omega$	-	17	34	-	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	11	22		
Fall Time	t _f		-	8	16		
Turn-On Delay Time	t _{d(on)}		-	7	14	ns	
Rise Time	t _r	$V_{DD} = 50 \text{ V}, R_{L} = 5 \Omega$	-	16	32	-	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	12	24		
Fall Time	t _f		-	7	14		
Drain-Source Body Diode Characteristi	cs						
Continuous Source-Drain Diode Current	Is	T _C = 25 °C		-	5	^	
Pulse Diode Forward Current ^a	I _{SM}		-	-	50	Α	
Body Diode Voltage	V _{SD}	I _S = 5 A	-	0.81	1.1	V	
Body Diode Reverse Recovery Time	t _{rr}		-	56	112	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 10 A, di/dt = 100 A/μs,	-	60	120	nC	
Reverse Recovery Fall Time	t _a	T _J = 25 °C	-	48	-	no	
Reverse Recovery Rise Time	t _b		-	8	-	ns	

Notes

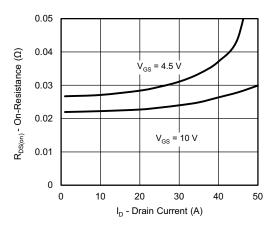
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

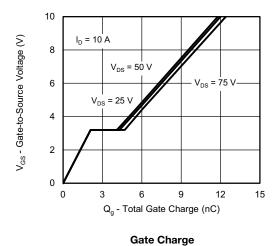


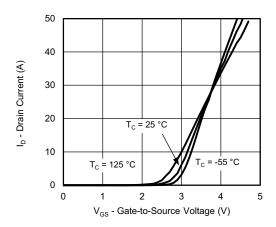


Output Characteristics

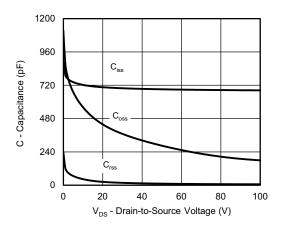


On-Resistance vs. Drain Current

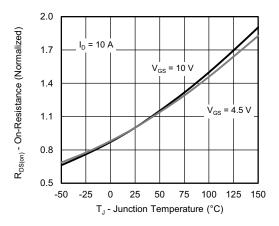




Transfer Characteristics

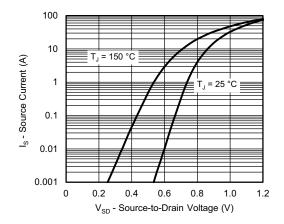


Capacitance

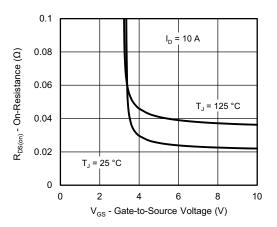


On-Resistance vs. Junction Temperature

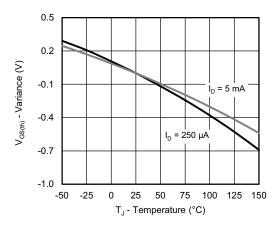




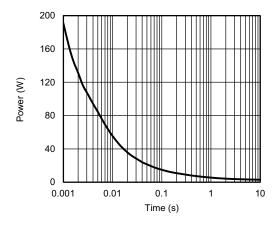
Source-Drain Diode Forward Voltage



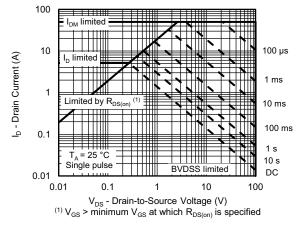
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

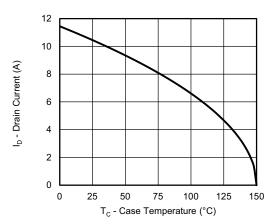


Single Pulse Power, Junction-to-Ambient

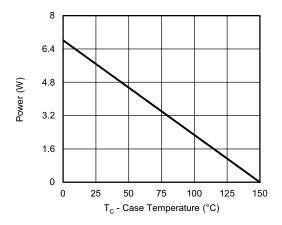


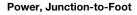
Safe Operating Area, Junction-to-Ambient

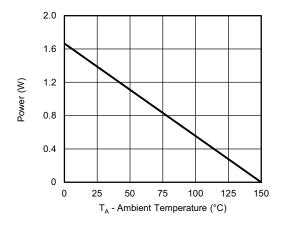




Current Derating a





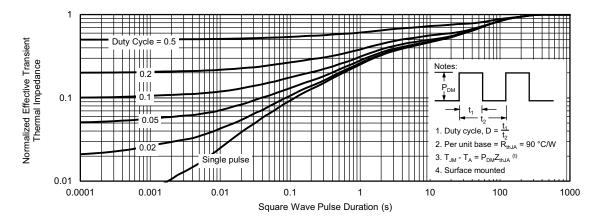


Power, Junction-to-Ambient

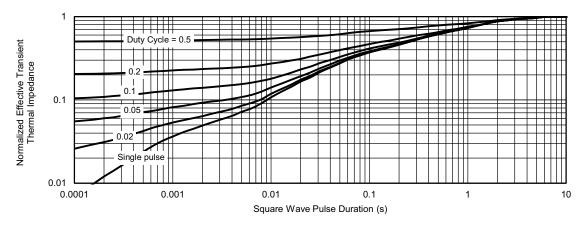
Note

a. The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67409.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	INCHES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

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