**Freescale Semiconductor**
Product Brief

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# MAC7200 Product Brief

## 32-bit Flash-based Microcontroller Family

Designed for automotive applications, MAC7200 devices comprise a family of 32-bit Flash-based microcontrollers. The MAC7200 family's pin compatibility enables users to choose between different memory and peripheral options for scalable designs. All devices are composed of a 32-bit central processing unit (ARM7TDMI-S™), and an enhanced direct memory Access (eDMA) controller combined with a cross-bar bus switch (XBS) to support efficient transfers between embedded Flash EEPROM memory, system RAM, on-chip peripherals and, optionally, external devices via an external bus interface (EBI). The Flash memory is partitioned into large blocks suitable for program storage, and smaller blocks suitable for EEPROM emulation, such that the best fit may be chosen for each application. One block is defined as a Shadow Block, intended as program storage available in Bootloader and Secure Bootloader modes.

The peripheral set includes asynchronous serial communications interfaces (eSCI), deserial serial

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peripheral interfaces (DSPI), an $I^2C$-bus interface, a configurable 16-bit timer subsystem (eMIOS) for functions such as dual action capture/compare and output pulse width modulation, a multi-channel 10/12-bit analog-to-digital converter (ATD), and CAN-compatible modules (FlexCAN). The inclusion of an on-chip oscillator (OSC) and phase-locked loop clock and reset generator (CRG) allows power consumption and performance to be adjusted to suit operational requirements. All module pins, with the exception of the ATD and CLKOUT pins, can be configured as bi-directional ports, and the devices provide several dedicated general purpose input/output port pins. All port pins can provide interrupt capability. The operating frequency maximum is 70 MHz across a range of –40°C to 150°C junction temperature. Devices are offered in 100-pin LQFP and 144-pin LQFP packages.

# 1 Features

In order to tailor functionality to system requirements, various package options implement different peripheral function combinations, as detailed in Table 1.

**Table 1. MAC7200 Device Derivatives**

| Device | Flash Partitions | | | SRAM | External Bus | ATD Channels | FlexCAN Modules | | eSCI Modules | | DSPI Modules | | | $I^2C$ Module | eMIOS Module | Timer Module | General-Purpose Input/Output Ports/Pins | | | | | | | | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Large | Small[2] | Shadow | | | | A | B | A | B | A | B | C | | | | A | B | C | D | E[3] | F | G | Total (max.)[1] | |
| MAC7201 | 448 KBytes | 64 KBytes | 32 KBytes | 32 KBytes | ✓ | 16 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | 8 or 16 channels,[4,5] 16-bit | 10 channels, 32-bit One 24-bit RTI | 16 | 16 | 16 | 12 | 16 | 16 | 10 | 102 | 144 LQFP |
| MAC7211 | | | | | ✓ | 8 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | 16 | 16 | 16 | 14 | 8 | 16 | 16 | 102 | 144 LQFP |
| MAC7241 | | | | | | 15 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | 3 | 16 | – | 6 | 15 | 16 | 10 | 66 | 100 LQFP |
| MAC7202 | 256 KBytes | | | 20 KBytes | ✓ | 16 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | 16 | 16 | 16 | 12 | 16 | 16 | 10 | 102 | 144 LQFP |
| MAC7212 | | | | | ✓ | 8 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | 16 | 16 | 16 | 14 | 8 | 16 | 16 | 102 | 144 LQFP |
| MAC7242 | | | | | | 15 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | 3 | 16 | – | 6 | 15 | 16 | 10 | 66 | 100 LQFP |

NOTES:
1. Peripheral functions and GPIO ports share pin positions, so the maximum assumes no peripherals are in use. Also, the Nexus Class 3 port shares GPIO pin positions in 100-pin packages.
2. Implemented as four 16 Kbyte blocks to support EEPROM emulation.
3. Port E pins may be used only for input (or peripheral function).
4. MAC72*x*1 devices implement channels 0 through 7 via primary multiplexing, while channels 8 through 15 are available via secondary or tertiary multiplexing with pins alternatively used for FlexCAN and DSPI functions.
5. MAC72*x*2 devices implement channels 0 through 7.

## 1.1 Chip-Level Features

- Up to 544 Kbytes of wide access Flash EEPROM
  - — Four Flash page buffers all 128-bits wide and individually configurable as either instruction or data buffers.
  - — Page buffers can be configured to enable fetch ahead and either least recently used or counter based buffer replacement schemes.

- Program and erase operations controlled by state machine.
- Internally generated program and erase voltages.
- ECC enabled array with 2-bit error detection, 1-bit error correction providing transparent operation.
- 64-bit minimum write size.
- Flash configuration:
  - Two or four large memory partitions, subdivided into blocks for optimum flexibility,
  - Four or eight small memory partitions, subdivided into blocks for optimum flexibility,
  - One relocatable 32 Kbyte shadow block, typically used for bootloader.
- Memory partitioning supports flexible utilization such as EEPROM emulation, application code or small protected blocks of configuration code or data.
- Read or program/erase access on flash partition basis.
- Flash BIU support for access protection for user/supervisor mode and instruction/data accesses.
- Protection violation flag.
- Flash lockout recovery mechanism through JTAG interface.
- 100,000 write/erase endurance.
- 20 year data retention.

• Up to 32 Kbyte RAM
- Single cycle accesses to RAM for byte, half-word and word reads and writes.
- ECC enabled array with 2-bit error detection, 1-bit error correction.

• Flexible Chip Modes for Debug and Security
- Normal Single-Chip Mode
  - All debug features available.
  - Boot from program Flash.
- Secured Single-Chip Mode
  - No debug features available.
  - Boot from program Flash.
  - JTAG lockout recovery available.
- Normal Expanded Mode
  - All debug features available.
  - Boot from external memory.
- Secured Expanded Mode
  - No debug features available.
  - Boot from external memory.
  - JTAG lockout recovery available.
- Bootloader Mode
  - All debug features available.
  - Boot from shadow Flash area.

  - Secured Bootloader Mode
    - No debug features available.
    - Boot from shadow Flash area.
    - JTAG lockout recovery available.
- Internal Voltage Regulators (VREG)
  - On-chip voltage regulators provide Flash, oscillator, PLL and core supply voltages from single 5 V input.
  - On-board bypass capacitors for voltage regulation.
- 100-pin LQFP and 144-pin LQFP package options
  - I/O lines with 5 V input and drive capability.
  - Programmable pull-up/pull-down or no-pull on all port pins.
  - Programmable slew rate on all bidirectional port pins.
  - 5 V ATD converter inputs.
  - 1.5 V logic supply.

## 1.2 Module Features

### 1.2.1 32-bit ARM7TDMI-S™ RISC Core

- Up to 70 MHz operating frequency.
- Efficient code density through 16-bit instructions (Thumb mode).
- 128-bit wide data path to on-chip Flash memory.
- Alternate general purpose registers.
- Byte (8-bit), half-word (16-bit), word (32-bit) data types supported.
- Cores and memory connected using high performance AMBA AHB bus.
- 32-bit slave bus provides separate interface for slower system peripherals.

### 1.2.2 Interrupt Controller

- 64 vectored interrupt sources.
- Interrupt sources available from internal peripherals, eDMA controller, software watchdog timer and external sources.
- Dedicated non-maskable interrupt pin (XIRQ/NMI) with programmable edge detection.
- 16 programmable interrupt priorities on every source.
- Multiple level interrupt nesting.
- Hardware support for first nesting level.
- Normal and fast interrupts supported.

### 1.2.3 Enhanced Direct Memory Access Controller (eDMA)

- DMA transfers possible between system memories, DSPI, eSCI, $I^2C$, ATD, eMIOS and general purpose I/O
- Programmable DMA channel multiplexer allows assignment of any DMA source to any available DMA channel.
- All DMA transfers use dual address format.
- Programmable transfer control descriptor stored in local DMA memory.
- Programmable source and destination address with configurable offset.
- 32-bit minor and 16-bit major loop counters for nested transfers.
- Different final source and destination addresses allow circular queue operation.
- Programmable priority levels for each channel.
- Bandwidth control for each channel.
- Programmable transfer sizes through major and minor loop counters.
- Independently programmable read/write sizes.
- Periodic triggering of up to 8 channels.

### 1.2.4 External Bus Interface (EBI)

- 20-bit address bus.
- 16-bit data bus (32-bit accesses automatically handled as two 16-bit accesses).
- 3 chip selects:
  - Each chip select pin assignable to an address range.
  - Configurable number of wait states available for accesses to slower external devices.
  - Access time may be controlled by external device via the $\overline{TA}$ pin.
- Burst accesses supported.
- MAC72x1 device always the bus master.

### 1.2.5 Analog-to-Digital Converter (ATD)

- Up to 16 analog input channels.
- 10-bit resolution with ±1-bit accuracy or 12-bit resolution with ±3-bit accuracy.
- 2 μs minimum conversion time.
- Internal sample and hold circuitry.
- Pre-measurement discharge of internal sample and hold circuit possible for all channels.
- Programmable input sample time for various source impedances.
- Queued conversion sequences supported by DMA controller.
- Analog inputs configurable as external sample triggers.
- On-chip timer triggers for sampling.

### 1.2.6 Controller-Area Network Module (FlexCAN)

- Full implementation of the CAN 2.0 protocol specification.
- Programmable bit rate up to 1 Mbps.
- 32 flexible mail boxes of 0-8 bytes data length on all modules.
- All mail boxes configurable for either Rx/Tx.
- Unused mail boxes space can be used as general purpose RAM.
- Supports standard or extended messages.
- Time stamp, based on a 16-bit free-running counter.
- Maskable interrupts.
- Programmable I/O modes.
- External transceiver assumed.

### 1.2.7 Enhanced Modular I/O Subsystem (eMIOS)

- Up to 16 unified channels, with every channel able to provide all timer functions and modes.
- All channels can be enabled for eDMA service.
- Channels can be individually disabled to assist with power saving.
- 16-bit counter bus for sharing time base around the module.
- One global prescaler and an individual prescaler available for each channel.
- Fourteen channel operating modes available on all channels:
  - Modulus counter,
  - Single action input capture or output compare,
  - Input pulse width and period measurement,
  - Double action output compare,
  - Output pulse width and frequency modulation,
  - Output pulse width modulation,
  - Center aligned output pulse width modulation with dead time insertion,
  - Pulse or edge accumulation and counting,
  - Windowed programmable time accumulation,
  - Quadrature decode.
- General purpose I/O available on unused eMIOS pins.

### 1.2.8 Deserial Serial Peripheral Interface (DSPI)

- Full duplex, synchronous transfers.
- Master or slave operation.
- Programmable master bit rates.
- Programmable clock polarity and phase.
- End-of-transmission interrupt flag.

- Programmable transfer baud rate.
- Programmable data frames from 4-bits to 16-bits.
- Up to six chip select lines enable 64 external devices to be selected using external muxing from a single DSPI.
- Six clock and transfer attributes registers.
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching.
- Two dedicated DMA request lines on each peripheral for receive and transmit data.
- FIFO for buffering up to 4 transfers on the transmit and receive side.
- Queueing operation possible through use of the DMA controllers channels.
- General purpose I/O functionality on pins when not used for DSPI

### 1.2.9 Enhanced Serial Communications Interface (eSCI)

- Standard non return-to-zero (NRZ) mark/space format.
- Full-duplex operation.
- Software selectable word length (8-bit or 9-bit words).
- 10/11 or 13/14 bit break character possible.
- 13-bit programmable baud-rate modulus counter.
- Separately enabled transmitter and receiver.
- Separate receiver and transmitter CPU interrupt requests.
- Programmable transmitter output polarity.
- Two receiver wake-up methods.
- Interrupt-driven operation.
- Receiver framing error detection.
- Hardware parity checking.
- 1/16 bit time noise reduction.
- LIN master mode state machine
  - — Supports generation of LIN message header.
  - — Detection and flagging of LIN errors.
- Two DMA request lines on each peripheral for receive and transmit data.

### 1.2.10 Inter-IC Bus Module ($I^2C$)

- Two wire bi-directional serial bus for on board communications.
- Compatibility with $I^2C$ bus standard.
- Multimaster operation.
- Software-programmable for one of 256 different serial clock frequencies.
- Software-selectable acknowledge bit.
- Interrupt-driven byte-by-byte data transfer.

- Arbitration-lost interrupt with automatic mode switching from master to slave.
- Calling address identification interrupt.
- Start and stop signal generation/detection.
- Repeated START signal generation.
- Acknowledge bit generation/detection.
- Bus-busy detection.
- Two DMA request lines to receive and transmit data

### 1.2.11 Clock and Reset Generator (CRG)

- Low power amplitude loop control Pierce oscillator.
- Clock generation and reset control performed in CRG.
- Phase-locked loop clock frequency multiplier.
- Self clocking mode available in absence of external clock.
- Low power 4 MHz to 40 MHz crystal oscillator reference clock.

### 1.2.12 Periodic Interrupt Timer (PIT) Module

- Independent timeout period for each timer.
- Four 32-bit general purpose PIT timers, configurable to generate DMA trigger pulses.
- Four 32-bit PITs to generate DMA trigger pulse.
- Two 32-bit timers that can be configured to generate ATD trigger pulses.
- One 24-bit real-time interrupt (RTI) timer.
- Software may select the oscillator or system clock to drive RTI counter.

### 1.2.13 Miscellaneous Control Module (MCM)

- Software watchdog timer with programmable system reset or interrupt response and optional windowed mode (may be driven by the oscillator or system clock).
- Access address information for faulted memory accesses.
- NMI configuration.

### 1.2.14 System Services Module (SSM)

- System configuration and status:
  - Memory sizes and status,
  - Security status,
  - Device mode,
  - eDMA status,
  - Debug Port,
  - Nexus Status,

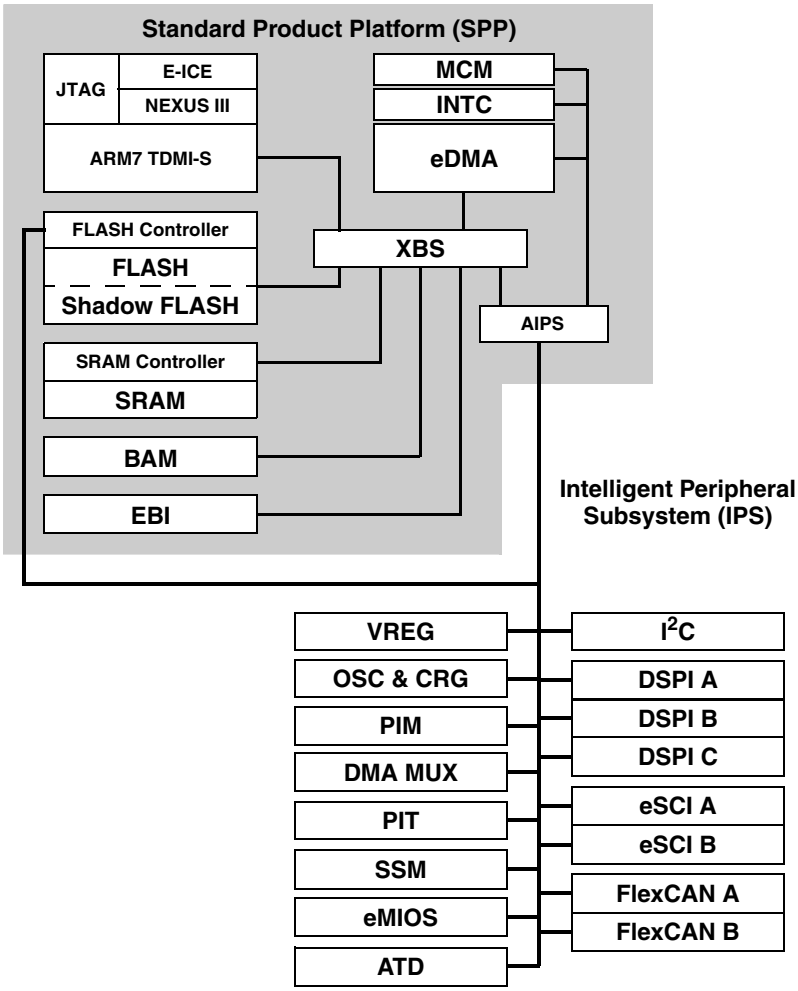
— System Reset.

### 1.2.15 General Purpose Input/Output (PIM)

- All pins, except the ATD and CLKOUT pins, are bidirectional and independently configurable.
- Port pins shared with peripherals, with
  — Up to 66 port pins on 100-pin LQFP devices,
  — Up to 102 port pins on 144-pin LQFP devices.

## 1.3 Block Diagram

Figure 1 shows the functional connections of modules included on MAC7200 devices.




**Note:** Refer to Table 1 for details of peripheral and memory configurations

**Figure 1. MAC7200 Family Block Diagram**

# 2 Developer Environment

The following development support features are integrated into all MAC7200 devices:

- Real time instruction and data trace support via Nexus Class 3 port.
- Nexus port shared with peripheral pins available on all devices.
- Alternate Nexus port not shared with peripheral pins available on 144-LQFP package.
- ARM Embedded ICE debug support on all devices.
- JTAG Test Access Port (TAP) interface.
- Debug mode access to CPU registers.
- Real-time memory access.
- Hardware breakpoints.

# 3 Documentation and Ordering

Table 2 lists the documents that provide a complete description of the MAC7200 microcontroller family and are required to design properly with devices in the family. Documentation is available from a local Freescale Semiconductor sales office or distributor, the Freescale Literature Distribution Center, or through the Freescale web site at http://www.freescale.com.

**Table 2. MAC7200 Family Documentation**

| Document Name | Order Number |
|---|---|
| MAC7200 Microcontroller Family Reference Manual | MAC7200RM |
| ARM Architecture Reference Manual (Second Edition) | ARM DDI 0100E |
| ARM7TDMI-S (Rev 4) Technical Reference Manual (Issue A) | ARM DDI 0234A |
| LIN Specification 2.0 | |
| CAN protocol specification, Version 2.0 B | |

Figure 2 shows an example orderable part number and description that is used to completely specify a MAC7200 family device.

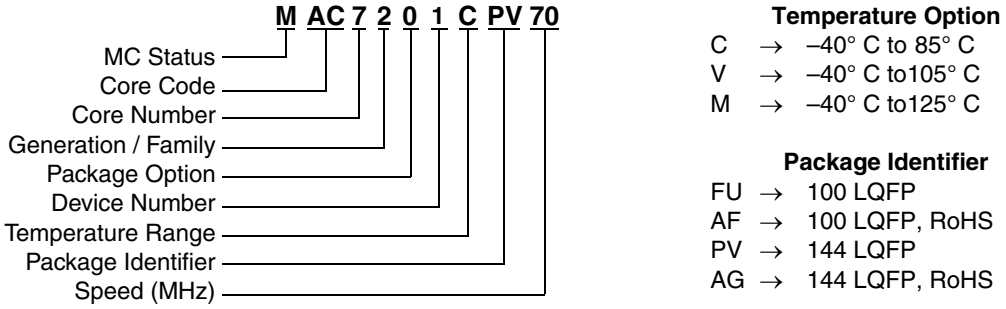



**Figure 2. Orderable Part Number Example**

# 4 Revision History

| Revision | Date | Updates / Changes |
|---|---|---|
| 0 | March 2007 | Initial release. |

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