100 MHz to 1000 MHz Integrated Broadband Receiver

FEATURES

- IQ quadrature demodulator
- Integrated fractional-N PLL and VCO
- Gain control range: 60 dB
- Input frequency range: 100 MHz to 1000 MHz
- Input P1dB: +12 dBm at 0 dB gain
- Input IP3: +22.5 dBm at 0 dB gain
- Noise figure: 11 dB at >39 dB gain, 49 dB at 0 dB gain
- Baseband 1 dB bandwidth: 250 MHz in wideband mode, 50 MHz in narrow-band mode
- SPI/I^2C serial interface
- Power supply: +3.3 V/350 mA

APPLICATIONS

- Broadband communications
- Cellular communications
- Satellite communications

GENERAL DESCRIPTION

The ADRF6850 is a highly integrated broadband quadrature demodulator, frequency synthesizer, and variable gain amplifier (VGA). The device covers an operating frequency range from 100 MHz to 1000 MHz for use in both narrow-band and wideband communications applications, performing quadrature demodulation from IF directly to baseband frequencies.

The ADRF6850 demodulator includes a high modulus fractional-N frequency synthesizer with integrated VCO, providing better than 1 Hz frequency resolution, and a 60 dB gain control range provided by a front-end VGA.

Control of all the on-chip registers is through a user-selected SPI interface or I^2C interface. The device operates from a single power supply ranging from 3.15 V to 3.45 V.

FUNCTIONAL BLOCK DIAGRAM

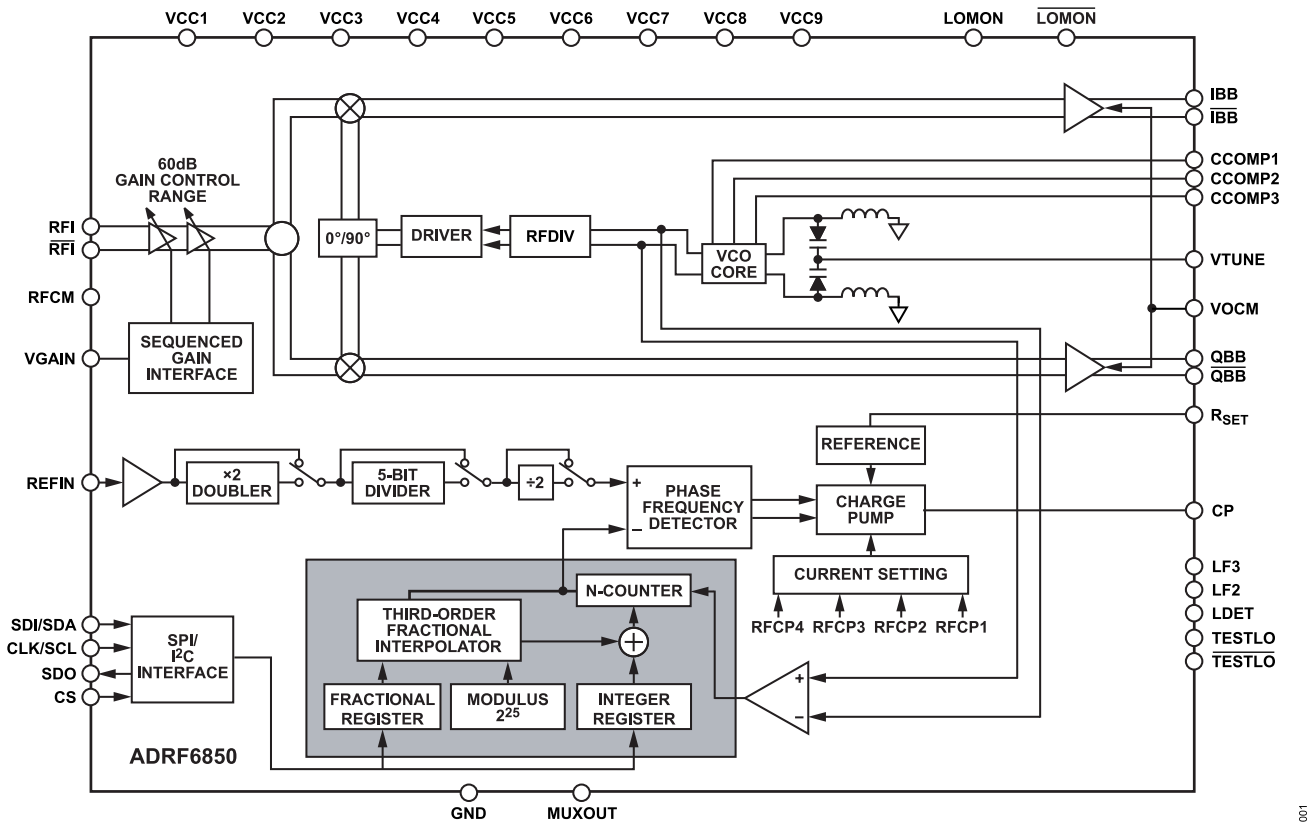

Figure 1.

Rev. A

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

7/2022—Rev. 0 to Rev. A

Deleted Evaluation Board Section, General Description Section, Hardware Description Section, Power Supplies Section, Recommended Decoupling for Supplies Section, SPI and I^2C Interface Section, Baseband Outputs and VOCM Section, Loop Filter Section, Reference Input Section, TESTLO Inputs Section, LOMON Outputs Section, CCOMPx Pins Section, MUXOUT Section, Lock Detect (LDET) Section, RF Inputs (RFI, RFCM, and $\overline{\text{RFI}}$) Section, and VGAIN Section 31
Changes to Evaluation Boards 32

10/2010—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.3 V; ambient temperature (T_A) = 25°C; Z_S = 50 Ω; Z_L = 100 Ω differential; PLL loop bandwidth = 50 kHz; REFIN = 13.5 MHz; PFD = 27 MHz; baseband frequency = 20 MHz, narrow-band mode, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT	RFI, $\overline{RFI}$, VGAIN pins				
Operating Frequency Range		100		1000	MHz
Input P1dB	0 dB gain		+12		dBm
	60 dB gain		−48		dBm
Input IP3	0 dB gain		+22.5		dBm
	60 dB gain		−38		dBm
Input IP2	0 dB gain, single-ended input		+40		dBm
	60 dB gain, single-ended input		−20		dBm
Noise Figure (NF)	0 dB gain		49		dB
	<39 dB gain NF rises 1:1 as gain in dB falls				
	>39 dB gain		11		dB
Maximum Gain	Z_S = 50 Ω single-ended, Z_L = 100 Ω differential		60		dB
Minimum Gain	Z_S = 50 Ω single-ended, Z_L = 100 Ω differential		0		dB
Gain Conformance Error[1]	V_{GAIN} from 200 mV to 1.3 V		0.5		dB
Gain Slope			25		mV/dB
VGAIN Input Impedance			20		kΩ
Return Loss	Relative to Z_S = 50 Ω, 100 MHz to 1 GHz		15		dB
REFERENCE CHARACTERISTICS	REFIN pin				
Input Frequency	With R divide-by-2 divider enabled	10		300	MHz
	With R divide-by-2 divider disabled	10		165	MHz
REFIN Input Sensitivity		0.4		V_{CC}	V p-p
REFIN Input Capacitance				10	pF
REFIN Input Current				±100	µA
CHARGE PUMP	CP and RSET pins				
I_{CP} Sink/Source	Programmable				
High Value	With R_{SET} = 4.7 kΩ		5		mA
Low Value			312.5		µA
Absolute Accuracy	With R_{SET} = 4.7 kΩ		2.5		%
VCO					
Gain	K_{VCO}		15		MHz/V
SYNTHESIZER SPECIFICATIONS	Loop bandwidth = 50 kHz				
Frequency Increment			1		Hz
Phase Frequency Detector		10		30	MHz
Spurs					
	Integer boundary < loop bandwidth		−55		dBc
	>10 MHz offset from carrier		−70		dBc
Phase Noise	LO frequency = 1000 MHz				
	@ 10 Hz offset		−75		dBc/Hz
	@ 100 Hz offset		−80		dBc/Hz
	@ 1 kHz offset		−90		dBc/Hz
	@ 10 kHz offset		−98		dBc/Hz
	@ 100 kHz offset		−110		dBc/Hz
	@ 1 MHz offset		−136		dBc/Hz
	>10 MHz offset		−149		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.26		°rms
Frequency Settling	Any step size, maximum frequency error = 1 kHz		260		µs

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Maximum Frequency Step for No Autocalibration	Frequency step with no autocalibration routine; Register CR24, Bit 0 = 1			100	kHz
BASEBAND OUTPUTS	IBB, $\overline{IBB}$, QBB, $\overline{QBB}$, VOCM pins				
Maximum Swing	Driving Z_L = 100 Ω differential		2.5		V p-p
Common-Mode Range		1.2		1.6	V
Output Impedance	Differential		28		Ω
Output DC Offset	RFI terminated in Z_S = 50 Ω		±20		mV
1 dB Bandwidth					
Wideband Mode			250		MHz
Narrow-Band Mode			50		MHz
IQ Balance					
Amplitude					
Wideband Mode	Baseband frequency ≤ 250 MHz		±0.1		dB
Narrow-Band Mode	Baseband frequency ≤ 33.2 MHz		±0.1		dB
Phase					
Wideband Mode	Baseband frequency ≤ 250 MHz		±0.5		Degrees
Narrow-Band Mode	Baseband frequency ≤ 33.2 MHz		±0.25		Degrees
IQ Output Impedance Mismatch	Baseband frequency = 10 MHz		±0.3		%
Group Delay Variation					
Wideband Mode	Baseband frequency ≤ 210 MHz		0.25		ns
	Baseband frequency ≤ 250 MHz		0.35		ns
Narrow-Band Mode	Baseband frequency ≤ 33.2 MHz		0.2		ns
LO to IQ Leakage	1× LO		−40		dBm
	2× LO		−60		dBm
	4× LO		−60		dBm
RF to IQ Leakage	Relative to IQ output level		−40		dBc
MONITOR OUTPUT	LOMON and pins				
Nominal Output Power			−24		dBm
LOGIC INPUTS	SDI/SDA, CLK/SCL, CS pins				
Input High Voltage, V_{INH}	CS	1.4			V
Input Low Voltage, V_{INL}	CS			0.6	V
Input High Voltage, V_{INH}	SDI/SDA, CLK/SCL	2.1			V
Input Low Voltage, V_{INL}	SDI/SDA, CLK/SCL			1.1	V
Input Current, I_{INH}/I_{INL}	CS, SDI/SDA, CLK/SCL			±1	µA
Input Capacitance, C_{IN}	CS, SDI/SDA, CLK/SCL			10	pF
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	SDO, LDET pins; I_{OH} = 500 µA	2.8			V
Output Low Voltage, V_{OL}	SDO, LDET pins; I_{OL} = 500 µA			0.4	V
	SDA (SDI/SDA) pins; I_{OL} = 3 mA			0.4	V
POWER SUPPLIES	VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7, VCC8, and VCC9 pins				
Voltage Range		3.15	3.3	3.45	V
Supply Current			350	440	mA
Operating Temperature		−40		+85	°C

[1] Difference between channel gain and linear fit to channel gain.

TIMING CHARACTERISTICS

SPECIFICATIONS

I²C Interface Timing

Table 2.

Parameter[1]	Symbol	Limit	Unit
SCL Clock Frequency	f_{SCL}	400	kHz max
SCL Pulse Width High	t_{HIGH}	600	ns min
SCL Pulse Width Low	t_{LOW}	1300	ns min
Start Condition Hold Time	$t_{HD;STA}$	600	ns min
Start Condition Setup Time	$t_{SU;STA}$	600	ns min
Data Setup Time	$t_{SU;DAT}$	100	ns min
Data Hold Time	$t_{HD;DAT}$	300	ns min
Stop Condition Setup Time	$t_{SU;STO}$	600	ns min
Data Valid Time	$t_{VD;DAT}$	900	ns max
Data Valid Acknowledge Time	$t_{VD;ACK}$	900	ns max
Bus Free Time	t_{BUF}	1300	ns min

[1] See Figure 2.

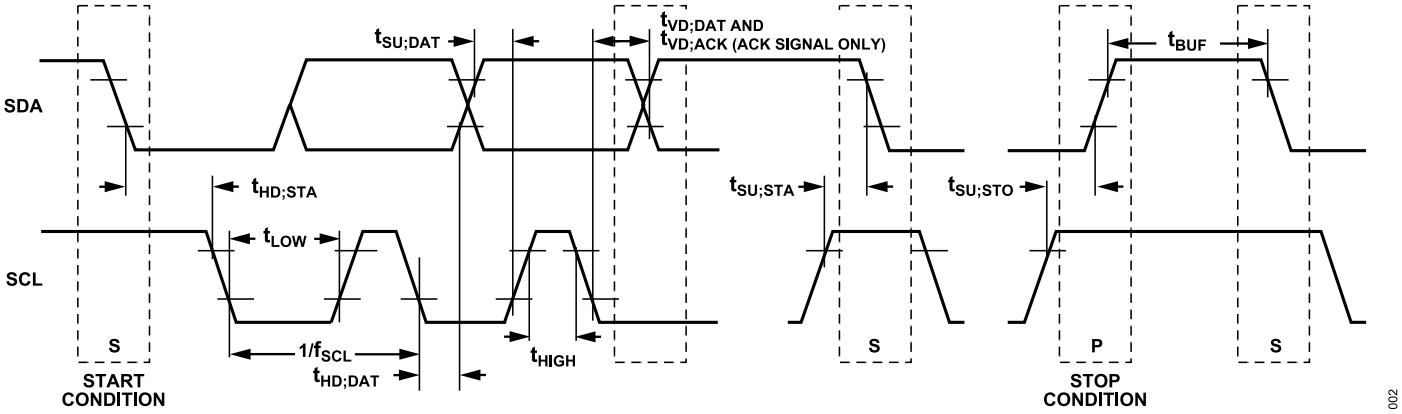

Figure 2. I²C Port Timing Diagram

SPECIFICATIONS

SPI Interface Timing

Table 3.

Parameter[1]	Symbol	Limit	Unit
CLK Frequency	f_{CLK}	20	MHz max
CLK Pulse Width High	t_1	15	ns min
CLK Pulse Width Low	t_2	15	ns min
Start Condition Hold Time	t_3	5	ns min
Data Setup Time	t_4	10	ns min
Data Hold Time	t_5	5	ns min
Stop Condition Setup Time	t_6	5	ns min
SDO Access Time	t_7	15	ns min
CS to SDO High Impedance	t_8	25	ns max

[1] See Figure 3.

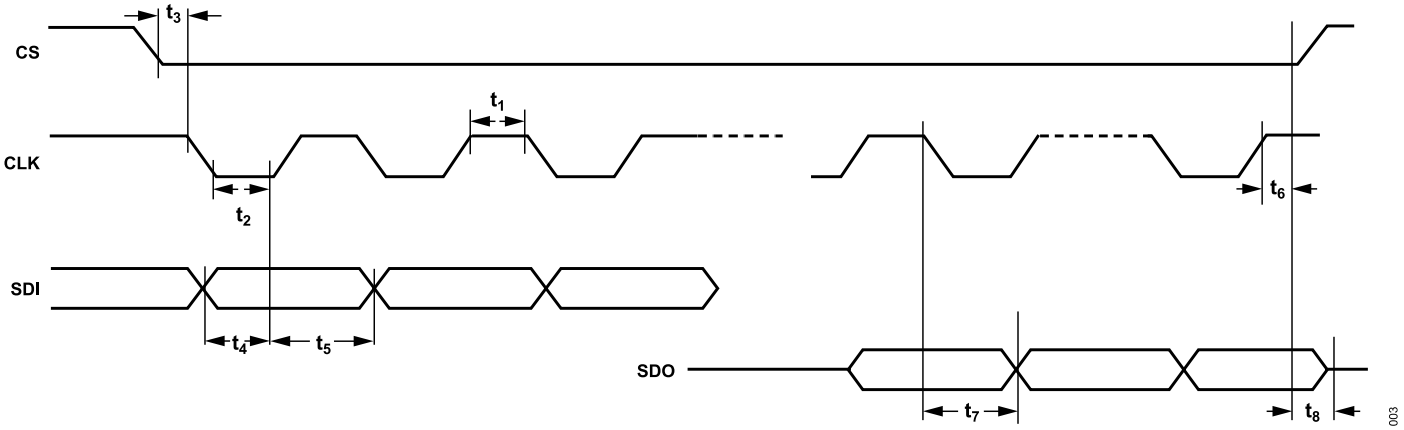

Figure 3. SPI Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage Pins (VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7, VCC8, VCC9)	−0.3 V to +4.0 V
Analog Input/Output	−0.3 V to +4.0 V
Digital Input/Output	−0.3 V to +4.0 V
RFI, $\overline{RFI}$, RFCM	0 V to 3.0 V
θ_{JA} (Exposed Paddle Soldered Down)	26°C/W
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

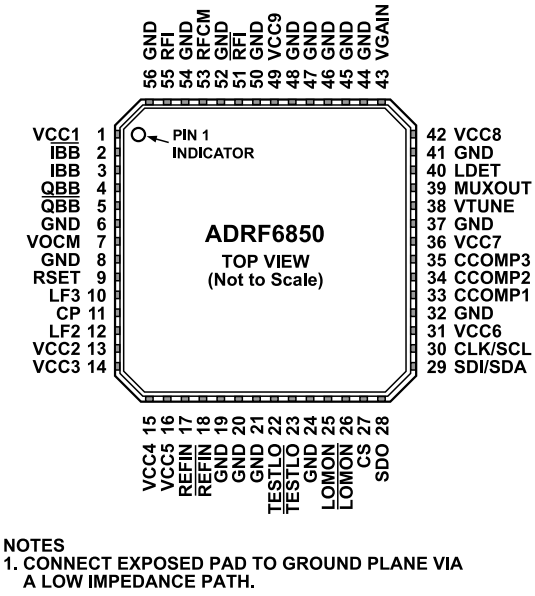

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 13, 14, 15, 16, 31, 36, 42, 49	VCC1 to VCC9	Positive Power Supplies. Apply a 3.3 V power supply to all VCCx pins. Decouple each pin with a power supply decoupling capacitor.
6, 8, 19, 20, 21, 24, 32, 37, 41, 44, 45, 46, 47, 48, 50, 52, 54, 56	GND	Analog Ground. Connect to a low impedance ground plane.
2, 3, 4, 5	$\overline{\text{IBB}}$, IBB, QBB, $\overline{\text{QBB}}$	Differential In-Phase and Quadrature Baseband Outputs. These low impedance outputs can drive 2.5 V p-p into 100 Ω differential loads.
7	VOCM	Baseband Common-Mode Voltage Input. When ac coupling the baseband output pins, ground VOCM. There is an option to apply an external voltage, which may be relevant when dc coupling the baseband output pins. Note that Register CR29, Bit 6 must be set accordingly.
33	CCOMP1	Internal Compensation Node. This pin must be decoupled to ground with a 100 nF capacitor.
34	CCOMP2	Internal Compensation Node. This pin must be decoupled to ground with a 100 nF capacitor.
35	CCOMP3	Internal Compensation Node. This pin must be decoupled to ground with a 100 nF capacitor.
38	VTUNE	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP output voltage.
9	RSET	Charge Pump Current Set. Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is $I_{CPmax} = \frac{23.5}{R_{SET}}$ where R_{SET} = 4.7 kΩ and $I_{CP\,max}$ = 5 mA.
11	CP	Charge Pump Output. When enabled, this provides ±I_{CP} to the external loop filter, which in turn, drives the internal VCO.
27	CS	Chip Select. CMOS input. When CS is high, the data stored in the shift registers is loaded into one of the 31 registers. In I^2C mode, when CS is high, the slave address of the device is 0x78, and when CS is low, the slave address is 0x58.
29	SDI/SDA	Serial Data Input for SPI Port, Serial Data Input/Output for I^2C Port. In SPI mode. This input is a high impedance CMOS data input, and data is loaded in an 8-bit word. In I^2C mode, this pin is a bidirectional port.
30	CLK/SCL	Serial Clock Input for SPI/I^2C Port. This serial clock is used to clock in the serial data to the registers. This input is a high impedance CMOS input.
28	SDO	Serial Data Output for SPI Port. Register states can be read back on the SDO data output line in an 8-bit word.
17	REFIN	Reference Input. AC couple this high impedance CMOS input.
18	$\overline{\text{REFIN}}$	Reference Input Bar. Ground this pin.
51, 55	$\overline{\text{RFI}}$, RFI	RF Inputs. 50 Ω internally biased RF inputs. For single-ended operation, RFI must be ac-coupled to the source, and $\overline{\text{RFI}}$ must be ac-coupled to the ground plane.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
53	RFCM	RF Input Common Mode. Connect to $\overline{\text{RFI}}$ when driving the input in single-ended mode. When driving the input differentially using a balun, connect this pin to the common terminal of the output coil of the balun. Decouple RFCM to the ground plane.
25, 26	LOMON, $\overline{\text{LOMON}}$	Differential Monitor Outputs. These pins provide a replica of the internal local oscillator frequency (1× LO) at four different power levels: −6 dBm, −12 dBm, −18 dBm, and −24 dBm, approximately. These open-collector outputs must be terminated with external resistors to VCCx. These outputs can be disabled through serial port programming and should be connected to VCCx if not used.
10, 12	LF3/LF2	Extra Loop Filter Pins for Fastlock. Use these pins to reduce lock time.
40	LDET	Lock Detect. This pin provides an active high output when the PLL frequency is locked. The lock detect timing is controlled by Register CR14 (Bit 7) and Register CR23 (Bit 3).
39	MUXOUT	Muxout. This output is a test output for diagnostic use only. Allow this pin to remain open circuit.
22, 23	TESTLO, $\overline{\text{TESTLO}}$	Differential Test Inputs. For internal use only. These pins should be grounded.
43	VGAIN	VGA Gain Input. Drive this pin by a voltage in the range from 0 V to 1.5 V. This voltage controls the gain of the VGA. A 0 V input sets the VGA gain to 0 dB, whereas a 1.5 V input sets the VGA gain to +60 dB if the VGA Gain Mode Polarity Bit CR30, Bit 2, is set to 0. If the VGA gain mode polarity bit is set to 1, a 0 V input sets the VGA gain to +60 dB, whereas a 1.5 V input sets the VGA gain to 0 dB.
	EP	Exposed Paddle. Connect the exposed pad to the ground plane via a low impedance path.

TYPICAL PERFORMANCE CHARACTERISTICS

A nominal condition is defined as 25°C, 3.30 V, and worst-case frequency. A worst-case condition is defined as having the worst-case temperature, supply voltage, and frequency.

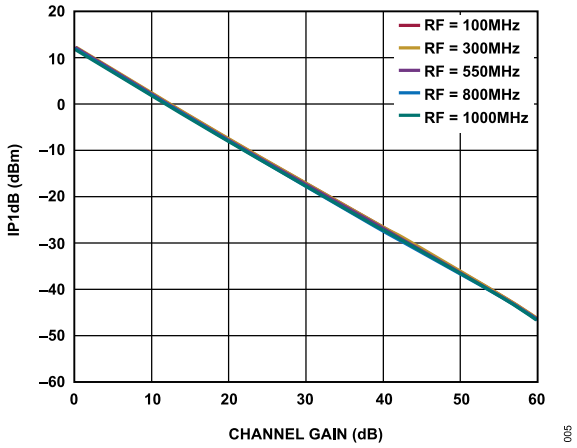

Figure 5. Input 1dB Compression Point (IP1dB) vs. Channel Gain, and RF Input Frequency, Nominal Conditions, Narrow-Band Mode

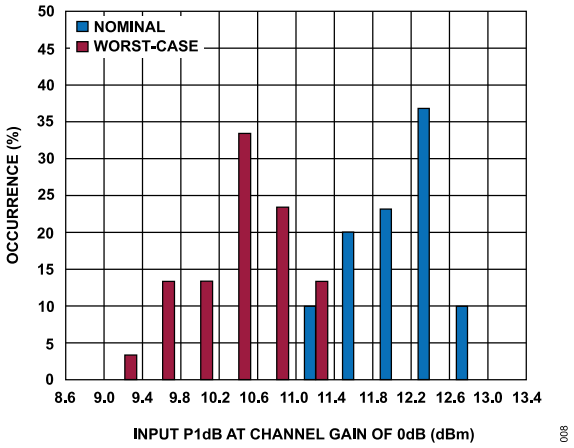

Figure 8. Input 1dB Compression Point (IP1dB) Distribution with Channel Gain = 0 dB at Nominal and Worst-Case Conditions

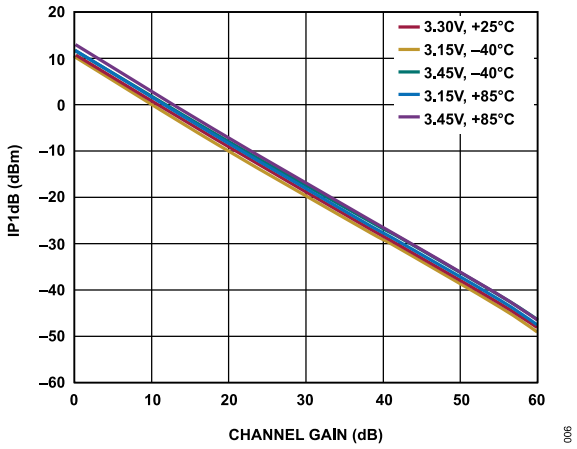

Figure 6. Input 1dB Compression Point (IP1dB) vs. Channel Gain, Supply, and Temperature, RF Input Frequency = 100 MHz, Narrow-Band Mode

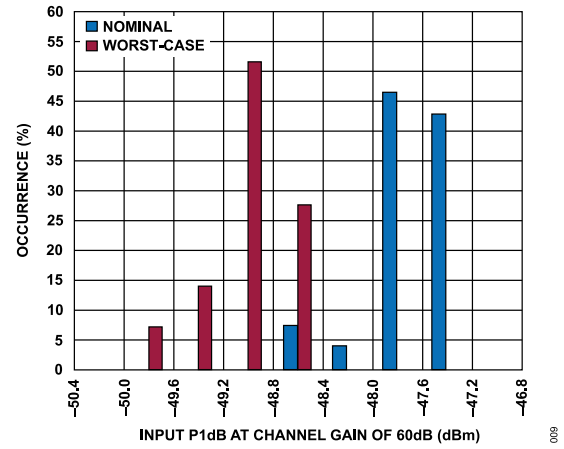

Figure 9. Input 1dB Compression Point (IP1dB) Distribution with Channel Gain = 60 dB at Nominal and Worst-Case Conditions

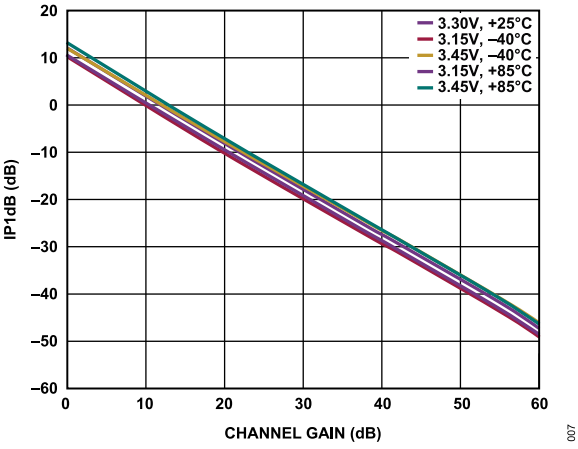

Figure 7. Input 1dB Compression Point (IP1dB) vs. Channel Gain, Supply, and Temperature, RF Input Frequency = 1000 MHz, Narrow-Band Mode

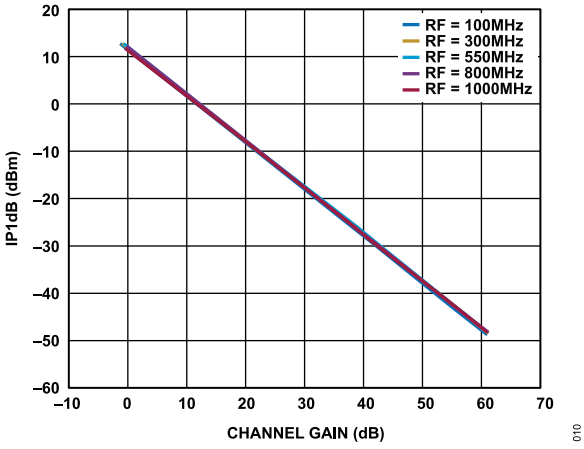

Figure 10. Input 1dB Compression Point (IP1dB) vs. Channel Gain, and RF Input Frequency, V_{OCM} = 1.2 V, Nominal Conditions, Narrow-Band Mode

TYPICAL PERFORMANCE CHARACTERISTICS

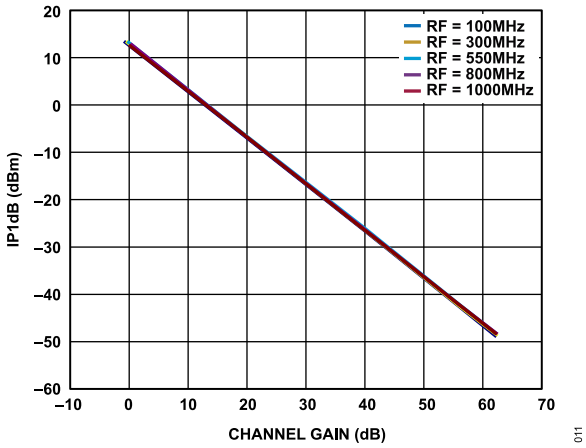

Figure 11. Input 1dB Compression Point (IP1dB) vs. Channel Gain, and RF Input Frequency, V_{OCM} = 1.6 V, Nominal Conditions, Narrow-Band Mode

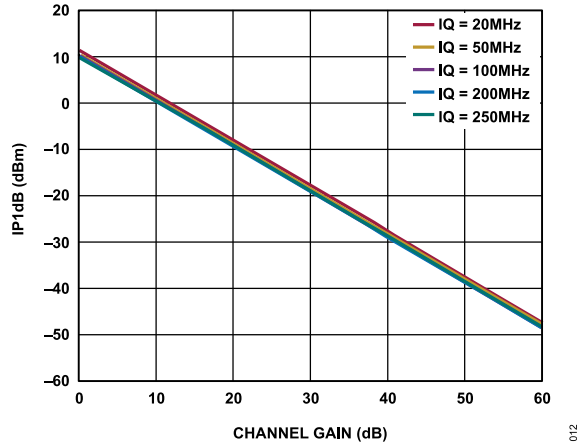

Figure 12. Input 1dB Compression Point (IP1dB) vs. Channel Gain, and IQ Output Frequency, LO = 1000 MHz, Nominal Conditions, Wideband Mode

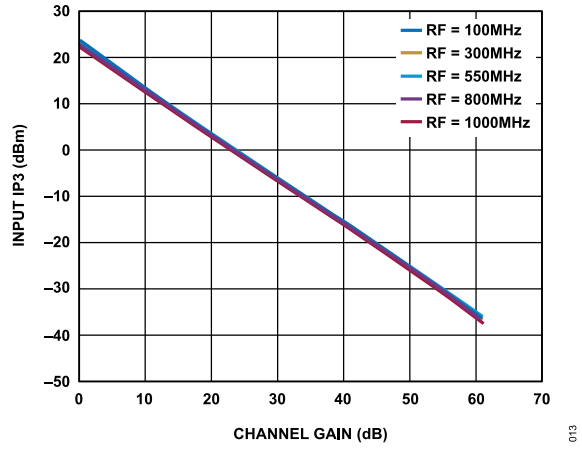

Figure 13. Input IP3 vs. Channel Gain, and RF Input Frequency, Nominal Conditions

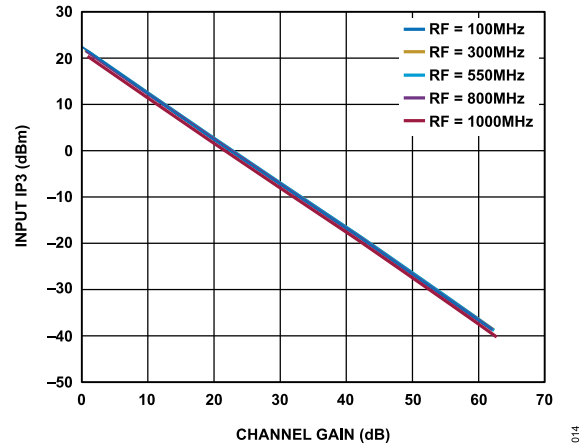

Figure 14. Input IP3 vs. Channel Gain, and RF Input Frequency, Worst-Case Conditions

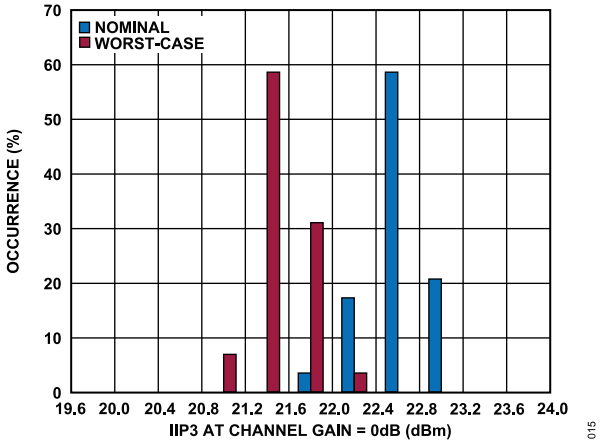

Figure 15. Input IP3 Distribution with Channel Gain = 0 dB at Nominal and Worst-Case Conditions

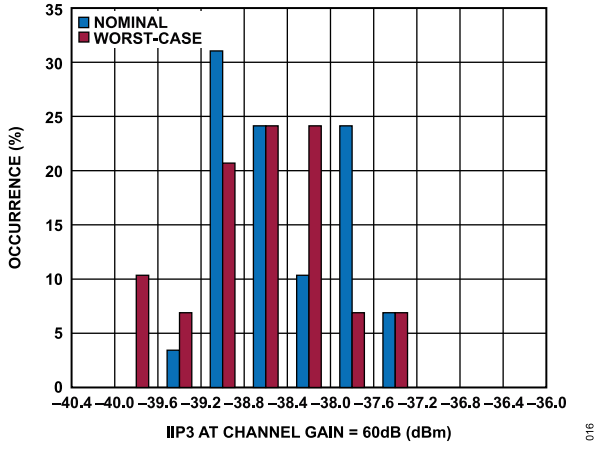

Figure 16. Input IP3 Distribution with Channel Gain = 60 dB at Nominal and Worst-Case Conditions

TYPICAL PERFORMANCE CHARACTERISTICS

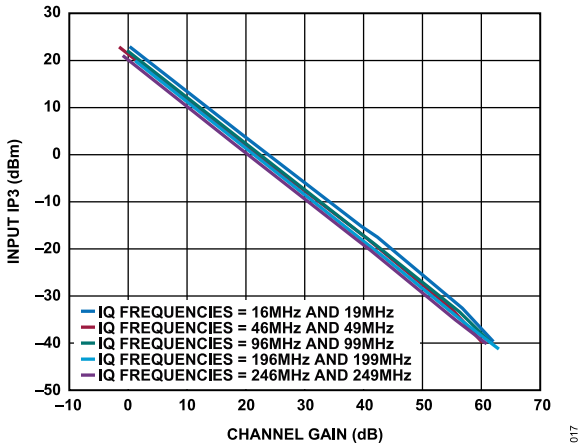

Figure 17. Input IP3 vs. Channel Gain, and IQ Output Frequency, Wideband Mode, Nominal Conditions

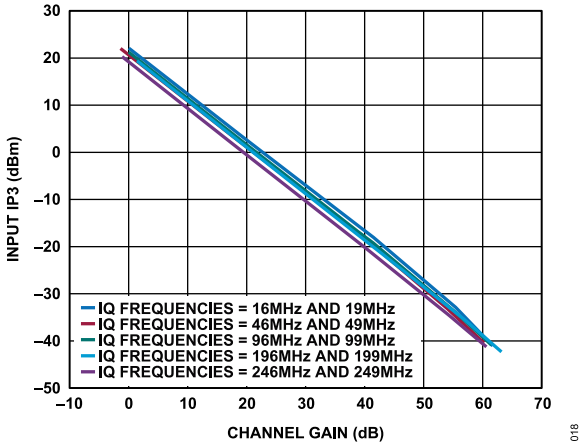

Figure 18. Input IP3 vs. Channel Gain, and IQ Output Frequency, Wideband Mode, Worst-Case Conditions

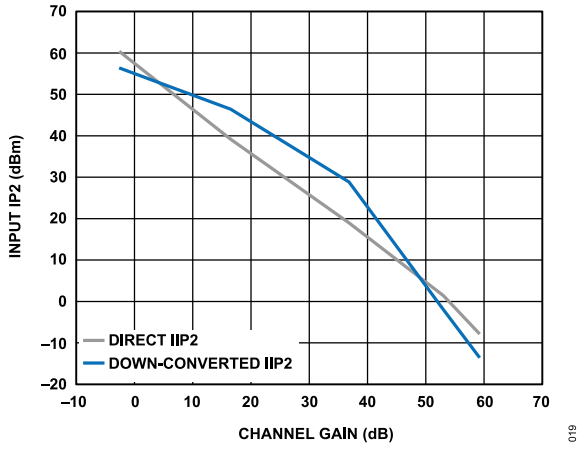

Figure 19. Input IP2 vs. Channel Gain, Wideband Mode, Nominal Conditions

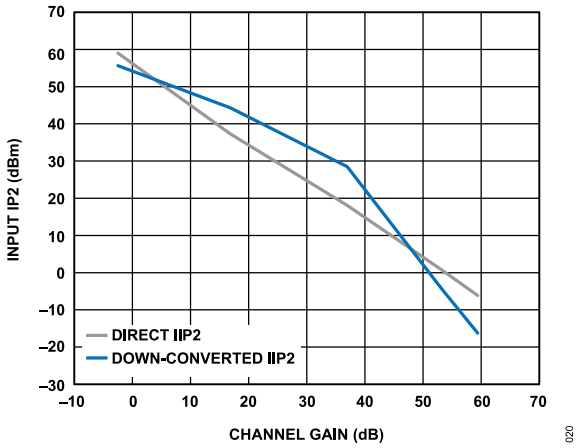

Figure 20. Input IP2 vs. Channel Gain, Wideband Mode, Worst-Case Conditions

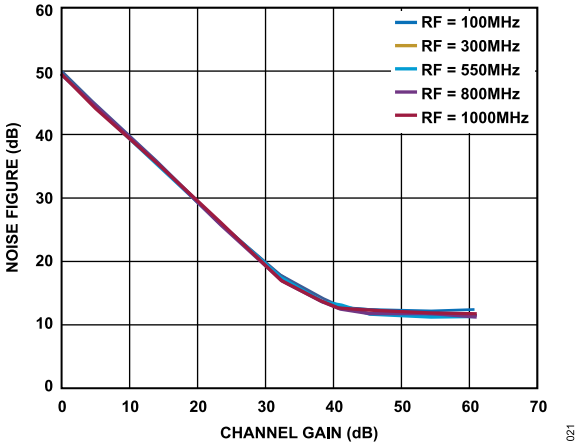

Figure 21. Noise Figure vs. Channel Gain, and RF Input Frequency, Narrow-Band Mode, Nominal Conditions

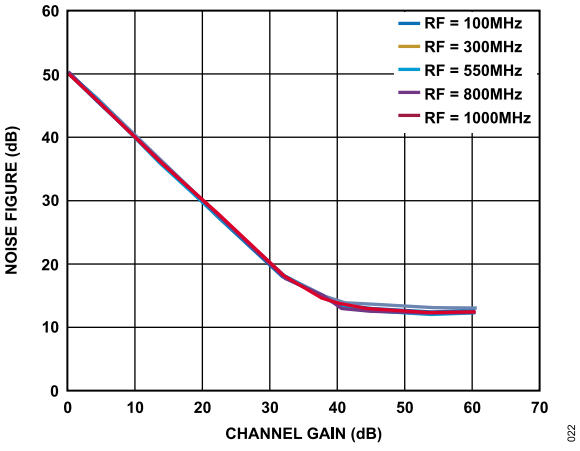

Figure 22. Noise Figure vs. Channel Gain, and RF Input Frequency, Narrow-Band Mode, Worst-Case Conditions

TYPICAL PERFORMANCE CHARACTERISTICS

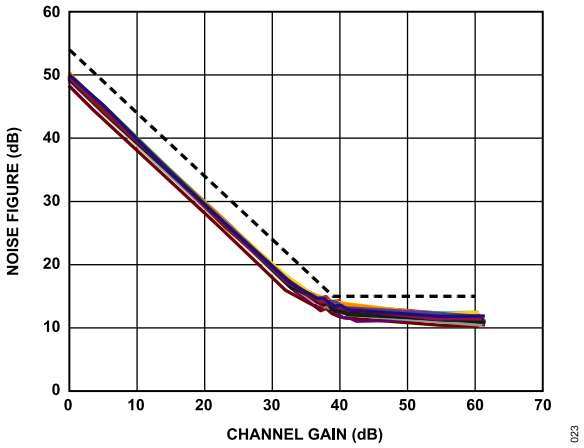

Figure 23. Noise Figure Distribution vs. Channel Gain, Narrow-Band Mode, Nominal Conditions

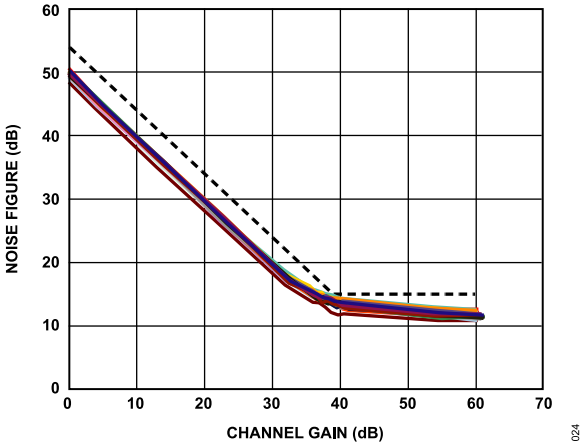

Figure 24. Noise Figure Distribution vs. Channel Gain, Narrow-Band Mode, Worst-Case Conditions

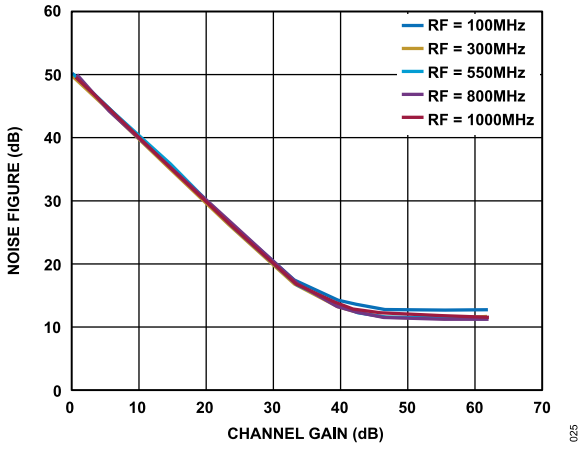

Figure 25. Noise Figure vs. Channel Gain, and RF Input Frequency, Wideband Mode, Nominal Conditions

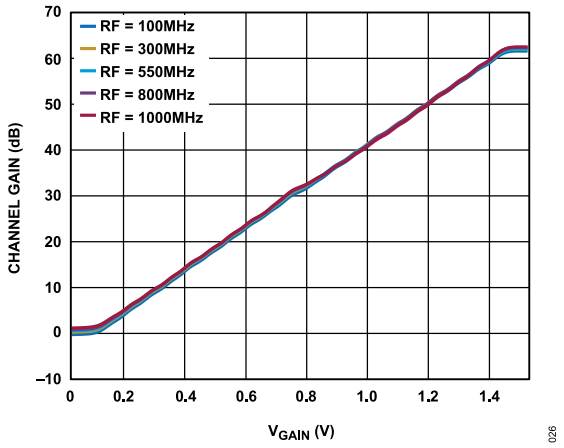

Figure 26. Channel Gain vs. V_{GAIN} and RF Input Frequency, Nominal Conditions

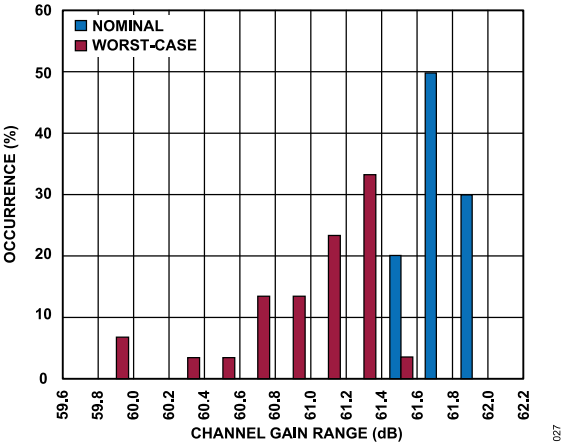

Figure 27. Channel Gain Range Distribution at Nominal and Worst-Case Conditions

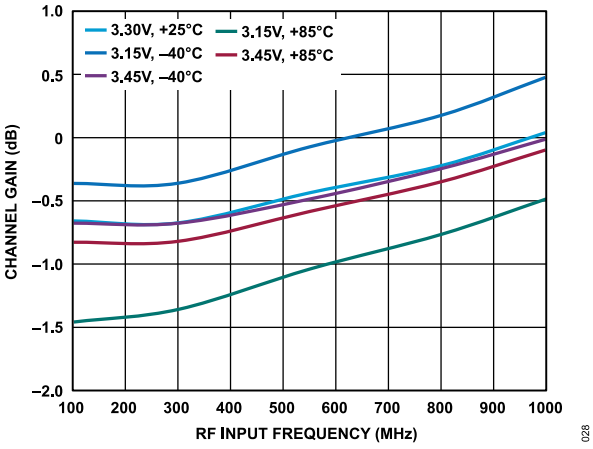

Figure 28. Minimum Channel Gain vs. RF Input Frequency, Supply, and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

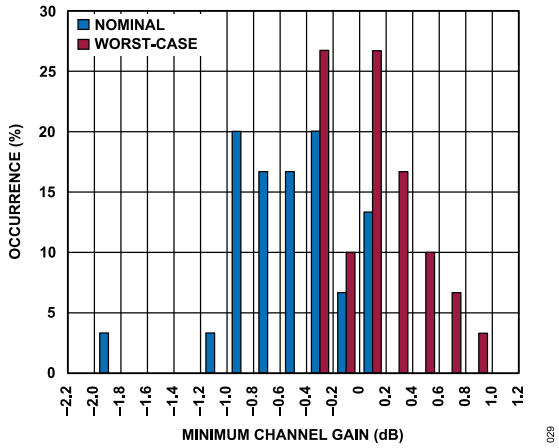

Figure 29. Minimum Channel Gain Distribution at Nominal and Worst-Case Conditions

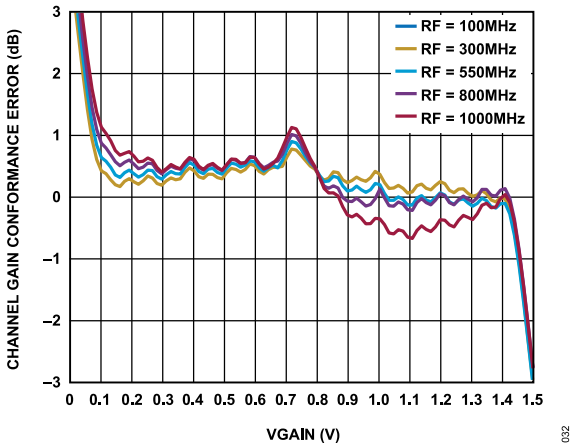

Figure 32. Channel Gain Conformance Error vs. V_{GAIN} and RF Input Frequency, Nominal Conditions

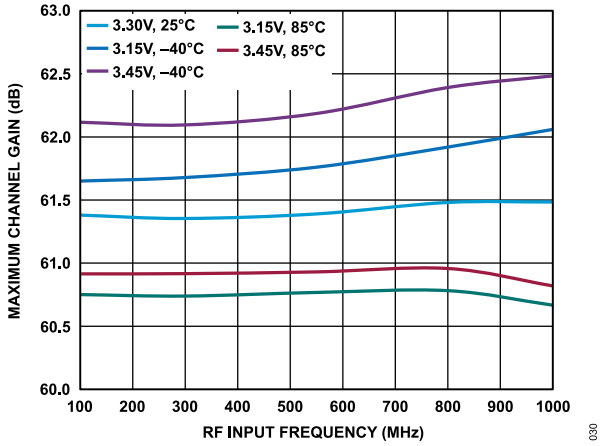

Figure 30. Maximum Channel Gain vs. RF Input Frequency, Supply, and Temperature

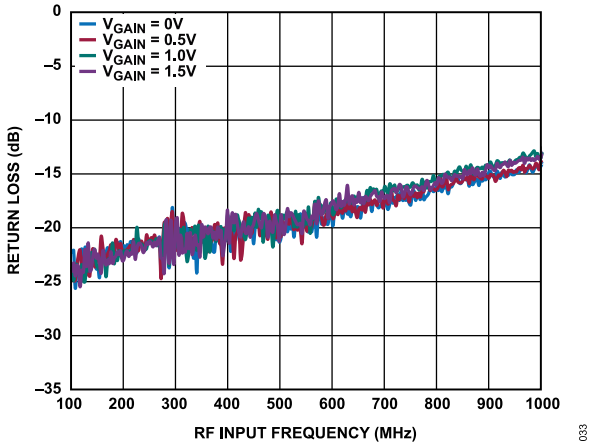

Figure 33. Input Return Loss vs. RF Input Frequency and Channel Gain, Nominal Conditions

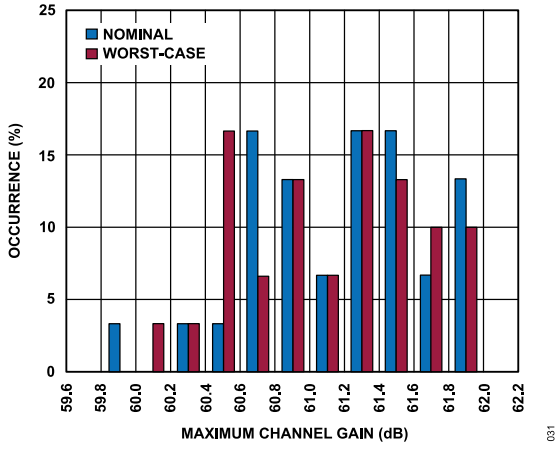

Figure 31. Maximum Channel Gain Distribution at Nominal and Worst-Case Conditions

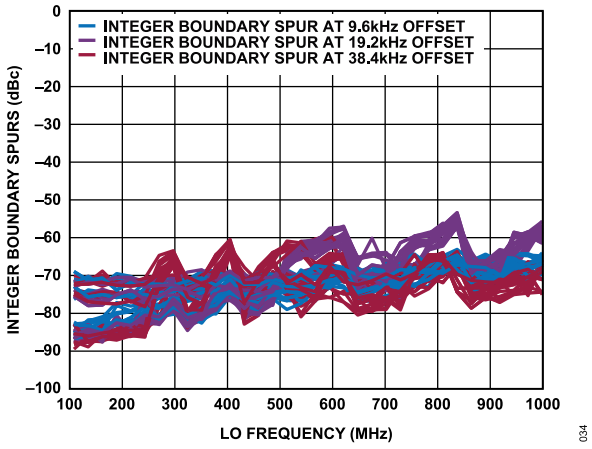

Figure 34. Integer Boundary Spurs vs. LO Frequency, Channel Gain, Supply, and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

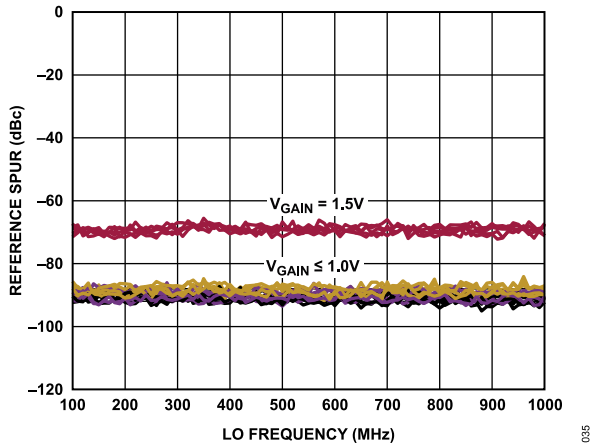

Figure 35. Reference Spurs at 13.5 MHz from Carrier vs. LO Frequency, Channel Gain, Supply, and Temperature

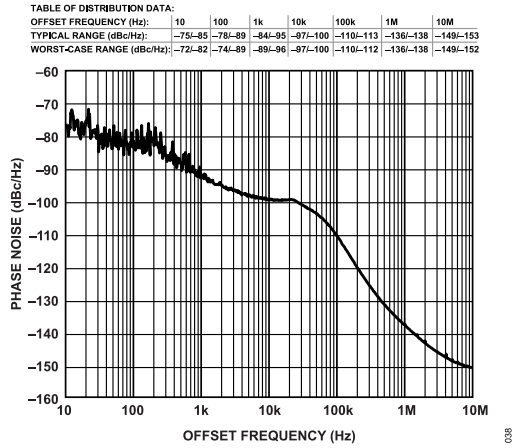

Figure 38. Phase Noise Performance Including Distribution Table at LO Frequency = 1000 MHz at Nominal and Worst-Case Conditions

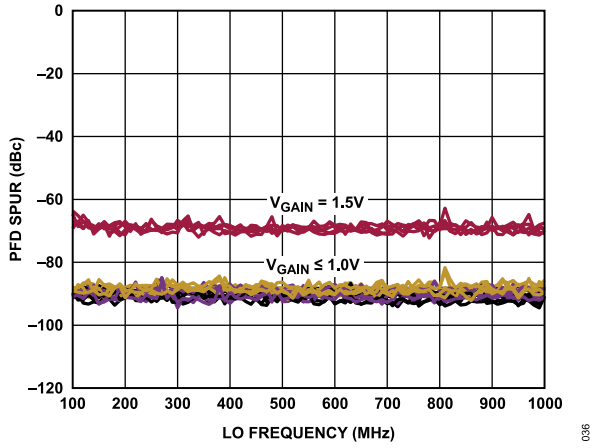

Figure 36. PFD Spurs at 27 MHz from Carrier vs. LO Frequency, Channel Gain, Supply, and Temperature

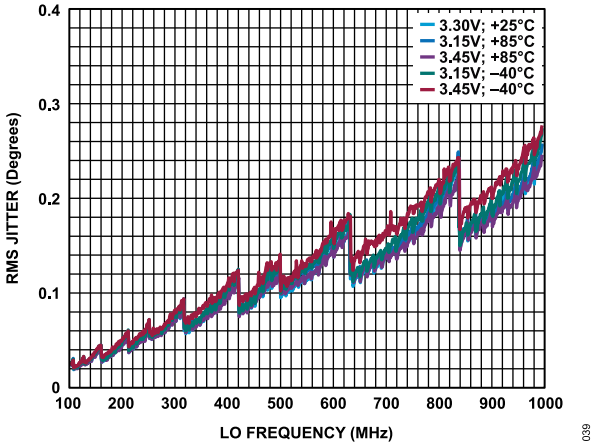

Figure 39. Integrated Phase Noise vs. LO Frequency, Supply, and Temperature

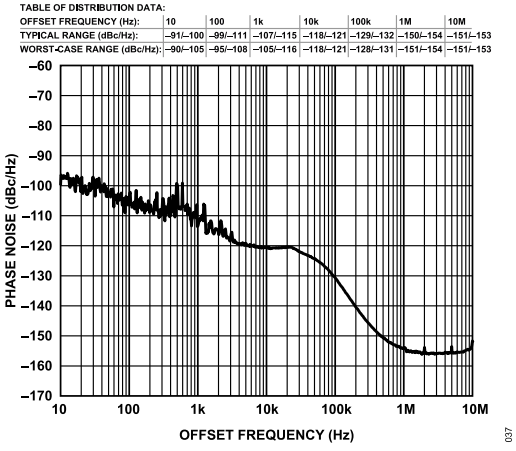

Figure 37. Phase Noise Performance Including Distribution Table at LO Frequency = 100 MHz at Nominal and Worst-Case Conditions

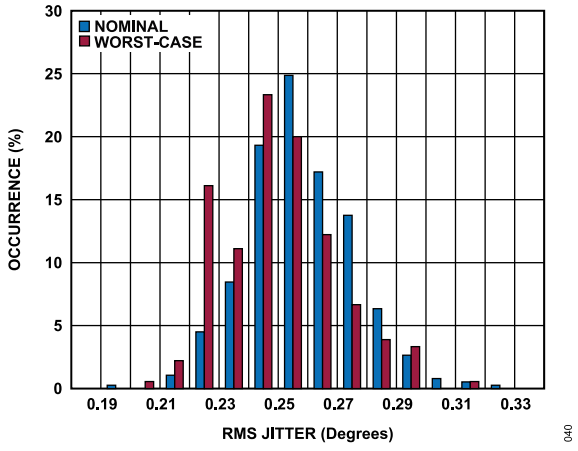

Figure 40. Integrated Phase Noise Distribution with LO Frequency = 1000 MHz at Nominal and Worst-Case Conditions

TYPICAL PERFORMANCE CHARACTERISTICS

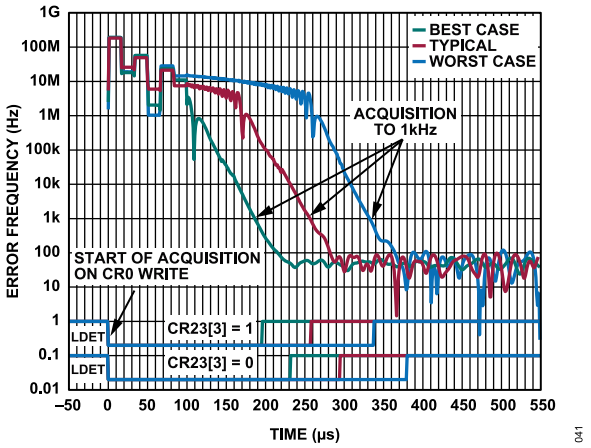

Figure 41. PLL Frequency Settling Time with Typical, Best-Case, and Worst-Case Frequency Hop with Lock Detect Shown, Nominal Conditions

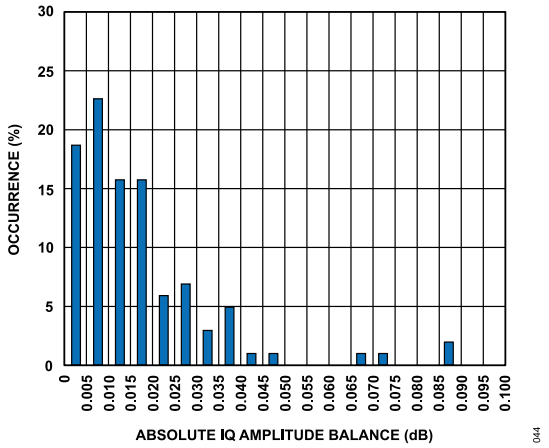

Figure 44. Absolute IQ Amplitude Balance, Narrow-Band Mode, Nominal Conditions

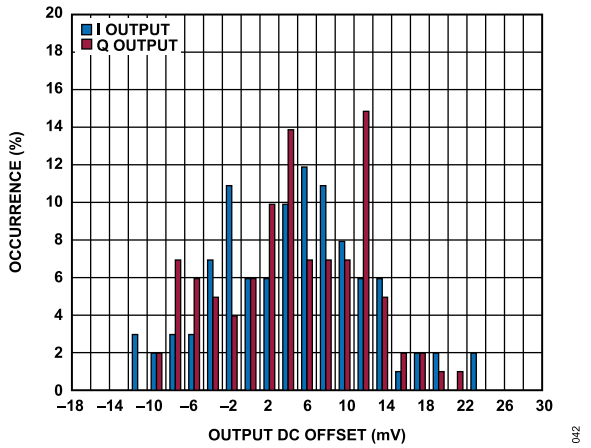

Figure 42. Output DC Offset Distribution for I and Q Outputs, Nominal Conditions

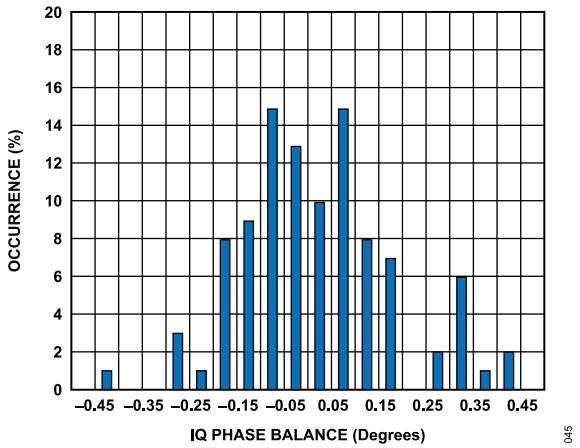

Figure 45. IQ Phase Balance, Narrow-Band Mode, Nominal Conditions

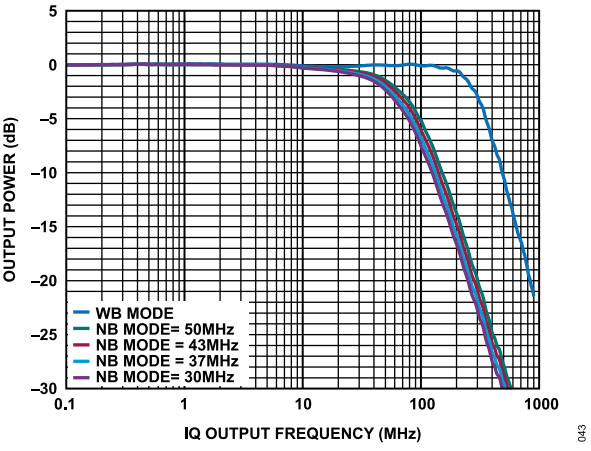

Figure 43. Normalized IQ Output Bandwidth, Narrow-Band, and Wideband Modes, Nominal Conditions

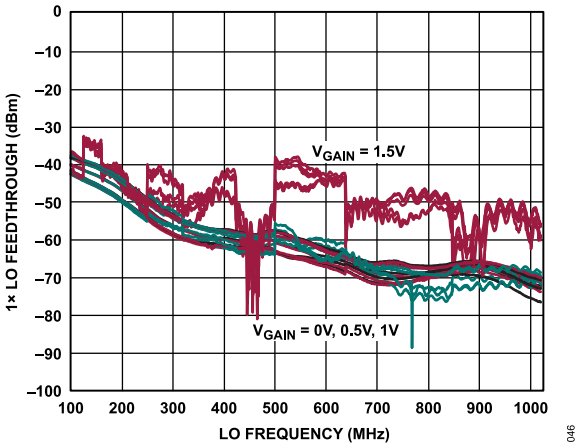

Figure 46. 1× LO Feedthrough vs. LO Frequency, V_{GAIN}, Supply, and Temperature (Narrow-Band Mode)

TYPICAL PERFORMANCE CHARACTERISTICS

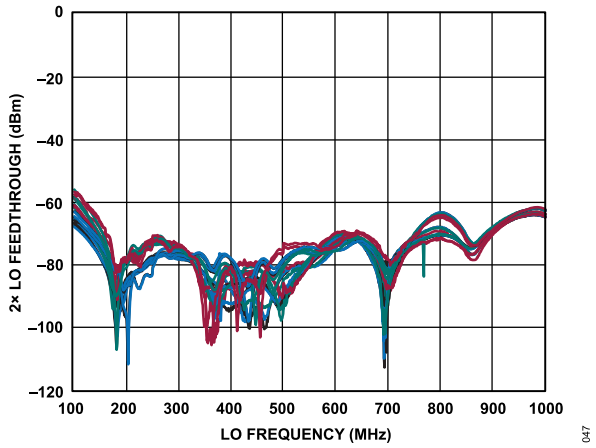

Figure 47. 2× LO Feedthrough vs. LO Frequency, V_{GAIN}, Supply, and Temperature (Narrow-Band Mode)

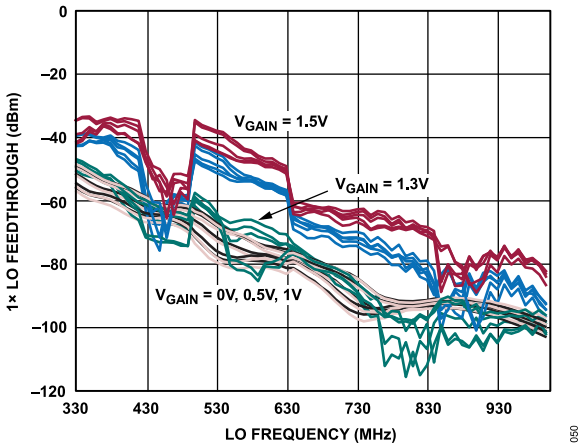

Figure 50. 1× LO Feedthrough vs. LO Frequency, V_{GAIN}, Supply, and Temperature, Fourth-Order Filter at 300 MHz Applied, Wideband Mode

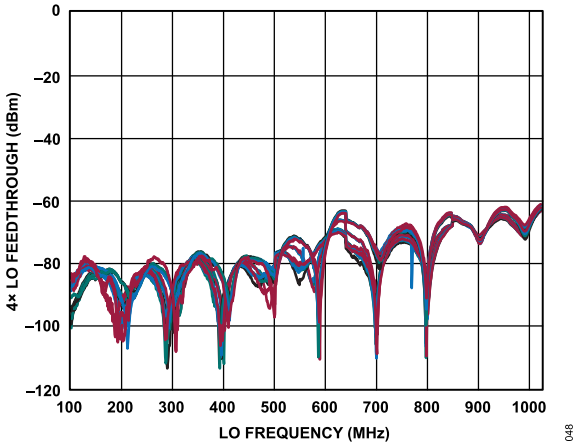

Figure 48. 4× LO Feedthrough vs. LO Frequency, V_{GAIN}, Supply, and Temperature (Narrow-Band Mode)

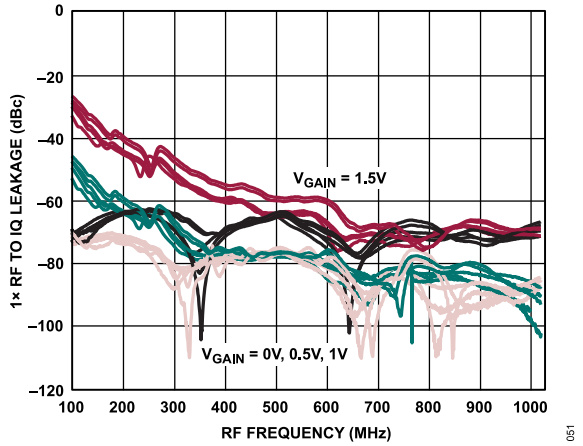

Figure 51. 1× RF Feedthrough vs. RF Input Frequency, V_{GAIN}, Supply, and Temperature, Narrow-Band Mode

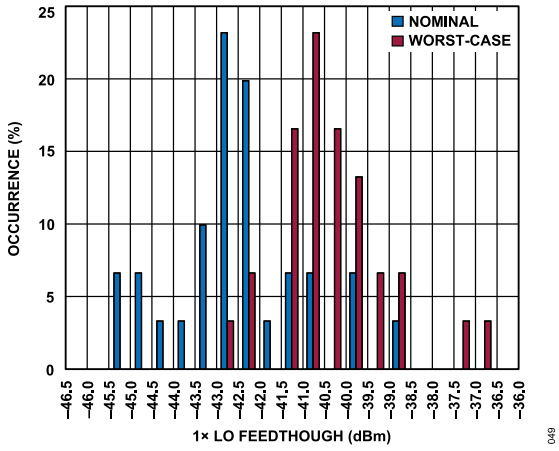

Figure 49. 1× LO Feedthrough Distribution at Nominal and Worst-Case Conditions with LO Frequency > 300 MHz, Narrow-Band Mode

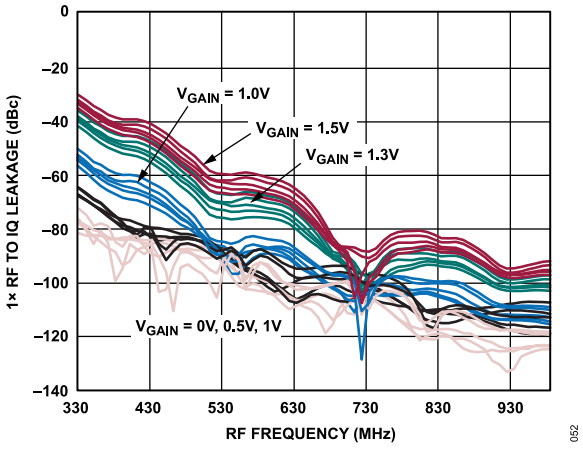

Figure 52. 1× RF Feedthrough vs. RF Input Frequency, V_{GAIN}, Supply, and Temperature, Fourth-Order Filter at 300 MHz Applied, Wideband Mode

THEORY OF OPERATION

OVERVIEW

The ADRF6850 device can be separated into the following basic building blocks:

- PLL synthesizer and VCO
- Quadrature demodulator
- Variable gain amplifier (VGA)
- I^2C/SPI interface

Each of these building blocks is described in detail in the sections that follow.

PLL SYNTHESIZER AND VCO

Overview

The phase-locked loop (PLL) consists of a fractional-N frequency synthesizer with a 25-bit fixed modulus, allowing a frequency resolution of less than 1 Hz over the entire frequency range. It also has an integrated voltage controlled oscillator (VCO) with a fundamental output frequency ranging from 2000 MHz to 4000 MHz. An RF divider, controlled by Register CR28, Bits[2:0], extends the lower limit of the frequency range to less than 400 MHz. This 400 MHz to 4000 MHz frequency output is then applied to a divide-by-4 quadrature circuit to provide a local oscillator (LO) ranging from 100 MHz to 1000 MHz to the quadrature demodulator.

Reference Input Section

The reference input stage is shown in Figure 53. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed, and SW1 and SW2 are open. This ensures that there is no loading of the REFIN pin at power-down.

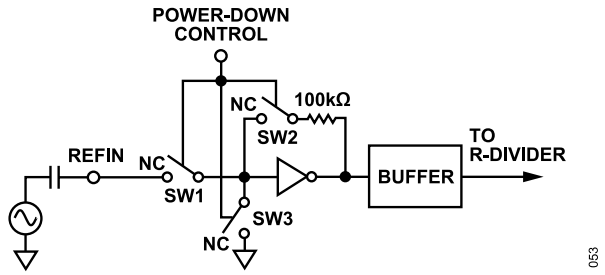

Figure 53. Reference Input Stage

Reference Input Path

The on-chip reference frequency doubler allows the input frequency of the reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves the in-band phase noise performance by 3 dBc/Hz.

The 5-bit R-divider allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

An additional divide-by-2 (÷2) function in the reference input path allows for a greater division range.

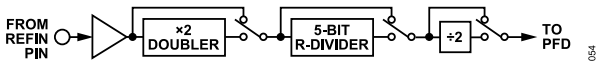

Figure 54. Reference Input Path

The PFD frequency equation is

$$f_{PFD} = f_{REFIN} \times [(1 + D)/(R \times (1 + T))] \quad (1)$$

where:
f_{REFIN} is the reference input frequency.
D is the doubler bit.
R is the programmed divide ratio of the binary 5-bit programmable reference divider (1 to 32).
T is the ÷2 bit (0 or 1).

RF Fractional-N Divider

The RF fractional-N divider allows a division ratio in the PLL feedback path that can range from 23 to 4095. The relationship between the fractional-N divider and the LO frequency is described in the following section.

INT and FRAC Relationship

The integer (INT) and fractional (FRAC) values make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD) frequency. See the Programming the Correct LO Frequency section for more information.

The LO frequency equation is

$$LO = f_{PFD} \times (INT + (FRAC/2^{25}))/2 \times 2^{RFDIV} \quad (2)$$

where:
LO is the local oscillator frequency.
f_{PFD} is the PFD frequency.
INT is the integer component of the required division factor and is controlled by the CR6 and CR7 registers.
$FRAC$ is the fractional component of the required division factor and is controlled by the CR0 to CR3 registers.
$RFDIV$ is the setting in Register CR28, Bits[2:0], and controls the setting of a divider at the output of the PLL.

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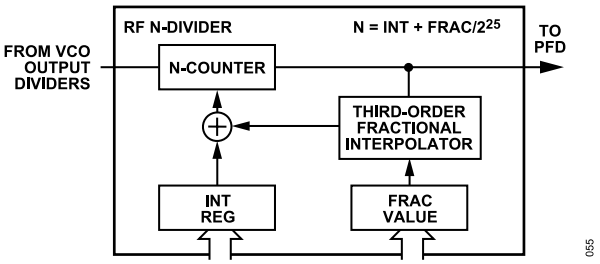

Figure 55. RF Fractional-N Divider

Phase Frequency Detector (PFD) and Charge Pump

The PFD takes inputs from the R-divider and the N-counter and produces an output proportional to the phase and frequency difference between them (see Figure 56 for a simplified schematic). The PFD includes a fixed delay element that sets the width of the antibacklash pulse, ensuring that there is no dead zone in the PFD transfer function.

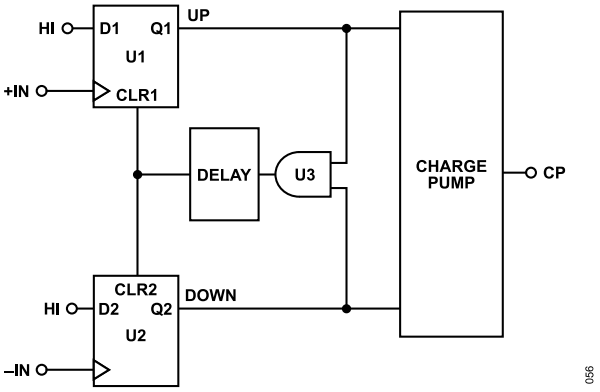

Figure 56. PFD Simplified Schematic

Lock Detect (LDET)

LDET (Pin 40) signals when the PLL has achieved lock to an error frequency of less than 1 kHz. On a write to Register CR0, a new PLL acquisition cycle starts, and the LDET signal goes low. When lock has been achieved, this signal returns high.

Voltage Controlled Oscillator (VCO)

The VCO core in the ADRF6850 consists of three separate VCOs, each with 16 overlapping bands. This configuration of 48 bands allows the VCO frequency range to extend from 2000 MHz to 4000 MHz. The three VCOs are divided externally by a programmable divider (RFDIV controlled by Register CR28, Bits[2:0]). This divider provides divisions of 1, 2, 4, and 8 to ensure that the frequency range is extended from 250 MHz (2000 MHz/8) to 4000 MHz (4000 MHz/1). A lower limit of only 400 MHz is required. A divide-by-4 quadrature circuit provides the full LO frequency range from 100 MHz to 1000 MHz. Figure 57 shows a sweep of V_{TUNE} vs. LO frequency demonstrating the three VCOs overlapping and the multiple overlapping bands within each VCO at the LO frequency range of 100 MHz to 1000 MHz. Note that this plot includes the RFDIV divider being incorporated to provide further divisions of the fundamental VCO frequency; thus, each VCO is used on four different occasions throughout the full LO frequency range. The choice of three 16-band VCOs and an RFDIV divider allows the wide frequency range to be covered without large VCO sensitivity (K_{VCO}) or resultant poor phase noise and spurious performance.

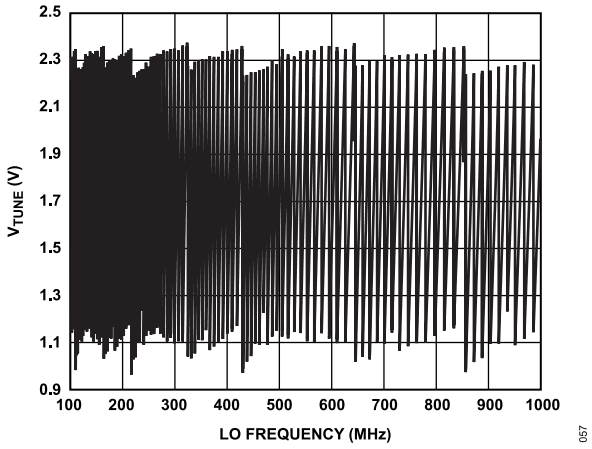

Figure 57. V_{TUNE} vs. LO Frequency

The correct VCO and band are chosen automatically by the VCO and band select circuitry when Register CR0 is updated. This is referred to as autocalibration. The autocalibration time is set by Register CR25.

$$Autocalibration\ Time = (BSCDIV \times 24)/PFD \quad (3)$$

where:
BSCDIV = Register CR25, Bits[7:0].
PFD = PFD frequency.

For a PFD frequency of 27 MHz, BSCDIV = 112 to set an autocalibration time of 100 µs.

Note that BSCDIV must be recalculated if the PFD frequency is changed. The recommended autocalibration setting is 100 µs. During this time, the VCO V_{TUNE} is disconnected from the output of the loop filter and is connected to an internal reference voltage. A typical frequency acquisition is shown in Figure 58.

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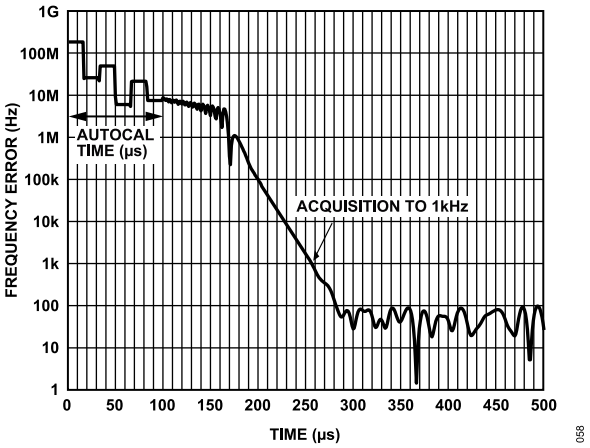

Figure 58. PLL Acquisition

After autocalibration, normal PLL action resumes, and the correct frequency is acquired to within a frequency error of 1 kHz in 260 µs typically. For a maximum cumulative step of 100 kHz, autocalibration can be turned off by Register CR24, Bit 0. This enables cumulative PLL acquisitions of 100 kHz or less to occur without the autocalibration procedure, which improves acquisition times significantly (see Figure 59).

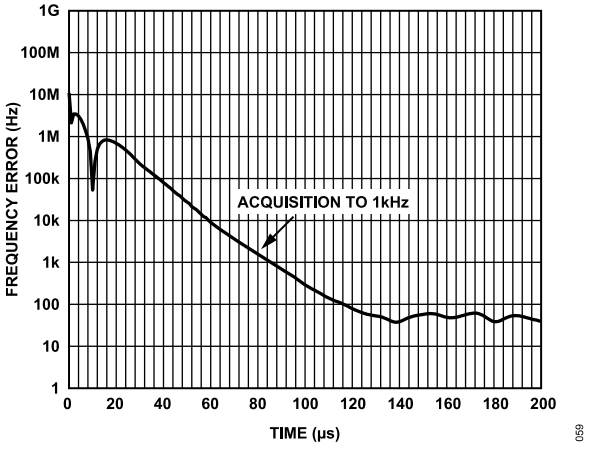

Figure 59. PLL Acquisition Without Autocalibration for a 100 kHz Step

The VCO displays a variation of K_{VCO} as V_{TUNE} varies within the band and from band to band. Figure 60 shows how the K_{VCO} varies across the fundamental LO frequency range from 500 MHz to 1000 MHz. Note that K_{VCO} is shown at the LO frequency rather than at the VCO frequency. Figure 60 is useful when calculating the loop filter bandwidth and individual loop filter components using ADISimPLL™. ADISimPLL is an Analog Devices, Inc., simulator that aids in PLL design, particularly with respect to the loop filter. It reports parameters such as phase noise, integrated phase noise, acquisition time, and so forth for a particular set of input conditions. ADISimPLL can be downloaded from www.analog.com.

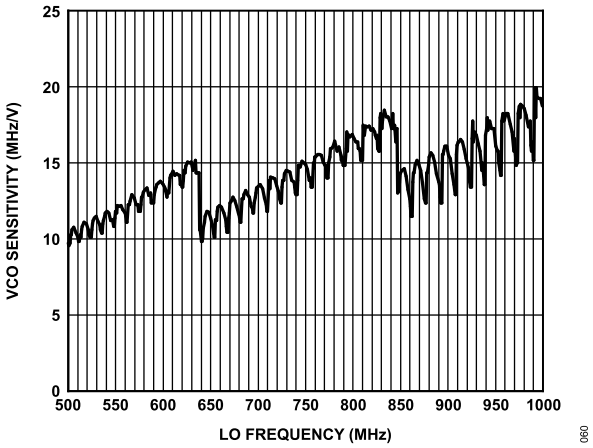

Figure 60. K_{VCO} vs. LO Frequency

Programming the Correct LO Frequency

There are two steps to programming the correct LO frequency. The user can calculate the N-divider ratio that is required in the PLL and the RFDIV value based on the required LO frequency and PFD frequency.

1. Calculate the value of RFDIV, which is used to program Register CR28, Bits[2:0], from the following lookup table (Table 6). See also Table 24.

Table 6. RFDIV Lookup Table

LO Frequency (MHz)	RFDIV = Register CR28[2:0]
500 to 1000	000 = divide-by-1
250 to 500	001 = divide-by-2
125 to 250	010 = divide-by-4
100 to 125	011 = divide-by-8

2. Using the following equation, calculate the value of the N-divider:

$$N = (2^{RFDIV} \times 2 \times LO)/(f_{PFD}) \quad (4)$$

where:
N is the N-divider value.
RFDIV is the setting in Register CR28, Bits[2:0].
LO is the local oscillator frequency.
f_{PFD} is the PFD frequency.

This equation is a different representation of Equation 2.

Example to Program the Correct LO Frequency

Assume that the PFD frequency is 27 MHz and the required LO frequency is 330 MHz.

1. From Table 6, $2^{RFDIV} = 2$.
2. $N = (2 \times 2 \times 330E+6)/(27E+6) = 48.88888889$.

The N-divider value is composed of integer (INT) and fractional (FRAC) components according to the following equation:

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$$N = INT + FRAC/2^{25} \quad (5)$$

INT = 48 and FRAC = 29,826,162.

The appropriate registers must then be programmed according to the register map, ensuring that Register CR0 is the last register to be programmed because this write starts a new PLL acquisition cycle.

QUADRATURE DEMODULATOR

The quadrature demodulator can be powered up by Register CR29, Bit 0. It has an output filter with narrow-band and wideband modes, which are selected by Register CR29, Bit 3. Wideband mode has a 1 dB filter cutoff of 250 MHz. Narrow-band mode has selectable cutoff filters of 30 MHz through 50 MHz by pro-gramming Register CR29, Bits[5:4]. A dc bias voltage of 1.4 V (V_{OCM}) can be set internally by setting Register CR29, Bit 6 = 1. To select an external dc bias voltage, set Register CR29, Bit 6 = 0, and drive Pin 7, VOCM, with the requisite external bias voltage.

VARIABLE GAIN AMPLIFIER (VGA)

The variable gain amplifier (VGA) at the input to the demodulator can be driven either single-ended or differentially.

To drive single-ended, connect Pin 53, RFCM, to Pin 51, $\overline{RFI}$, and decouple both pins to ground with a 10 nF capacitor. Drive the input signal through Pin 55, RFI.

To drive differentially, use a balun with the RFI and $\overline{RFI}$ pins driven by the balanced outputs of the balun, and connect the RFCM pin to the common balun output terminal. Decouple RFCM to ground.

The VGA gain range is approximately 60 dB and is achieved by varying the VGAIN voltage from 0 V to 1.5 V. The Typical Performance Characteristics section has more information on the VGA gain performance. A 0 V input on VGAIN sets the VGA gain to 0 dB, whereas a 1.5 V input sets the VGA gain to +60 dB if the VGA Gain Mode Polarity Bit CR30, Bit 2, is set to 0. If the VGA gain mode polarity bit is set to 1, a 0 V input voltage on VGAIN sets the VGA gain to +60 dB, whereas a 1.5 V input sets the VGA gain to 0 dB.

The VGA can be powered down by setting Register CR30, Bit 0, to 0 and can be powered up by setting this same bit to 1.

I²C INTERFACE

The ADRF6850 supports a 2-wire, I²C-compatible serial bus that drives multiple peripherals. The part powers up in I²C mode but is not locked in this mode. To remain in I²C mode, it is recommended that the user tie the CS line to either 3.3 V or GND, thus disabling SPI mode.

The serial data (SDA) and serial clock (SCL) inputs carry information between any devices that are connected to the bus. Each slave device is recognized by a unique address. The ADRF6850 has two possible 7-bit slave addresses for both read and write operations, 0x78 and 0x58. The MSB of the 7-bit slave address is set to 1. Bit 5 of the slave address is set by the CS pin (Pin 27). Bits[4:0] of the slave address are set to 11000. The slave address consists of the seven MSBs of an 8-bit word. The LSB of the word sets either a read or a write operation (see Figure 61). Logic 1 corresponds to a read operation, whereas Logic 0 corresponds to a write operation.

To control the device on the bus, the following protocol must be followed:

1. The master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows.
2. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address and the R/W bit). The bits are transferred from MSB to LSB.
3. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit.
4. All other devices then withdraw from the bus and maintain an idle condition. During the idle condition, the device monitors the SDA and SCL lines waiting for the start condition and the correct transmitted address.
5. The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte indicates that the master writes information to the peripheral. Logic 1 on the LSB of the first byte indicates that the master reads information from the peripheral.

The ADRF6850 acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/W bit. The ADRF6850 has 34 subaddresses to enable the user-accessible internal registers; therefore, it interprets the first byte as the device address and the second byte as the starting subaddress.

Auto-increment mode is supported, which allows data to be read from or written to the starting subaddress, and each subsequent address, without manually addressing the subsequent subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all registers.

Stop and start conditions can be detected at any stage of the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. If an invalid subaddress is issued by the user, the ADRF6850 does not issue an acknowledge and returns to the idle condition. In a no acknowledge condition, the SDA line is not pulled low on the ninth pulse. See Figure 62 and Figure 63 for sample write and read data transfers, Figure 64 for the timing protocol, and Figure 2 for a more detailed timing diagram.

THEORY OF OPERATION

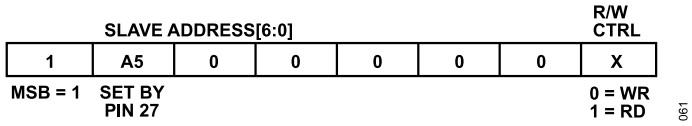


Figure 61. Slave Address Configuration

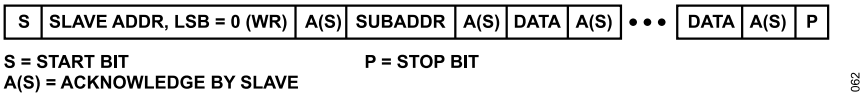


Figure 62. I²C Write Data Transfer

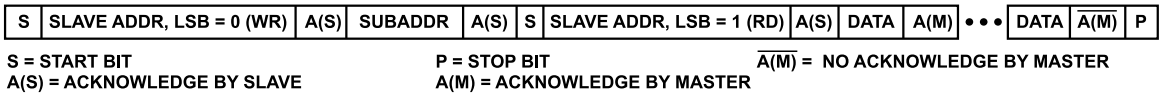


Figure 63. I²C Read Data Transfer

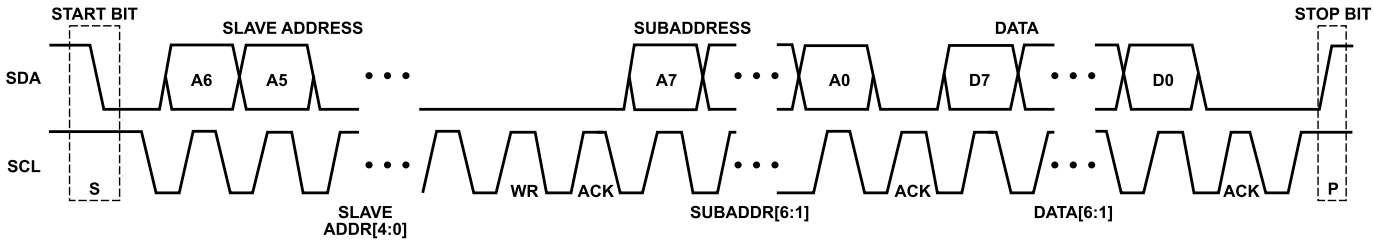


Figure 64. I²C Data Transfer Timing

THEORY OF OPERATION

SPI INTERFACE

The ADRF6850 supports the SPI protocol; however, the part powers up in I^2C mode. To select and lock the SPI mode, three pulses must be sent to the CS pin, as shown in Figure 65. When the SPI protocol is locked in, it cannot be unlocked while the device remains powered up. To reset the serial interface, the part must be powered down and powered up again.

Serial Interface Selection

The CS pin controls selection of the I^2C or SPI interface. Figure 65 shows the selection process that is required to lock in the SPI mode. To communicate with the part using the SPI protocol, three pulses must be sent to the CS pin. On the third rising edge, the part selects and locks the SPI protocol. Consistent with most SPI standards, the CS pin must be held low during all SPI communication to the part and held high at all other times.

SPI Serial Interface Functionality

The SPI serial interface of the ADRF6850 consists of the CS, SDI (SDI/SDA), CLK (CLK/SCL), and SDO pins. CS is used to select the device when more than one device is connected to the serial clock and data lines. CLK is used to clock data in and out of the part. The SDI line is used to write to the registers. The SDO pin is a dedicated output for the read mode. The part operates in slave mode and requires an externally applied serial clock to the CLK pin. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

Figure 66 shows an example of a write operation to the ADRF6850. Data is clocked into the registers on the rising edge of CLK using a 24-bit write command. The first eight bits represent the write command (0xD4), the next eight bits are the register address, and the final eight bits are the data to be written to the specific register. Figure 67 shows an example of a read operation. In this example, a shortened 16-bit write command is first used to select the appropriate register for a read operation, the first eight bits representing the write command (0xD4) and the final eight bits representing the specific register. Then the CS line is pulsed low for a second time to retrieve data from the selected register using a 16-bit read command, the first eight bits representing the read command (0xD5) and the final eight bits representing the contents of the register being read. Figure 3 shows the timing for both SPI read and SPI write operations.

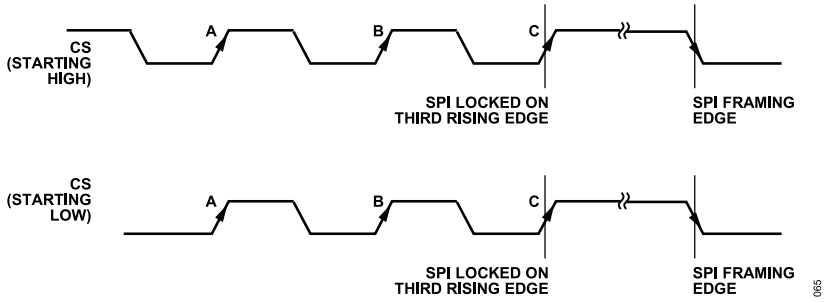


Figure 65. Selecting the SPI Protocol

THEORY OF OPERATION

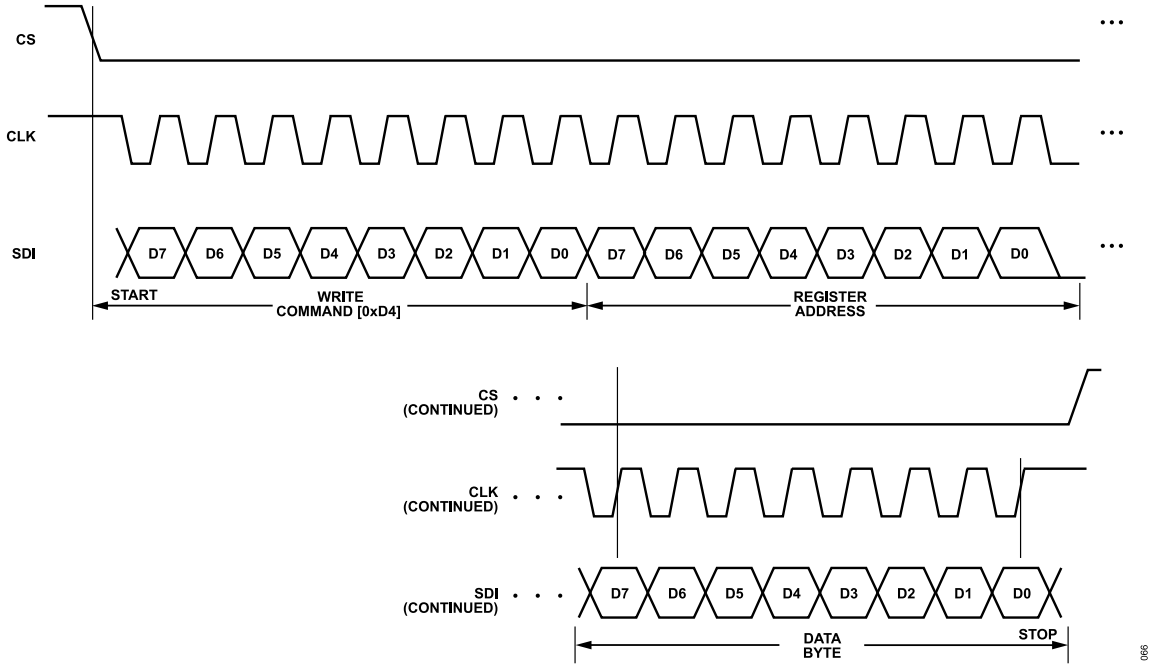


Figure 66. SPI Byte Write Example

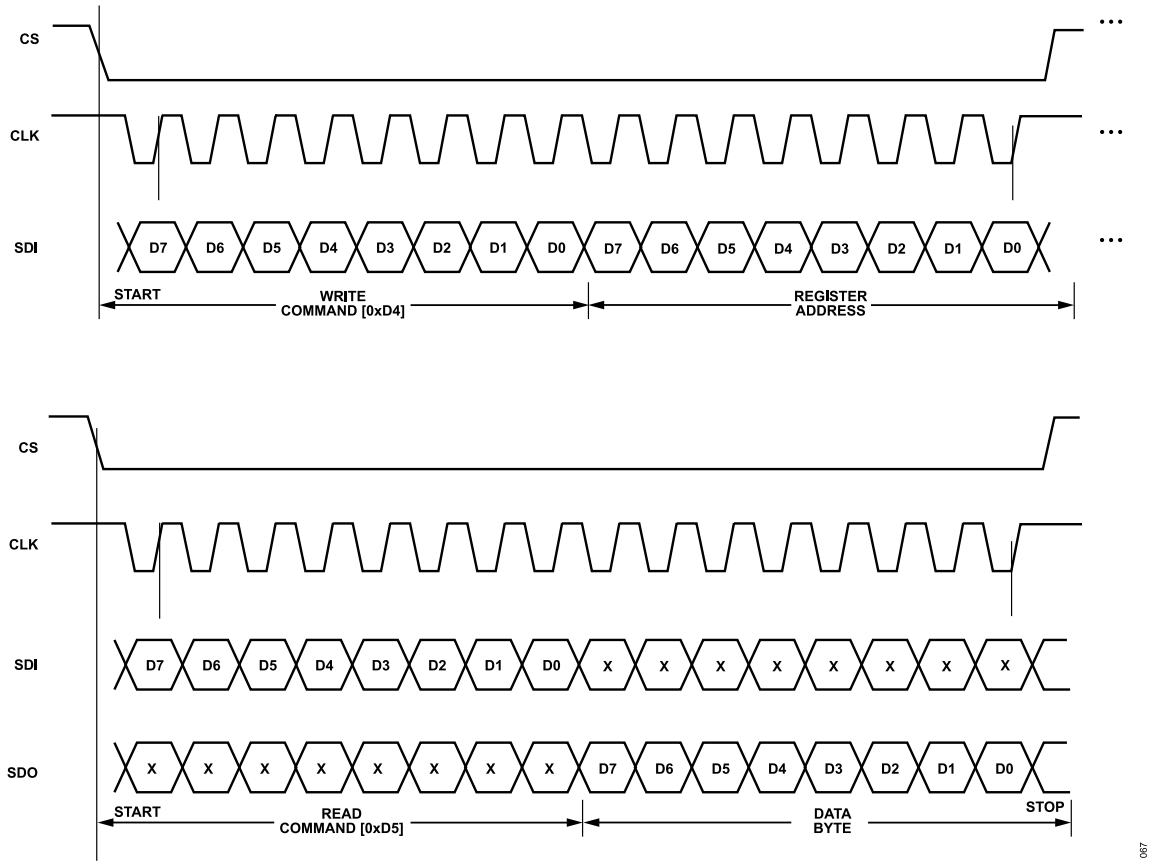


Figure 67. SPI Byte Read Example

THEORY OF OPERATION

PROGRAM MODES

The ADRF6850 has 34 8-bit registers to allow program control of a number of functions. Only 31 of these registers are writeable. Either an SPI or an I^2C interface can be used to program the register set. For details about the interfaces and timing, see Figure 61 to Figure 67. The registers are documented in Table 8 to Table 27.

Several settings in the ADRF6850 are double buffered. These settings include the FRAC value, the INT value, the RFDIV value, the 5-bit R-divider value, the reference doubler, the R ÷2 divider, and the charge pump current setting. This means that two events must occur before the part uses a new value for any of the double buffered settings. First, the new value is latched into the device by writing to the appropriate register. Next, a new write must be performed on Register CR0. When Register CR0 is written, a new PLL acquisition occurs.

For example, updating the fractional value involves a write to Register CR3, Register CR2, Register CR1, and Register CR0. Register CR3 should be written to first, followed by Register CR2 and Register CR1 and, finally, Register CR0. The new acquisition begins after the write to Register CR0. Double buffering ensures that the bits written to do not take effect until after the write to Register CR0.

12-Bit Integer Value

Register CR7 and Register CR6 program the integer value (INT) of the feedback division factor (N); see Equation 5 for details. The INT value is a 12-bit number whose MSBs are programmed through Register CR7, Bits[3:0]. The LSBs are programmed through Register CR6, Bits[7:0]. The LO frequency setting is described by Equation 2. An alternative to this equation is provided by Equation 4, which details how to set the N-divider value. Note that these registers are double buffered.

25-Bit Fractional Value

Register CR3 to Register CR0 program the fractional value (FRAC) of the feedback division factor (N); see Equation 5 for details. The FRAC value is a 25-bit number whose MSB is programmed through Register CR3, Bit 0. The LSB is programmed through Register CR0, Bit 0. The LO frequency setting is described by Equation 2. Again, an alternative to this equation is described by Equation 4, which details how to set the N-divider value. Note that these registers are double buffered.

RFDIV Value

The RFDIV value is dependent on the value of the LO frequency. The RFDIV value can be selected from the list in Table 6. Apply the selected RFDIV value to Equation 4, together with the LO frequency and PFD frequency values, to calculate the correct N-divider value.

Reference Input Path

The reference input path consists of a reference doubler, a 5-bit frequency divider, and a divide-by-2 function (see Figure 54). The doubler is programmed through Register CR10, Bit 5. The 5-bit divider is enabled by programming Register CR5, Bit 4; and the division ratio is programmed through Register CR10, Bits[4:0]. The R ÷2 divider is programmed through Register CR10, Bit 6. Note that these registers are double buffered.

Charge Pump Current

Register CR9, Bits[7:4], set the charge pump current setting. With an R_{SET} value of 4.7 kΩ, the maximum charge pump current is 5 mA. The following equation applies:

$$I_{CP\ max} = 23.5/R_{SET} \quad (6)$$

The charge pump current has 16 settings from 325 µA to 5 mA.

Power-Down/Power-Up Control Bits

The four programmable power-up and power-down control bits are as follows:

- Register CR12, Bit 2. Master power control bit for the PLL, including the VCO. This bit is normally set to a default value of 0 to power up the PLL.
- Register CR27, Bit 2. Controls the LO monitor outputs, LOMON and $\overline{\text{LOMON}}$. The default is 0 when the monitor outputs are powered down. Setting this bit to 1 powers up the monitor outputs to one of −6 dBm, −12 dBm, −18 dBm, or −24 dBm, as controlled by Register CR27, Bits[1:0].
- Register CR29, Bit 0. Controls the quadrature demodulator power. The default is 0, which powers down the demodulator. Write a 1 to this bit to power up the demodulator.
- Register CR30, Bit 0. This bit controls the VGA power and must be set to a 1 to power up the VGA.

Lock Detect (LDET)

Lock detect is enabled by setting Register CR23, Bit 4, to 1. Register CR23, Bit 3, in conjunction with Register CR14, Bit 7, sets the number of up/down pulses generated by the PFD before lock detect is declared by the LDET pin returning high. The options are 2048 pulses, 3072 pulses, and 4096 pulses.

The default setting is 3072 pulses, which is selected by programming Register CR23, Bit 3, to 0, and Register CR14, Bit 7, to 0. A more aggressive setting of 2048 is selected when Register CR23, Bit 3, is set to 1 and Register CR14, Bit 7, is set to 0. This improves the lock detect time by 50 µs (for a PFD frequency of 27 MHz). Note, however, that it does not affect the acquisition time to an error frequency of 1 kHz. A setting of 4096 pulses is selected when Register CR14, Bit 7, is set to 1. For best operation, set Register CR23, Bit 2 to 0. This bit sets up the PFD up/down pulses to a coarse or low precision setting.

THEORY OF OPERATION

Baseband VOCM Reference

Register CR29, Bit 6, selects whether the common-mode reference for the baseband outputs is internal or external. When the baseband outputs are ac-coupled, then the internal reference must be selected by setting Register CR29, Bit 6, to 1, and by grounding Pin 7, VOCM.

When the baseband outputs are dc-coupled, it is likely that an external bias is needed unless the internal dc bias provided is within a suitable range to match the specification of the follow-on device. This is accomplished by setting Register CR29, Bit 6, to 0, and driving Pin 7, VOCM, with the requisite external bias voltage.

Narrow-Band and Wideband Filter Mode

By default, the second-order low-pass filter in the output buffers of the baseband output signal paths is selected, and the baseband outputs are in narrow-band mode. By setting Register CR29, Bits[5:4], this filter can be set to a cutoff frequency of 50 MHz, 43 MHz, 37 MHz, or 30 MHz. By setting Register CR29, Bit 3, to 1, this filter is bypassed and wideband mode is selected.

Table 7. Baseband Filter Settings

CR29[5:4]	Filter Cutoff Frequency (MHz)
00	50
01	43
10	37
11	30

VGA Gain Mode Polarity

The polarity of the VGA gain is set by programming Bit 2 of Register CR30. By setting Register CR30, Bit 2, to 0, a positive gain slope is selected where V_{GAIN} = 0 V sets the VGA gain to be 0 dB, and V_{GAIN} = 1.5 V sets the VGA gain to be 60 dB. By setting Register CR30, Bit 2, to 1, a negative gain slope is selected.

REGISTER MAP

REGISTER MAP SUMMARY

Table 8. Register Map Summary

Register Address (Hex)	Register Name	Type	Description
0x00	CR0	Read/write	Fractional Word 4
0x01	CR1	Read/write	Fractional Word 3
0x02	CR2	Read/write	Fractional Word 2
0x03	CR3	Read/write	Fractional Word 1
0x04	CR4	Read/write	Reserved
0x05	CR5	Read/write	Reference 5-bit, R-divider enable
0x06	CR6	Read/write	Integer Word 2
0x07	CR7	Read/write	Integer Word 1
0x08	CR8	Read/write	Reserved
0x09	CR9	Read/write	Charge pump current setting
0x0A	CR10	Read/write	Reference frequency control
0x0B	CR11	Read/write	Reserved
0x0C	CR12	Read/write	PLL power-up
0x0D	CR13	Read/write	Reserved
0x0E	CR14	Read/write	Lock Detector Control 2
0x0F	CR15	Read/write	Reserved
0x10	CR16	Read/write	Reserved
0x11	CR17	Read/write	Reserved
0x12	CR18	Read/write	Reserved
0x13	CR19	Read/write	Reserved
0x14	CR20	Read/write	Reserved
0x15	CR21	Read/write	Reserved
0x16	CR22	Read/write	Reserved
0x17	CR23	Read/write	Lock Detector Control 1
0x18	CR24	Read/write	Autocalibration
0x19	CR25	Read/write	Autocalibration timer
0x1A	CR26	Read/write	Reserved
0x1B	CR27	Read/write	LO monitor output
0x1C	CR28	Read/write	LO selection
0x1D	CR29	Read/write	Demodulator power and filter selection
0x1E	CR30	Read/write	VGA
0x1F	CR31	Read only	Reserved
0x20	CR32	Read only	Reserved
0x21	CR33	Read only	Revision code

REGISTER MAP

REGISTER BIT DESCRIPTIONS

Table 9. Register CR0 (Address 0x00), Fractional Word 4

Bit	Description
7	Fractional Word F7[1]
6	Fractional Word F6[1]
5	Fractional Word F5[1]
4	Fractional Word F4[1]
3	Fractional Word F3[1]
2	Fractional Word F2[1]
1	Fractional Word F1[1]
0	Fractional Word F0 (LSB)[1]

[1] Double buffered. Load on the write to Register CR0.

Table 10. Register CR1 (Address 0x01), Fractional Word 3

Bit	Description
7	Fractional Word F15[1]
6	Fractional Word F14[1]
5	Fractional Word F13[1]
4	Fractional Word F12[1]
3	Fractional Word F11[1]
2	Fractional Word F10[1]
1	Fractional Word F9[1]
0	Fractional Word F8[1]

[1] Double buffered. Load on the write to Register CR0.

Table 11. Register CR2 (Address 0x02), Fractional Word 2

Bit	Description
7	Fractional Word F23[1]
6	Fractional Word F22[1]
5	Fractional Word F21[1]
4	Fractional Word F20[1]
3	Fractional Word F19[1]
2	Fractional Word F18[1]
1	Fractional Word F17[1]
0	Fractional Word F16[1]

[1] Double buffered. Load on the write to Register CR0.

Table 12. Register CR3 (Address 0x03), Fractional Word 1

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Fractional Word F24 (MSB)[1]

[1] Double buffered. Load on the write to Register CR0.

Table 13. Register CR5 (Address 0x05), Reference 5-Bit, R-Divider Enable

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	5-bit R-divider enable[1] 0 = disable 5-bit R-divider (default) 1 = enable 5-bit R-divider
3	Reserved
2	Reserved
1	Reserved
0	Reserved

[1] Double buffered. Load on the write to Register CR0.

Table 14. Register CR6 (Address 0x06), Integer Word 2

Bit	Description
7	Integer Word N7[1]
6	Integer Word N6[1]
5	Integer Word N5[1]
4	Integer Word N4[1]
3	Integer Word N3[1]
2	Integer Word N2[1]
1	Integer Word N1[1]
0	Integer Word N0[1]

[1] Double buffered. Load on the write to Register CR0.

Table 15. Register CR7 (Address 0x07), Integer Word 1

Bit	Description
[7:4]	MUXOUT control 0000 = tristate 0001 = logic high 0010 = logic low 1101 = RCLK/2 1110 = NCLK/2
3	Integer Word N11[1]
2	Integer Word N10[1]
1	Integer Word N9[1]
0	Integer Word N8[1]

[1] Double buffered. Load on the write to Register CR0.

Table 16. Register CR9 (Address 0x09), Charge Pump Current Setting

Bit	Description
[7:4]	Charge pump current[1] 0000 = 0.31 mA (default) 0001 = 0.63 mA 0010 = 0.94 mA 0011 = 1.25 mA 0100 = 1.57 mA 0101 = 1.88 mA 0110 = 2.19 mA 0111 = 2.50 mA

REGISTER MAP

Table 16. Register CR9 (Address 0x09), Charge Pump Current Setting

Bit	Description
	1000 = 2.81 mA
	1001 = 3.13 mA
	1010 = 3.44 mA
	1011 = 3.75 mA
	1100 = 4.06 mA
	1101 = 4.38 mA
	1110 = 4.69 mA
	1111 = 5.00 mA
3	Reserved
2	Reserved
1	Reserved
0	Reserved

[1] Double buffered. Load on the write to Register CR0.

Table 17. Register CR10 (Address 0x0A), Reference Frequency Control

Bit	Description
7	Reserved[1]
6	R divide-by-2 divider enable[1]
	0 = bypass R divide-by-2 divider
	1 = enable R divide-by-2 divider
5	R-doubler enable[1]
	0 = disable doubler (default)
	1 = enable doubler
[4:0]	5-bit R-divider setting[1]
	00000 = divide by 32 (default)
	00001 = divide by 1
	00010 = divide by 2
	…
	11110 = divide by 30
	11111 = divide by 31

[1] Double buffered. Load on the write to Register CR0.

Table 18. Register CR12 (Address 0x0C), PLL Power-Up

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	PLL power-down
	0 = power up PLL (default)
	1 = power down PLL
1	Reserved
0	Reserved

Table 19. Register CR14 (Address 0x0E), Lock Detector Control 2

Bit	Description
7	Lock Detector Up/Down Count 2
	0 = 2048/3072 up/down pulses
	1 = 4096 up/down pulses
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Reserved

Table 20. Register CR23 (Address 0x17), Lock Detector Control 1

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Lock detector enable
	0 = lock detector disabled (default)
	1 = lock detector enabled
3	Lock detector up/down count
	With Register CR14[7] = 0:
	0 = 3072 up/down pulses
	1 = 2048 up/down pulses
2	Lock detector precision
	0 = low, coarse (16 ns)
	1 = high, fine (6 ns)
1	Reserved
0	Reserved

Table 21. Register CR24 (Address 0x18), Autocalibration

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Disable autocalibration
	0 = enable autocalibration (default)
	1 = disable autocalibration

Table 22. Register CR25 (Address 0x19), Autocalibration Timer

Bit	Description
[7:0]	Autocalibration timer

Table 23. Register CR27 (Address 0x1B), LO Monitor Output

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved

REGISTER MAP

Table 23. Register CR27 (Address 0x1B), LO Monitor Output

Bit	Description
3	Reserved
2	Power-up monitor output
	0 = power down (default)
	1 = power up
[1:0]	Monitor output power into 50 Ω
	00 = −24 dBm (default)
	01 = −18 dBm
	10 = −12 dBm
	11 = −6 dBm

Table 24. Register CR28 (Address 0x1C), LO Selection

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved; set to 1
[2:0]	RFDIV
	000 = divide by 1; LO = 500 MHz to 1000 MHz
	001 = divide by 2; LO = 250 MHz to 500 MHz
	010 = divide by 4; LO = 125 MHz to 250 MHz
	011 = divide by 8; LO = 100 MHz to 125 MHz

Table 25. Register CR29 (Address 0x1D), Demodulator Power and Filter Selection

Bit	Description
7	Reserved
6	Internal baseband (V_{OCM}) select
	0 = select external baseband (V_{OCM}) reference
	1 = select internal baseband (V_{OCM}) reference
[5:4]	Narrow-band filter cut off
	00 = 50 MHz
	01 = 43 MHz
	10 = 37 MHz
	11 = 30 MHz
3	Baseband wideband/narrow-band modes
	0 = narrow-band mode
	1 = wideband mode
2	Reserved; set to 0
1	Reserved; set to 0
0	Power-up demodulator
	0 = power down (default)
	1 = power up

Table 26. Register CR30 (Address 0x1E), VGA

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved

Table 26. Register CR30 (Address 0x1E), VGA

Bit	Description
3	Reserved
2	VGA gain mode polarity
	0 = positive gain slope
	1 = negative gain slope
1	Reserved
0	Power-up VGA
	0 = power down
	1 = power up

Table 27. Register CR33 (Address 0x21), Revision Code[1]

Bit	Description
7	Revision code
6	Revision code
5	Revision code
4	Revision code
3	Revision code
2	Revision code
1	Revision code
0	Revision code

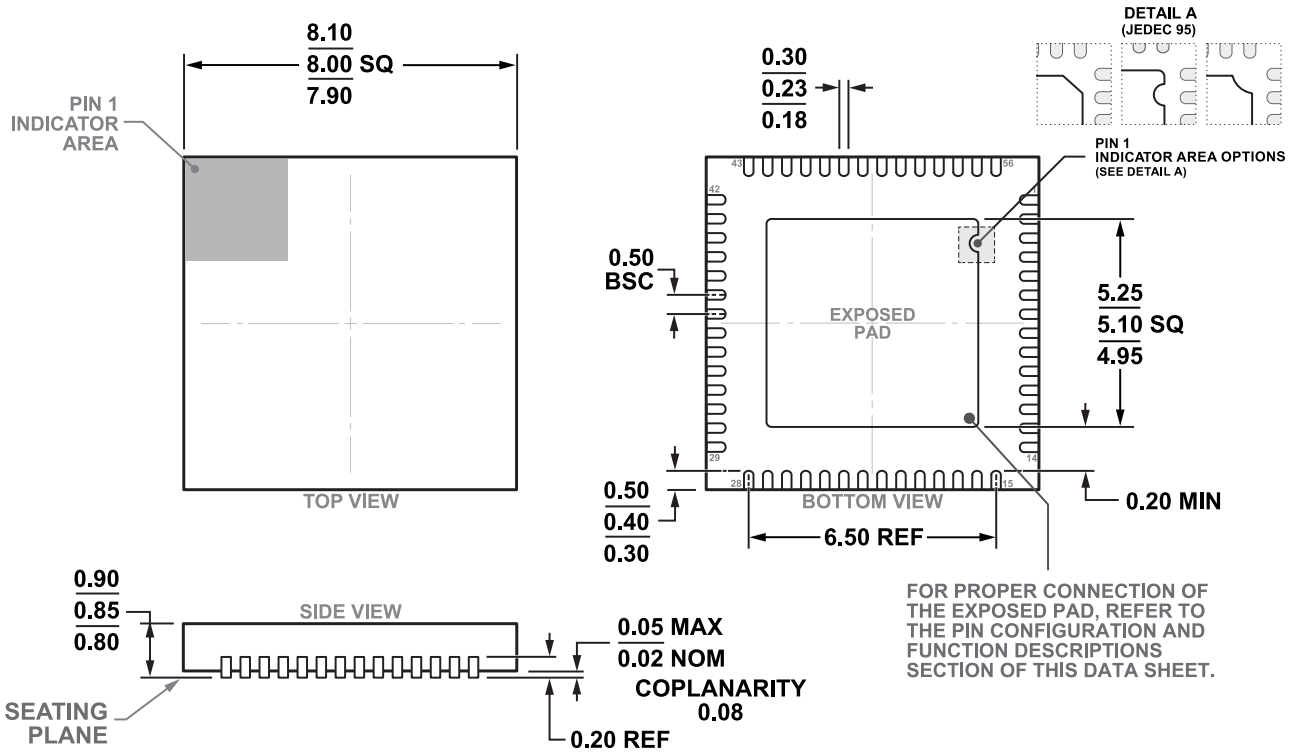
SUGGESTED POWER-UP SEQUENCE

INITIAL REGISTER WRITE SEQUENCE

After applying power to the device, adhere to the following write sequence, particularly with respect to the reserved register settings. Note that Register CR33, Register CR32, and Register CR31 are read-only registers. Also note that all writeable registers should be written to on power-up. Refer to the Register Map section for more details on all registers.

1. Write the following to Register CR30 = 0x00. Set VGA power to off and the VGA gain slope to be positive.
2. Write the following to Register CR29: 0x41. The demodulator is powered up. The baseband narrow-band mode is selected and set to a cutoff frequency of 50 MHz. The internal baseband V_{OCM} reference is selected.
3. Write the following to Register CR28: 0x0X RFDIV depends on the value of the LO frequency to be used and is set according to Table 6. Note that Register CR28, Bit 3, is set to 1.
4. Write the following to Register CR27: 0x00. Power the LO monitor in a power-down state.
5. Write the following to Register CR26: 0x00. Reserved register.
6. Write the following to Register CR25: 0x70. Set the autocalibration time to 100 µs with a PFD frequency setting of 27 MHz. If the PFD frequency is different, set CR25 according to Equation 3.
7. Write the following to Register CR24: 0x38. Enable autocalibration.
8. Write the following to Register CR23: 0x70. Enable lock detector and set lock detector counter = 3072 up/down pulses.
9. Write the following to Register CR22: 0x00. Reserved register.
10. Write the following to Register CR21: 0x00. Reserved register.
11. Write the following to Register CR20: 0x00. Reserved register.
12. Write the following to Register CR19: 0x00. Reserved register.
13. Write the following to Register CR18: 0x60. Reserved register.
14. Write the following to Register CR17: 0x00. Reserved register.
15. Write the following to Register CR16: 0x00. Reserved register.
16. Write the following to Register CR15: 0x00. Reserved register.
17. Write Register CR14: 0x00. Lock Detector Control 2.
18. Write Register CR13: 0x08. Reserved register.
19. Write the following to Register CR12: 0x18. PLL powered up.
20. Write the following to Register CR11: 0x00. Reserved register.
21. Write the following to Register CR10: 0x21. The reference path doubler is enabled and the 5-bit divider and R divide-by-2 divider are bypassed.
22. Write the following to Register CR9: 0x70. With the recommended loop filter component values and R_{SET} = 4.7 kΩ, the charge pump current is set to 2.5 mA for a loop bandwidth of 50 kHz.
23. Write the following to Register CR8: 0x00. Reserved register.
24. Write the following to Register CR7: 0x0X. Set according to Equation 4 and Equation 5 in the Theory of Operation section.
25. Write the following to Register CR6: 0xXX. Set according to Equation 4 and Equation 5 in the Theory of Operation section.
26. Write Register CR5: 0x00. Disable the 5-bit reference divider.
27. Write the following to Register CR4: 0x01. Reserved register.
28. Write the following to Register CR3: 0x0X. Set according to Equation 4 and Equation 5 in the Theory of Operation section.
29. Write the following to Register CR2: 0xXX. Set according to Equation 4 and Equation 5 in the Theory of Operation section.
30. Write the following to Register CR1: 0xXX. Set according to Equation 4 and Equation 5 in the Theory of Operation section.
31. Write the following to Register CR0: 0xXX. Set according to Equation 4 and Equation 5 in the Theory of Operation section. Register CR0 must be the last register written for all the double buffered bit writes to take effect.
32. Monitor the LDET output or wait 260 µs to ensure that the PLL is locked.
33. Write the following to Register CR30: 0x01. Set the VGA to power on.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2

Figure 68. 56-Lead Lead Frame Chip Scale Package [LFCSP]
8 mm × 8 mm Body and 0.85 mm Package Height
(CP-56-20)
Dimensions shown in millimeters

Updated: July 08, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF6850BCPZ	-40°C to +85°C	56-Lead LFCSP (8mm x 8mm w/ EP)		CP-56-5
ADRF6850BCPZ-R7	-40°C to +85°C	56-Lead LFCSP (8mm x 8mm w/ EP)	Reel, 750	CP-56-5

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADRF6850-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).