DRV8836 Dual Low-Voltage H-Bridge IC

1 Features

- Dual-H-Bridge Motor Driver
  - Capable of Driving Two DC Motors or One Stepper Motor
  - Low MOSFET On-Resistance: HS + LS 305 mΩ
- 1.5-A Maximum Drive Current Per H-Bridge
- Configure Bridges Parallel for 3-A Drive Current
- 2-V to 7-V Operating Supply Voltage
- Flexible PWM or PHASE/ENABLE Interface
- Low-Power Sleep Mode With 95-nA Maximum Supply Current
- Dedicated nSLEEP Input Pin
- Tiny 2.00-mm × 3.00-mm WSON Package

2 Applications

- Battery-Powered:
  - DSLR Lenses
  - Consumer Products
  - Toys
  - Robotics
  - Cameras
  - Medical Devices

3 Description

The DRV8836 provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device has two H-bridge drivers, and can drive two DC motors or one stepper motor, as well as other devices like solenoids. The output driver block for each consists of N-channel power MOSFET configured as an H-bridge to drive the motor winding. An internal charge pump generates gate drive voltages.

The DRV8836 supplies up to 1.5-A of output current per H-bridge. It operates on a power supply voltage from 2 V to 7 V.

PHASE/ENABLE and IN/IN interfaces can be selected which are compatible with industry-standard devices. A low-power sleep mode is provided which turns off all unnecessary logic to provide a very low current state.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature.

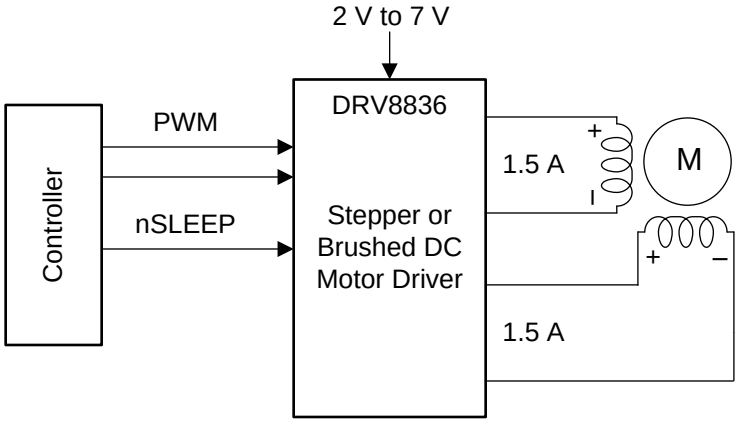
The DRV8836 is packaged in a tiny 12-pin WSON package (Eco-friendly: RoHS and no Sb/Br).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8836	WSON (12)	2.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2015) to Revision D — **Page**

- Deleted nFAULT from the *Simplified Schematic* in the *Description* section ... 1

Changes from Revision B (January 2014) to Revision C — **Page**

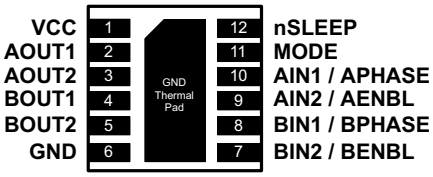
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (September 2013) to Revision B — **Page**

- Added t_{OCR} and t_{DEAD} parameters to *Electrical Characteristics* ... 5

5 Pin Configuration and Functions

DSS Package
12-Pin WSON
Top View



Pin Functions

PIN		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
GND, Thermal pad	6	—	Device ground	
VCC	1	—	Device and motor supply	Bypass to GND with a 0.1-μF (minimum) ceramic capacitor
CONTROL				
AIN1/APHASE	10	I	Bridge A input 1/PHASE input	IN/IN mode: Logic high sets AOUT1 high PH/EN mode: Sets direction of H-bridge A Internal pulldown resistor
AIN2/AENBL	9	I	Bridge A input 2/ENABLE input	IN/IN mode: Logic high sets AOUT2 high PH/EN mode: Logic high enables H-bridge A Internal pulldown resistor
BIN1/BPHASE	8	I	Bridge B input 1/PHASE input	IN/IN mode: Logic high sets BOUT1 high PH/EN mode: Sets direction of H-bridge B Internal pulldown resistor
BIN2/BENBL	7	I	Bridge B input 2/ENABLE input	IN/IN mode: Logic high sets BOUT2 high PH/EN mode: Logic high enables H-bridge B Internal pulldown resistor
MODE	11	I	Input mode select	Logic low selects IN/IN mode Logic high selects PH/EN mode Internal pulldown resistor
nSLEEP	12	I	Sleep input	Active low places part in low-power sleep state Internal pulldown resistor
OUTPUT				
AOUT1	2	O	Bridge A output 1	Connect to motor winding A
AOUT2	3	O	Bridge A output 2	
BOUT1	4	O	Bridge B output 1	Connect to motor winding B
BOUT2	5	O	Bridge B output 2	

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output.

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

		MIN	MAX	UNIT
	Power supply voltage, VCC	–0.3	7	V
	Digital input pin voltage	–0.5	VCC + 0.5	V
	Peak motor drive output current	Internally limited		A
	Continuous motor drive output current per H-bridge(3)	–1.5	1.5	A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values pertain to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Device power supply voltage	2	7	V
V_{IN}	Logic level input voltage	0	V_{CC}	V
I_{OUT}	H-bridge output current(1)	0	1.5	A
f_{PWM}	Externally applied PWM frequency	0	250	kHz

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC(1)		DRV8836 DSS (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VCC}	VCC operating supply current	f_{PWM} = 50 kHz, no load		1.7	2.5	mA
I_{CCQ}	VCC sleep mode supply current	nSLEEP = 0 V, all inputs 0 V		40	95	nA
		V_{CC} = 3 V, nSLEEP = 0 V, all inputs 0 V		10		
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising			2	V
		V_{CC} falling			1.9	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				0.25 × V_{CC}	V
V_{IH}	Input high voltage		0.5 × V_{CC}			V
I_{IL}	Input low current	V_{IN} = 0	–5		5	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
R_{PD}	Pulldown resistance			100		kΩ
H-BRIDGE FETS						
$R_{DS(ON)}$	HS + LS FET on resistance	V_{CC} = 3 V, I_O = 800 mA, T_J = 25°C		370	420	mΩ
		V_{CC} = 5 V, I_O = 800 mA, T_J = 25°C		305	355	
I_{OFF}	OFF-state leakage current				±200	nA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.6		3.5	A
t_{DEG}	Overcurrent deglitch time			1		µs
t_{OCR}	Overcurrent protection retry time			1		ms
t_{DEAD}	Output dead time			100		ns
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

6.6 Timing Requirements(1)

T_A = 25°C, V_{CC} = 5 V, R_L = 20 Ω

NO.			MIN	MAX	UNIT
1	t_1	Delay time, xPHASE high to xOUT1 low		210	ns
2	t_2	Delay time, xPHASE high to xOUT2 high		150	ns
3	t_3	Delay time, xPHASE low to xOUT1 high		150	ns
4	t_4	Delay time, xPHASE low to xOUT2 low		210	ns
5	t_5	Delay time, xENBL high to xOUTx high		150	ns
6	t_6	Delay time, xENBL high to xOUTx low		150	ns
7	t_7	Output enable time		210	ns
8	t_8	Output disable time		210	ns
9	t_9	Delay time, xINx high to xOUTx high		125	ns
10	t_{10}	Delay time, xINx low to xOUTx low		125	ns
11	t_R	Output rise time	20	188	ns
12	t_F	Output fall time	8	30	ns

(1) Not production tested – ensured by design

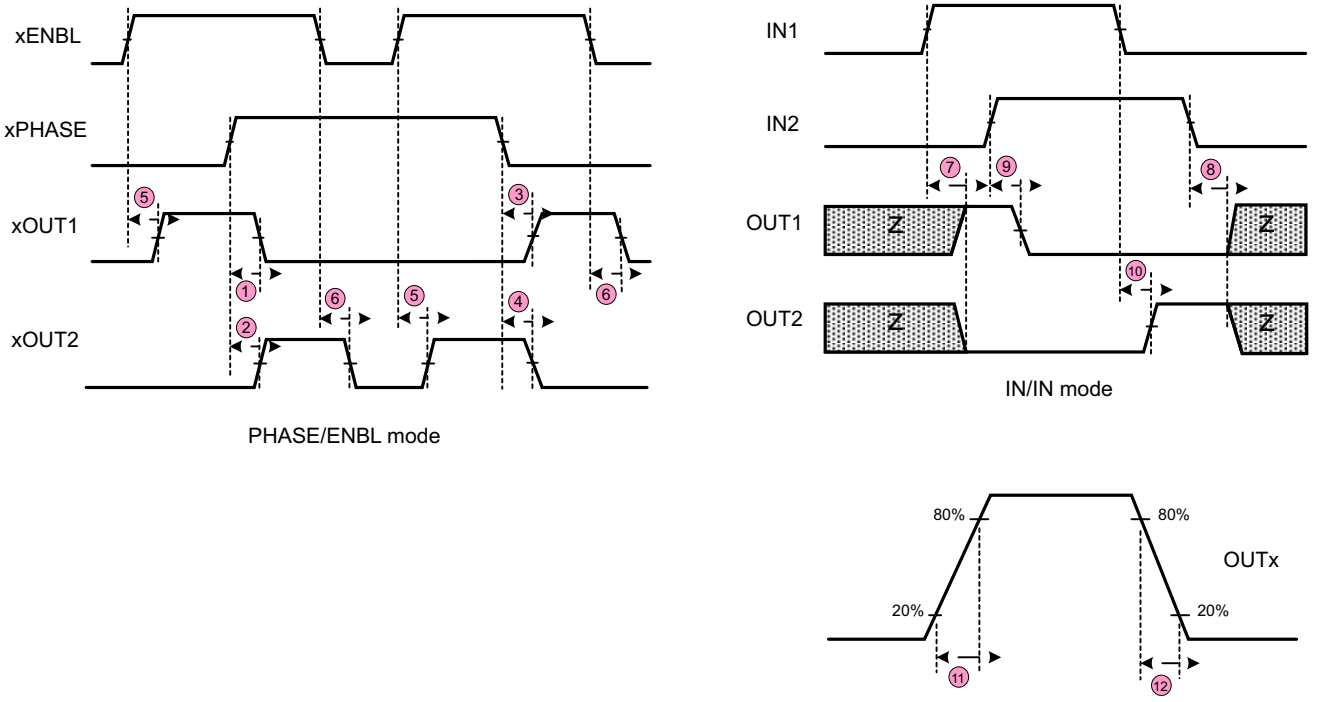


Figure 1. Timing Requirements

6.7 Typical Characteristics

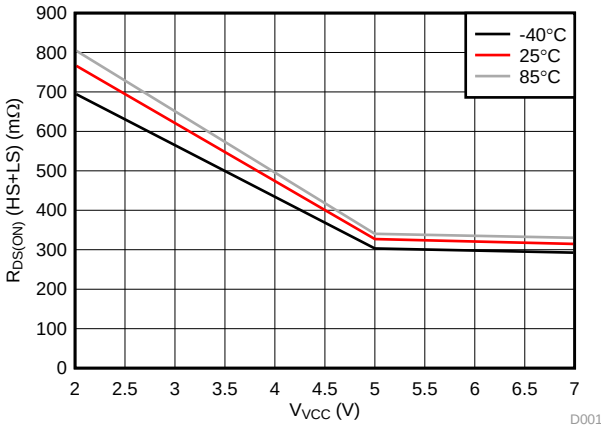


Figure 2. $RDS_{(ON)}$ (HS + LS)

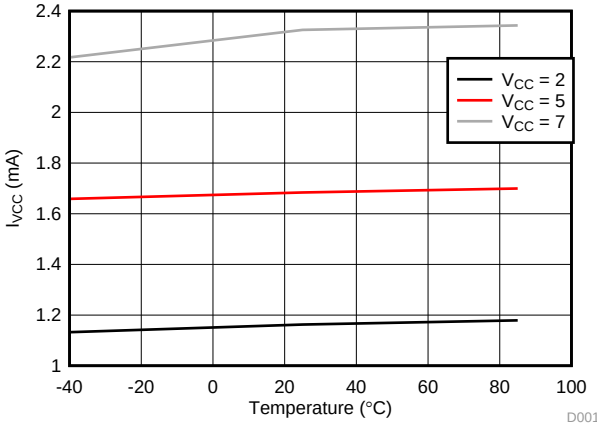


Figure 3. V_{CC} Operating Current, fPWM = 50 kHz, No Load

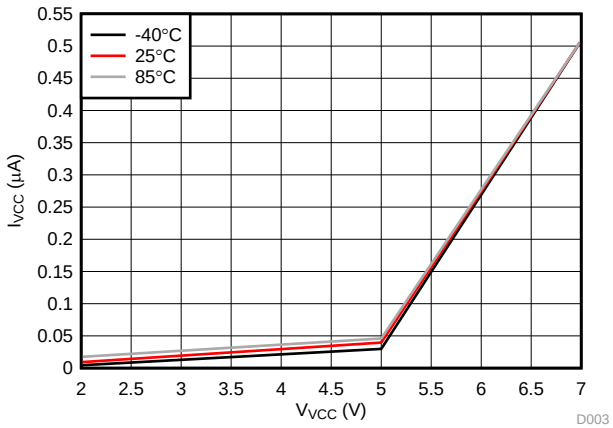


Figure 4. V_{CC} Sleep Current

7 Detailed Description

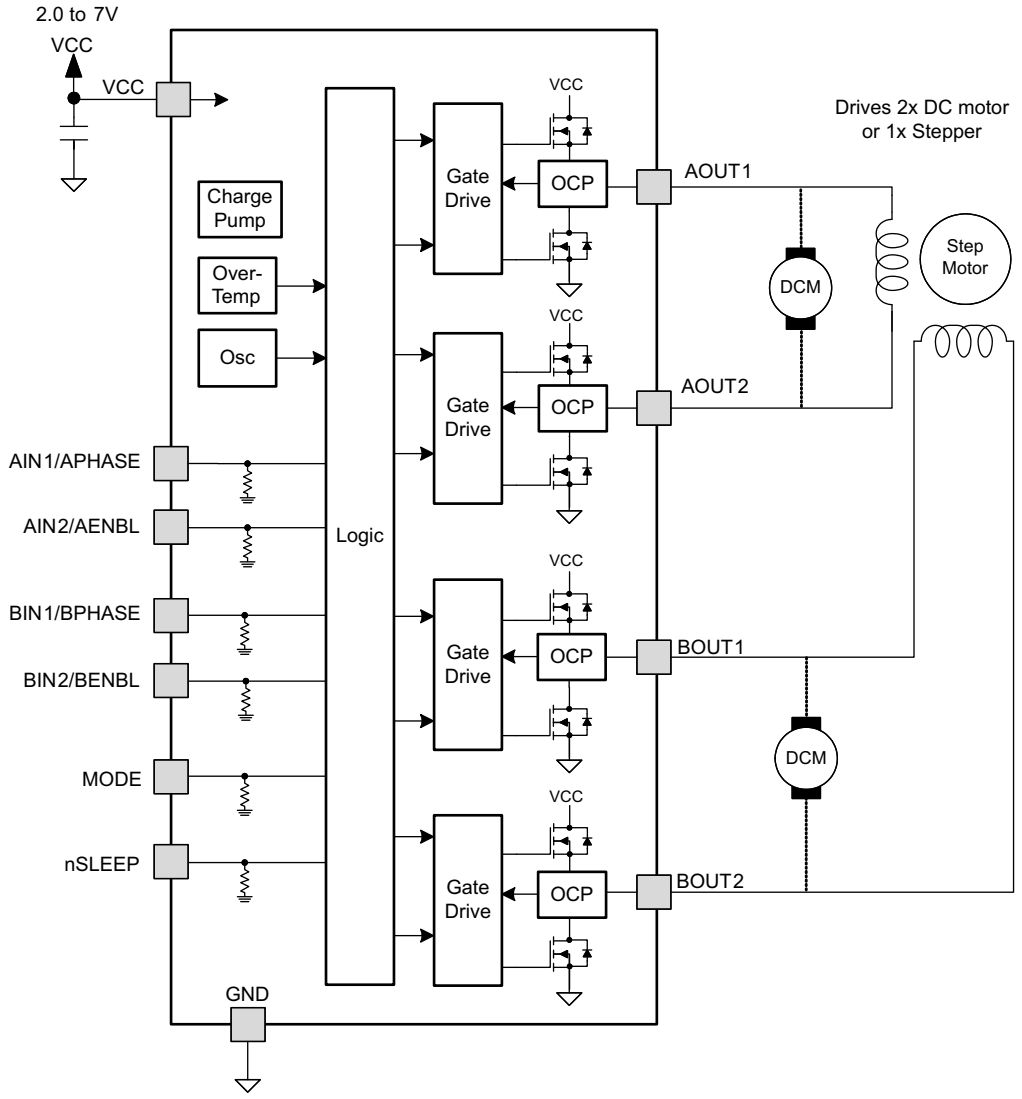
7.1 Overview

The DRV8836 is an integrated motor driver solution used for brushed motor control. The device integrates two H-bridges, and can drive two DC motor or one stepper motor. The output driver block for each H-bridge consists of N-channel power MOSFETs. An internal charge pump generates the gate drive voltages. Protection features include overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature protection.

The bridges connect in parallel for additional current capability.

The mode pin allows selection of either a PHASE/ENABLE or IN/IN interface.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Sleep Mode

If the nSLEEP pin enters a logic-low state, the DRV8836 enters a low-power sleep mode. In this state all unnecessary internal circuitry is powered down.

7.3.2 Power Supplies and Input Pins

There is a weak pulldown resistor (approximately 100 kΩ) to ground on the input pins.

7.3.3 Protection Circuits

The DRV8836 is fully protected against undervoltage, overcurrent, and overtemperature events.

7.3.3.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge disable. After approximately 1 ms, the bridge re-enables automatically.

Overcurrent conditions on both high and low side devices, like a short to ground, supply, or across the motor winding results in an overcurrent shutdown.

7.3.3.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge disable. Once the die temperature has fallen to a safe level operation automatically resumes.

7.3.3.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls below the undervoltage lockout threshold voltage, all circuitry in the device disables, and internal logic resets. Operation resumes when VCC rises above the UVLO threshold.

Table 1. Device Protection

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VCC undervoltage (UVLO)	VCC < VUVLO	None	Disabled	Disabled	VCC > VUVLO
Overcurrent (OCP)	IOUT > IOCP	None	Disabled	Operating	tOCR
Thermal shutdown (TSD)	TJ > TTSD	None	Disabled	Operating	TJ < TTSD – THYS

7.4 Device Functional Modes

The DRV8836 is active when the nSLEEP pin is set to a logic high. When in sleep mode, the H-bridge FETs disable (Hi-Z).

Table 2. Device Operating Modes

OPERATING MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Operating	nSLEEP high	Operating	Operating
Sleep mode	nSLEEP low	Disabled	Disabled
Fault encountered	Any fault condition met	Disabled	See Table 1

7.4.1 Bridge Control

Two control modes are available in the DRV8836: IN/IN mode and PHASE/ENABLE mode. IN/IN mode is selected if the MODE pin is driven low or left unconnected; PHASE/ENABLE mode is selected if the MODE pin is driven to logic high. The following tables show the logic for these modes.

Table 3. IN/IN Mode

MODE	xIN1	xIN2	xOUT1	xOUT2	FUNCTION (DC MOTOR)
0	0	0	Z	Z	Coast
0	0	1	L	H	Reverse
0	1	0	H	L	Forward
0	1	1	L	L	Brake

Table 4. PHASE/ENABLE Mode

MODE	xENABLE	xPHASE	xOUT1	xOUT2	FUNCTION (DC MOTOR)
1	0	X	L	L	Brake
1	1	1	L	H	Reverse
1	1	0	H	L	Forward

8 Application and Implementation

NOTE

The information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8836 is used in one or two motor control applications. When configured in parallel, the DRV8836 provides double the current to one motor.

8.2 Typical Application

The two H-bridges in the DRV8836 can be connected in parallel for double the current of a single H-bridge. Figure 5 shows the connections.

The following design is a common application of the DRV8836.

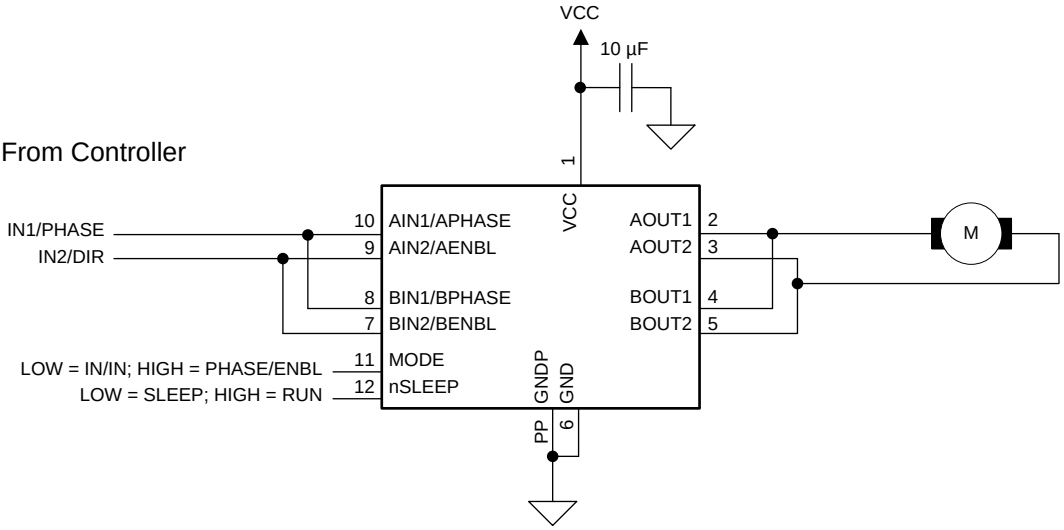


Figure 5. Parallel Mode Connections

8.2.1 Design Requirements

The design requirements are shown in Table 5.

Table 5. Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	VCC	4 V
Motor RMS current	IRMS	0.3 A
Motor startup current	ISTART	0.6 A
Motor current trip point	ILIMIT	0.5 A

8.2.2 Detailed Design Procedure

The following design procedure can be used to configure the DRV8836 in a brushed motor application.

8.2.2.1 Motor Voltage

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Low-Power Operation

When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

8.2.3 Application Curve

The following scope captures motor startup as VCC ramps from 0 V to 6 V. Channel 1 is V_{CC}, and Channel 4 is the motor current of an unloaded motor during startup. The motor used is a NMB Technologies Corporation OOB7PA12C, PPN7PA12C1. As V_{CC} ramps the current in the motor increases until the motor speed builds up. The motor current then reduces for normal operation.

Inputs are set as follows:

- Mode: IN/IN
- AIN1: High
- AIN2: Low

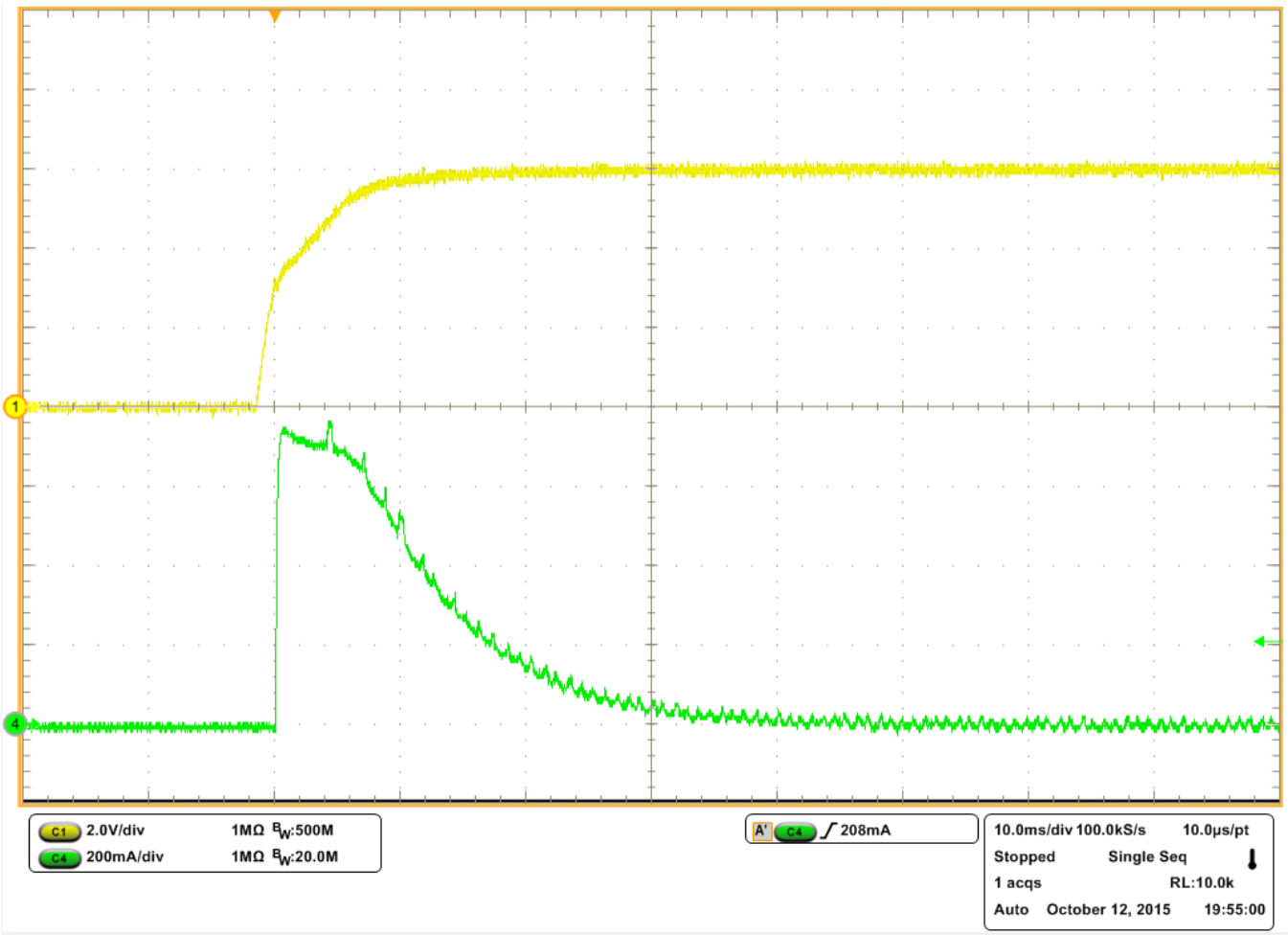


Figure 6. Motor Startup With No Load

9 Power Supply Recommendations

9.1 Bulk Capacitance

The appropriate local bulk capacitance is an important factor in motor drive system design. More bulk capacitance is generally beneficial but may increase costs and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate current changes from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

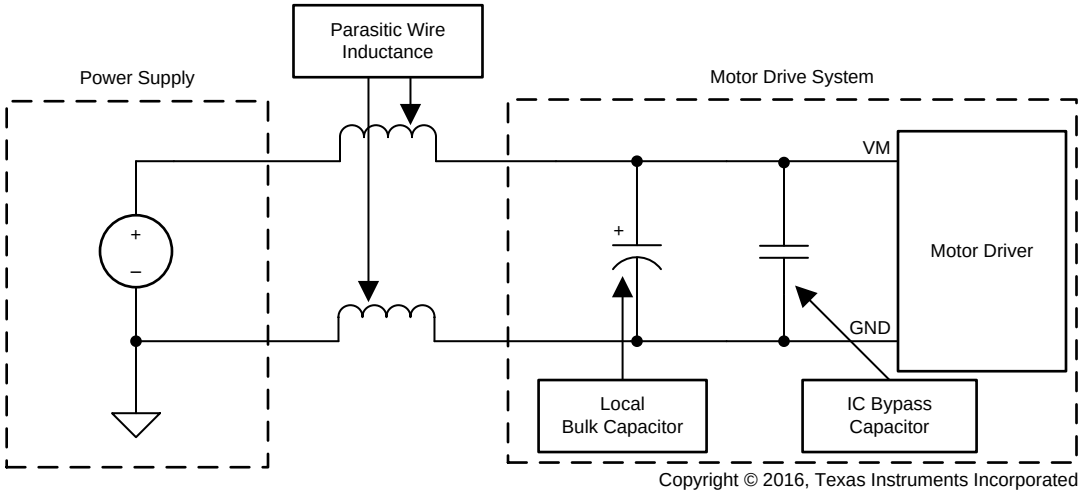


Figure 7. Bulk Capacitor

10 Layout

10.1 Layout Guidelines

The VCC pin should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1-µF rated for VCC. This capacitor should be placed as close to the VCC pin as possible with a thick trace or ground plane connection to the device GND pin.

The VCC pin must bypass to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8836.

10.2 Layout Example

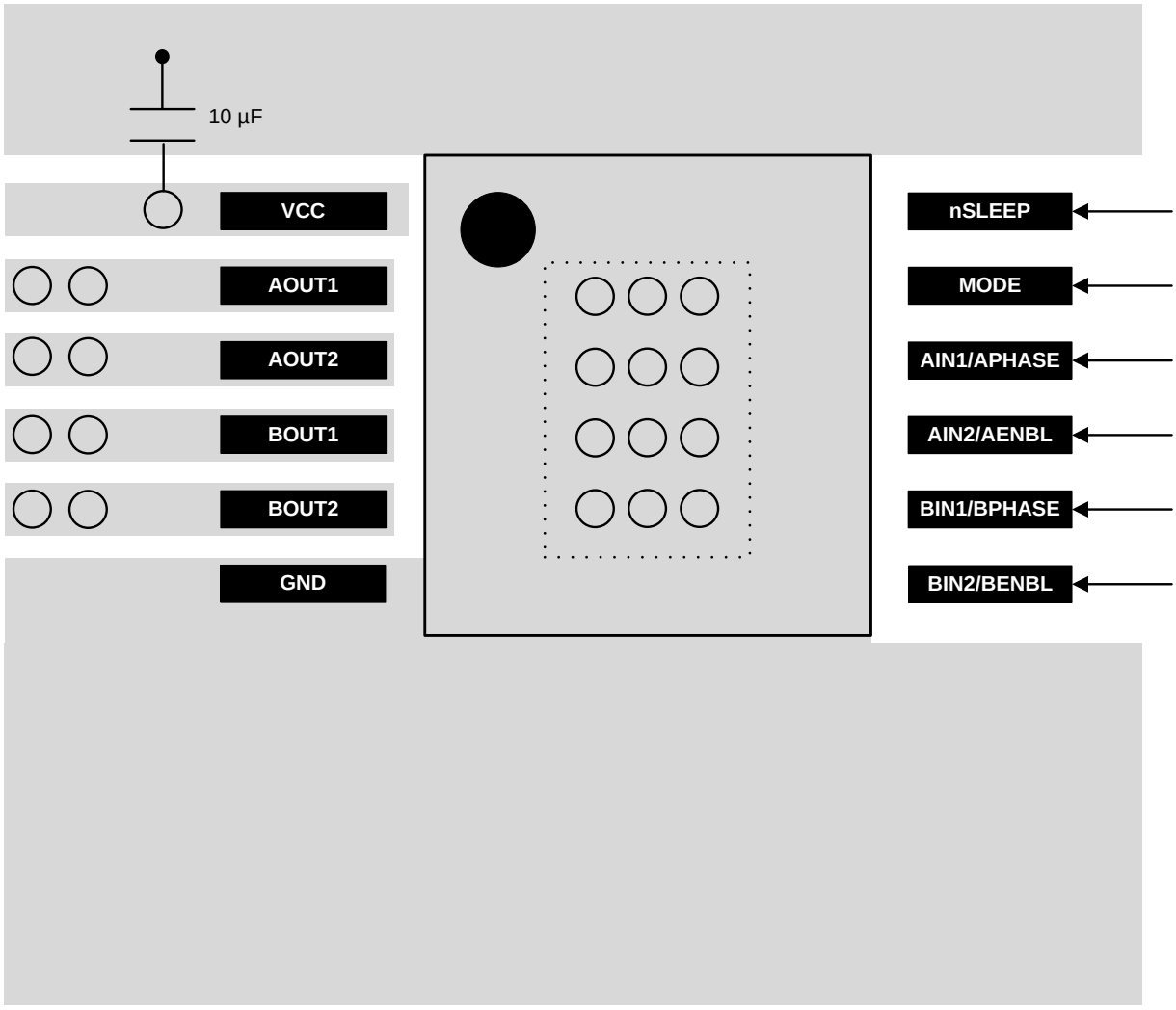


Figure 8. Layout Recommendation

10.3 Thermal Considerations

The DRV8836 has thermal shutdown (TSD) as described in *Thermal Shutdown (TSD)*. If the die temperature exceeds approximately 150°C, the device disables until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or an ambient temperature that is too high.

10.3.1 Power Dissipation

The power dissipated in the output FET resistance or $R_{DS(on)}$ dominates the power dissipation in the DRV8836. The average power dissipation when running both H-bridges can be roughly estimated by Equation 1:

$$P_{TOT} = 2 \times R_{DS(ON)} \times (I_{OUT(RMS)})^2 \quad (1)$$

where

- P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of the HS plus LS FETs, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to approximately 0.7× the full-scale output current setting. The factor of 2 comes from the fact that there are two H-bridges.

The maximum amount of power dissipated in the device is dependent on ambient temperature and heatsinking.

Thermal Considerations (continued)

NOTE

$R_{DS(ON)}$ increases with temperature. As the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For more information on PCB design, refer to TI application report SLMA002, *PowerPAD™ Thermally Enhanced Package*, and TI application brief SLMA004, *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Calculating Motor Driver Power Dissipation*, SLVA504
- *DRV8835/DRV8836 Evaluation Module*, SLVU694
- *Understanding Motor Driver Current Ratings*, SLVA505

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8836DSSR	ACTIVE	WSON	DSS	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	836	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

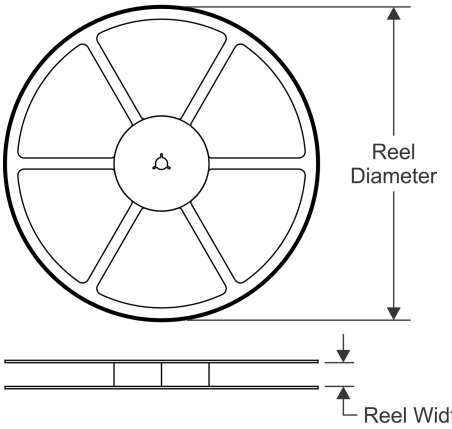
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

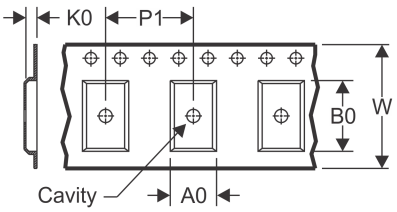
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

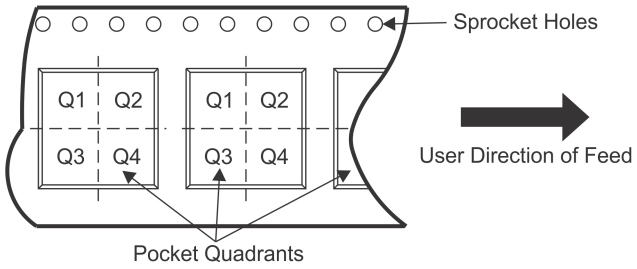


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

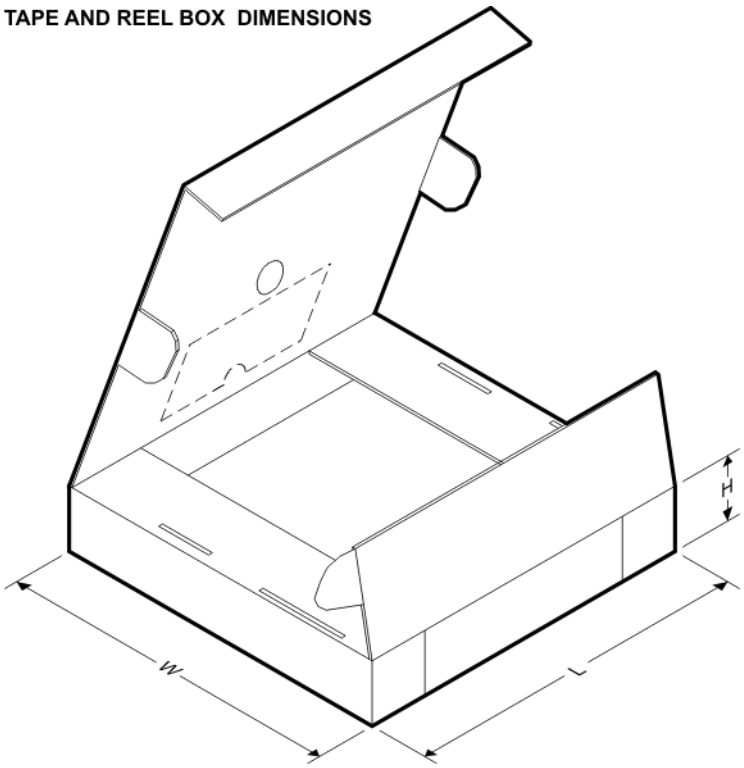
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8836DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



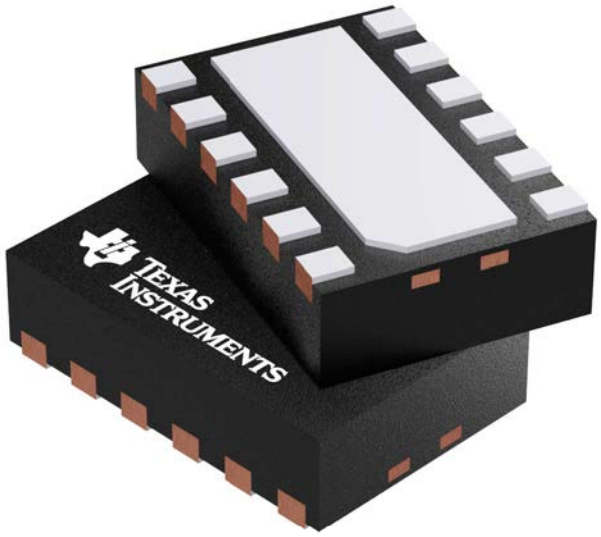
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8836DSSR	WSON	DSS	12	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DSS 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



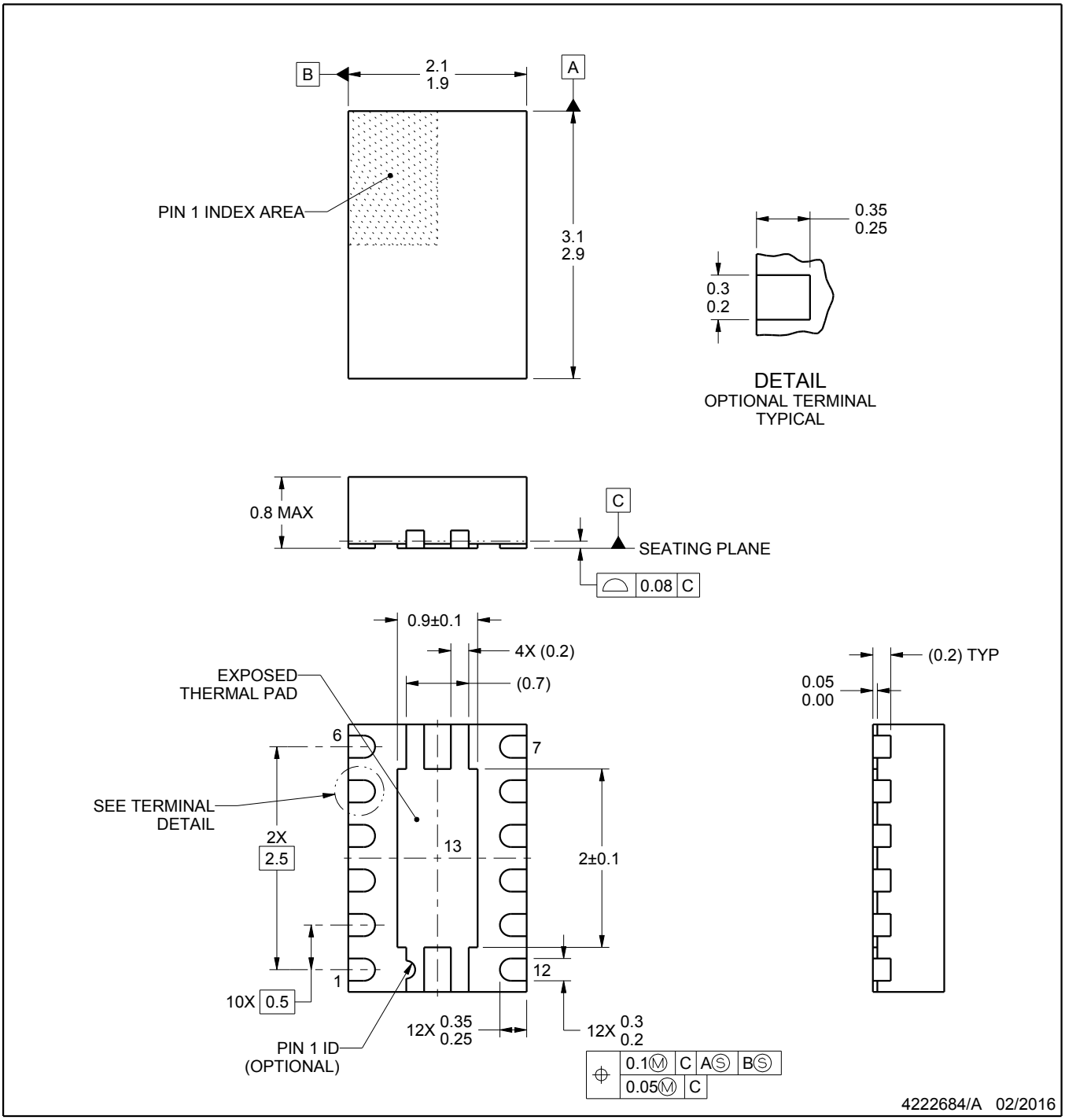
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSS0012A

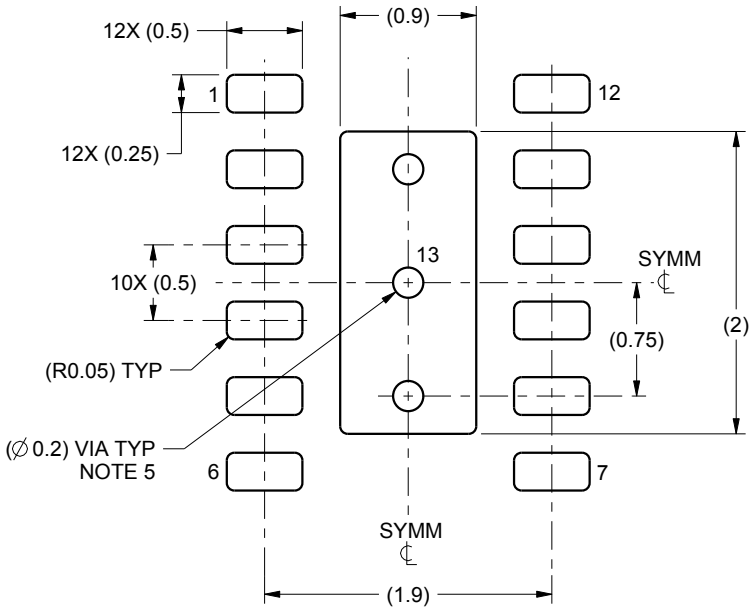
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

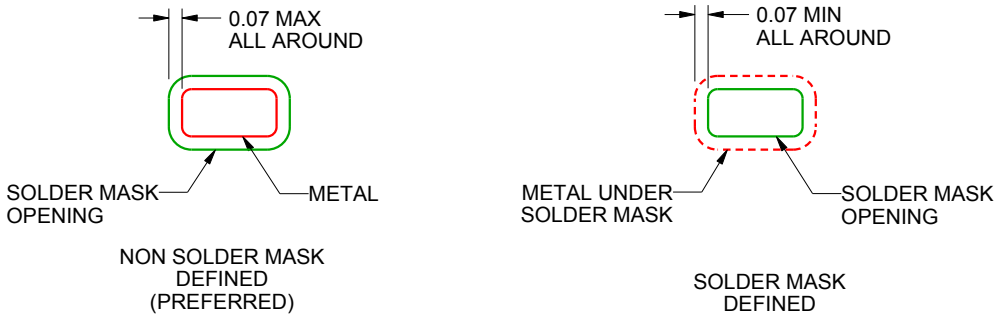


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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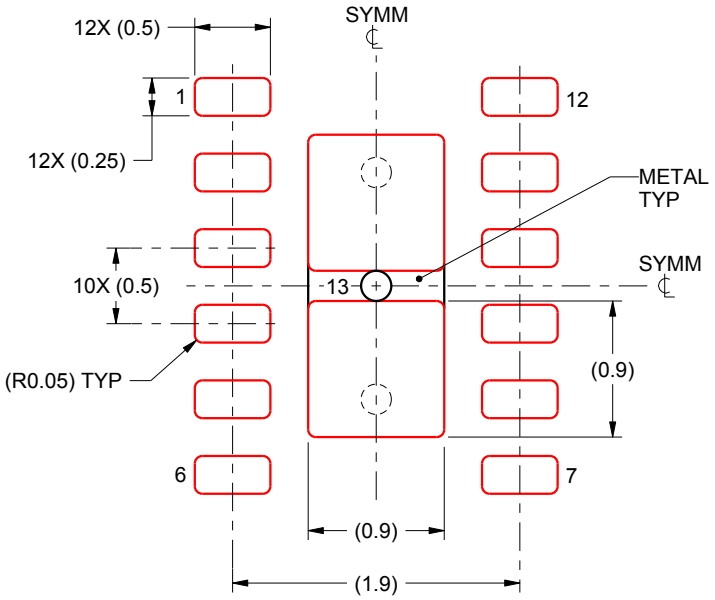
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown. It is recommended that vias located under solder paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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