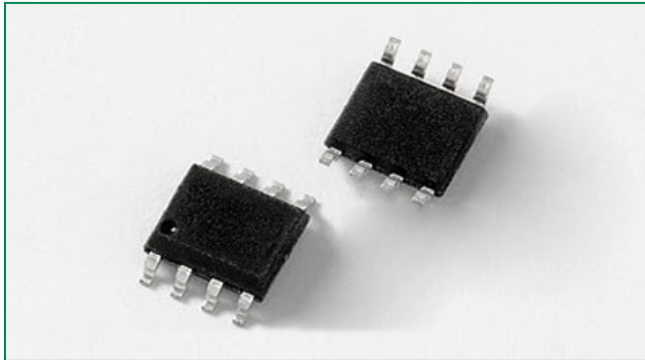


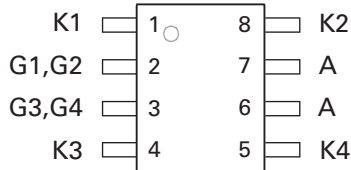
B61089QDR, Dual port negative voltage tracking SLIC protector



Agency Approvals

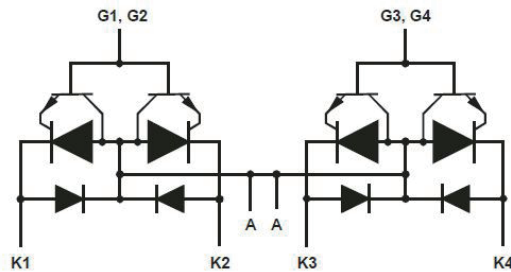
Agency	Agency File Number
	E133083

Pinout



Pin #	Pin Name	Description
1, 4, 5, 8	K1, K3, K4, K2	Connect to subscriber lines (Tip/Ring)
2, 3	G1, G2, G3, G4	Connect to battery (Reference Voltage)
6, 7	A	Connect to ground (earth)

Schematic Symbol



Description

This component is designed to protect two different SLIC (Subscriber Line Interface Card) tip/ring pairs with independent voltage tracking for each pair. This B61089QDR will protect the SLIC interface against lightning induced surge and power fault events. It contains fast switching crowbaring structures for negative events and a simple fast switching diode structure for positive events. It is compatible with the Basic Levels of ITU K.20, K.21. For compliance with the Enhanced Levels of ITU, TIA 968-B, or GR-1089, an additional series resistor in the tip and ring leads may be required.

The SLIC chipset voltage reference may change as the on-hook/off-hook line condition changes. Therefore, this component is referenced to the $-V_{BAT}$ so that its negative protection threshold follows this changing reference voltage level. This B61089QDR utilizes a transistor gain network so that a low 5 mA current level will activate the thyristor based portion of this protector component during negative events. This also allows an easier turn on during slow rising power fault events. For all positive disturbances, the fast switching diode connected to earth reference will provide the needed protection.

Features

- Dual port negative voltage tracking programmable component
- Supports battery voltages down to -170V
- Low gate triggering current 5 mA max
- Fails in a short circuit condition when it is surged in excess of its ratings to protect all downstream equipment
- Surge capability does not degrade after multiple surge events within its ratings
- High holding current 150 mA min
- Specified 2/10 limiting voltage
- Integrated diodes for positive surge protection
- ESD Immunity(HBM): JESD22 Class 3B, ≥8KV
- MSL: Level 1 - unlimited
- RoHS compliant and lead-free

Applications

- Wireless In the Local Loop (WLL)
- Voice applications which require regenerated POTS
- VoIP applications
- PBX
- FXS applications
- Digital Pair Gain systems (DPG) and Digital Loop Carrier systems (DLC)
- Small Office Home Office (SOHO)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Test Conditions	Value	Unit
I_{PPSM}^*	Non-repetitive peak on-state pulse current	10/1000 μs	30	A
		5/310 μs	40	
		2/10 μs	120	
		8/20 μs	110	
I_{TSM}/I_{FSM}^*	Non repetitive peak on-state current, 50Hz/60Hz	0.5s	6.5	A
		1s	4.5	
		5s	2.4	
		30s	1.3	
		900s	0.72	
I_{GSM}^*	Non repetitive peak gate current, 2/10 μs pulse, cathodes commoned		40	A
V_{DRM}	Repetitive peak off-state voltage, $V_{GK}=0$		-170	V
V_{GKRM}	Repetitive peak gate-cathode voltage, $V_{KA}=0$		-167	V
T_A	Operating free-air temperature range		-40 - 85	$^\circ\text{C}$
T_{STG}	Storage temperature range		-40 - 150	$^\circ\text{C}$
T_J	Junction temperature		-40 - 150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering during 10s		260	$^\circ\text{C}$
$R_{\theta JA}$	Junction to ambient thermal resistance	$P_{tot} = 0.8 \text{ W}, T_A = 25^\circ\text{C}, 5 \text{ cm}^2, \text{FR4 PCB}$	160	$^\circ\text{C}/\text{W}$

* Notes :

- Initially the protector must be in thermal equilibrium with $T_J = 25^\circ\text{C}$. The surge may be repeated after the component returns to its initial conditions.

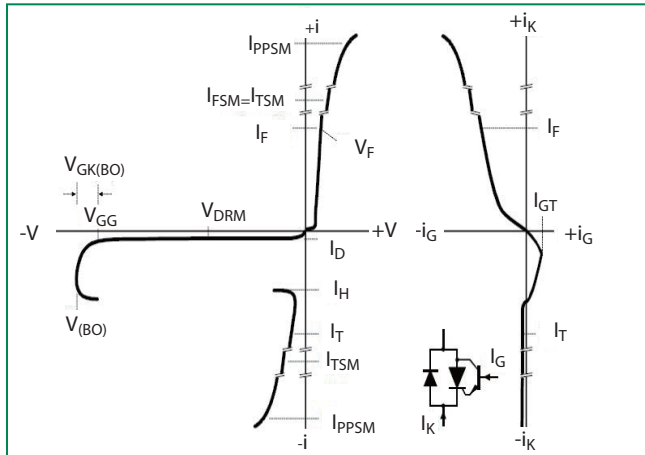
- These non-repetitive rated currents are peak values for either polarity. The rated current values may be applied to any cathode-anode terminal pair. Additionally, all cathode-anode terminal pairs may have their rated current values applied simultaneously (in this case the anode terminal current will be four times the rated current value of an individual terminal pair).

Electrical Characteristics

Symbol	Parameter	Test Conditions	Max	Unit
V_F	Forward voltage	$I_F = 5\text{A}, t_w = 200\mu\text{s}$	3	V
V_{FRM}	Ramp peak forward recovery voltage	$di/dt = \pm 10\text{A}/\mu\text{s}, dv/dt \leq \pm 100\text{V}/\mu\text{s}$ maximum ramp value = $\pm 10\text{A}, T_J = 25^\circ\text{C}$	5	V
V_{FRM}	Impulse peak forward recovery voltage	2/10 $\mu\text{s}, I_{TM} = -27\text{A}, R_s = 50\Omega, di/dt = -27\text{A}/\mu\text{s}$	12	V
I_D	Off-state current	$V_D = V_{DRM}, V_{GK} = 0, T_J = 25^\circ\text{C}$	-5	μA
$V_{(BO)}$	Ramp breakover voltage	$di/dt = \pm 10\text{A}/\mu\text{s}, dv/dt \leq \pm 100\text{V}/\mu\text{s}, V_{GG} = -100\text{V}$ maximum ramp value = $\pm 10\text{A}, T_J = 25^\circ\text{C}$	-112	V
$V_{(BO)}$	Impulse breakover voltage	2/10 $\mu\text{s}, I_{TM} = -27\text{A}, R_s = 50\Omega, di/dt = -27\text{A}/\mu\text{s}, V_{GG} = -100\text{V}$	-115	V
$V_{GK(BO)}$	Gate-cathode impulse breakover voltage	2/10 $\mu\text{s}, I_{TM} = -27\text{A}, R_s = 50\Omega, di/dt = -27\text{A}/\mu\text{s}, V_{GG} = -100\text{V}$	15	V
I_H	Holding current	$I_T = -1\text{A}, di/dt = 1\text{A}/\text{ms}, V_{GG} = -100\text{V}$	-150 (min)	mA
I_{GKS}	Gate reverse current	$V_{GG} = V_{GK} = V_{GKRM}, V_{KA} = 0, T_J = 25^\circ\text{C}$	-5	μA
I_{GT}	Gate trigger current	$I_T = -3\text{A}, t_{p(g)}^* \geq 20\mu\text{s}, V_{GG} = -100\text{V}, T_J = 25^\circ\text{C}$	5	mA
V_{GT}	Gate trigger voltage	$I_T = -3\text{A}, t_{p(g)}^* \geq 20\mu\text{s}, V_{GG} = -100\text{V}$	1.4	V
C_{KA}	Cathode-anode off-state capacitance	$f = 1\text{MHz}, V_d = 1\text{V}, I_G = 0, V_D = -3\text{V}$	100	pF
		$f = 1\text{MHz}, V_d = 1\text{V}, I_G = 0, V_D = -48\text{V}$	50	

* $T_{p(g)}$: gate pulse time

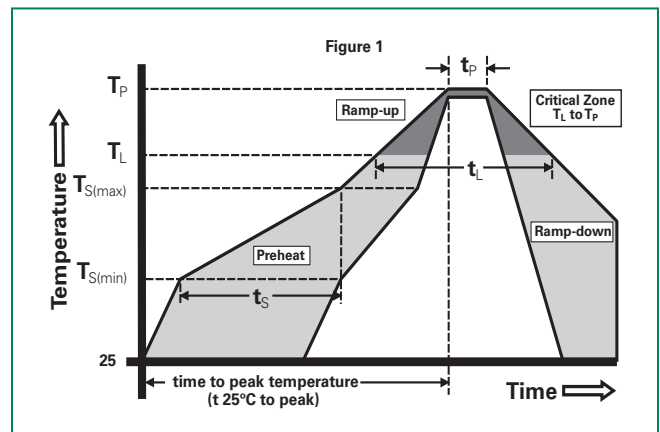
V-I Characteristics



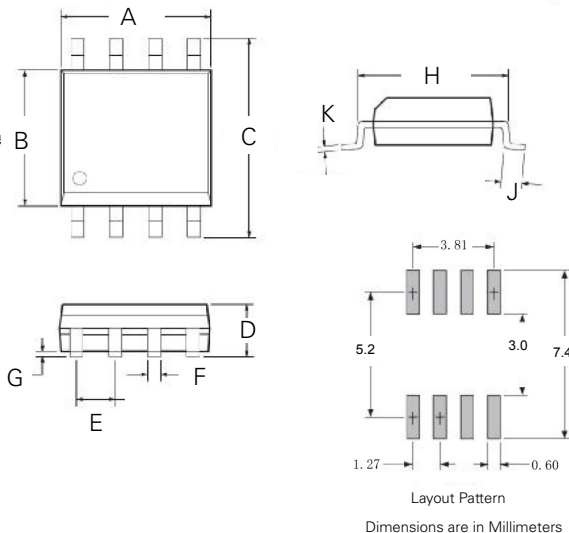
Parameter	Symbol
Off-state current	I_D
Repetitive peak off-state voltage	V_{DRM}
On-state Current(RMS)	I_T
Non-repetitive Peak On-state Current	I_{TSM}
Holding current	I_H
Breakover voltage	$V_{(BO)}$
Forward voltage	V_F
Gate-cathode impulse breakover voltage	$V_{GK(BO)}$
Gate trigger current	I_{GT}
SLIC supply voltage	V_{GG}

Soldering Parameters

Reflow Condition	Pb-Free assembly	
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)	3°C/sec. Max.	
$T_{s(max)}$ to T_L - Ramp-up Rate	3°C/sec. Max.	
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_p)	+260(+0/-5)°C	
Time within 5°C of actual Peak Temp (t_p)	30 secs. Max.	
Ramp-down Rate	6°C/sec. Max.	
Time 25°C to Peak Temp (T_p)	8 min. Max.	
Do not exceed	+260°C	



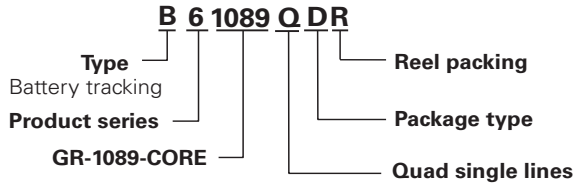
Dimensions — MS-012 (Narrow Body)



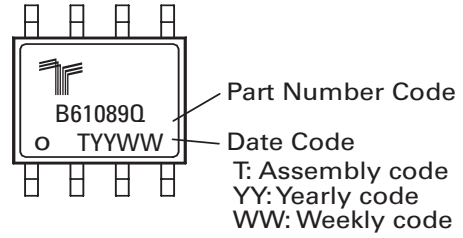
Dimension	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.193	0.201	4.90	5.10
B	0.154	0.162	3.62	4.12
C	0.228	0.244	5.80	6.20
D	0.053	0.069	1.35	1.74
E	0.050 BSC		1.27 BSC	
F	0.013	0.019	0.34	0.49
G	0.004	0.008	0.100	0.210
H	0.181	0.205	4.60	5.21
J	0.020	0.044	0.51	1.12
K	0.007	0.009	0.18	0.22

* BSC = Basic Spacing between Centers

Part Numbering



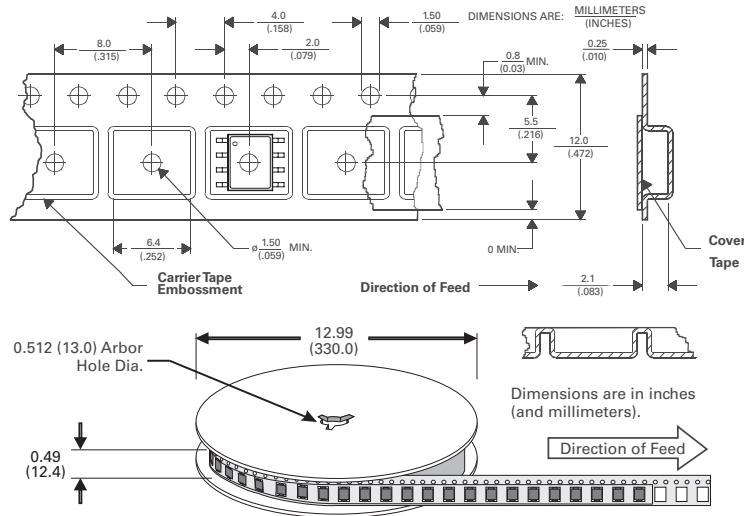
Part Marking



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
D	MS-012 SMT 8-pin SOIC Tape and Reel Pack	2500	N/A	EIA-481-D

Tape and Reel Specifications — MS-012 (Narrow Body)



Application Note

This B61089QDR MS-012 SMT (SOIC-8) Dual port Battrax® is specifically designed to provide surge protection for SLIC (Subscriber Line Interface Circuit) cards implementing negative ringing only. This single 8-pin component provides protection for two SLIC ports (T1/R1 & T2/R2) by shunting positive and negative surges to the ground reference.

The negative surges are diverted to ground through the SCRs which are connected between the TIP/RING conductors and the ground reference. These SCRs have a transistor buffered gate that provides a low current magnitude trigger level; typically 5 mA or less. The SCRs will reset when the magnitude of the loop current drops below the component's holding current parameter I_H . The fast switching diodes will turn on for any positive surge event > 3V between tip and ground or between ring and ground.

This SCR's turn-on threshold for negative polarity events tracks the negative reference voltage ($-V_{BAT}$) of the SMART SLIC component. As the line conditions change from off-hook to on-hook, the SLIC reference voltage level will also change in an effort to conserve energy. The negative tracking protection component will typically operate at a voltage of -1.4 V below $-V_{BAT}$ during negative surge conditions or power fault events.

The two gate capacitors, which act as charge reservoirs, supply the needed current to trigger the thyristor components to the on-state and should be physically located in close proximity to the B61089 gate (pins 2&3). During slow rising ac power fault events, the discharge current of the capacitor ($I_C = C dv/dt$) easily achieves the 5 mA threshold to activate the SCR. This solution below will comply with the power fault and surge requirements of GR-1089 Intra-building Port Type and the Basic level of ITU K20/21. For GR-1089 Port Type 3 and Enhanced level of ITU K20/21, the series resistor value may need to be increased. The TeleLink fuse complies with both GR-1089 intra-building and inter-building requirements and both Basic and Enhanced levels of the ITU Recommendations.

