



Dual P-Channel 1.8-V (G-S) MOSFET

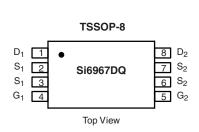
PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)			
- 8	0.030 at V _{GS} = - 4.5 V	± 5.0			
	0.045 at V _{GS} = - 2.5 V	± 4.0			
	0.070 at V _{GS} = - 1.8 V	± 3.0			

FEATURES

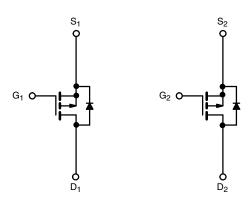
- · Halogen-free
- TrenchFET® Power MOSFETs: 1.8 V Rated



ROHS



Ordering Information: Si6967DQ-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unles	ss otherwise no	ted		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	- 8	.,	
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) ^{a, b}	T _A = 25 °C	1	± 5.0		
	T _A = 70 °C	I _D	± 4.0		
Pulsed Drain Current		I _{DM}	± 30	Α	
Continuous Source Current (Diode Conduction) ^{a, b}		I _S	- 1.25		
Maximum Power Dissipation ^{a, b}	T _A = 25 °C	В	1.1	10/	
	T _A = 70 °C	P _D	0.72	W	
Operating Junction and Storage Temperature Range		T _J , T _{stq}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}		110	°C/W		
	Steady State	' ¹thJA	115		C/ VV		

Notes:

- a. Surface Mounted on FR4 board.
- b. t≤10 s

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm.

Si6967DQ

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.45			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 6.4 V, V _{GS} = 0 V		- 1			
		$V_{DS} = -6.4 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			- 25	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge$ - 8 V, V_{GS} = - 4.5 V	- 30			Α	
Drain-Source On-State Resistance ^a		V _{GS} = - 4.5 V, I _D = - 5.0 A		0.024	0.030	5 Ω	
	R _{DS(on)}	$V_{GS} = -2.5 \text{ V}, I_D = -4.0 \text{ A}$		0.033	0.045		
		$V_{GS} = -1.8 \text{ V}, I_D = -3.0 \text{ A}$		0.048	0.070		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 8 V, I _D = - 5.0 A		18		S	
Diode Forward Voltage ^a	V_{SD}	I _S = - 1.25 A, V _{GS} = 0 V		- 0.68	- 1.1	V	
Dynamic ^b			•	•			
Total Gate Charge	Q_g			20	40	nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = -6 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -5.0 \text{ A}$		4.5			
Gate-Drain Charge	Q_{gd}			3.6		1	
Turn-On Delay Time	t _{d(on)}			20	50		
Rise Time	t _r	V_{DD} = - 6 V, R_L = 6 Ω		30	60	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ - 1 A, V_{GEN} = - 4.5 V, R_G = 6 Ω		85	150		
Fall Time	t _f			50	90		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 1.25 A, dI/dt = 100 A/μs		50	100		

Notes:

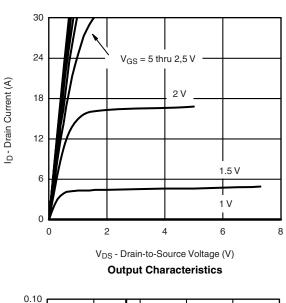
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

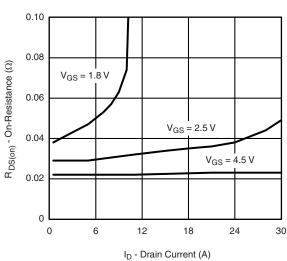
a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

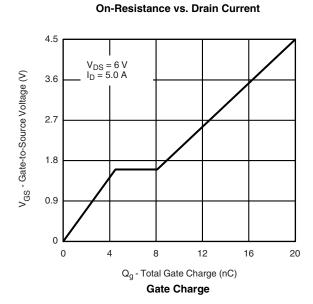
b. Guaranteed by design, not subject to production testing.

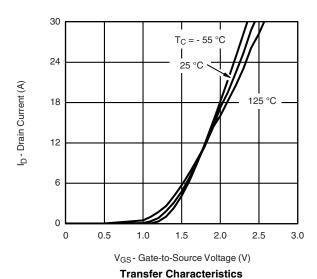


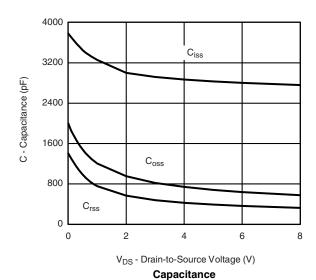
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

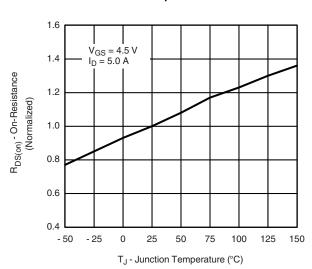










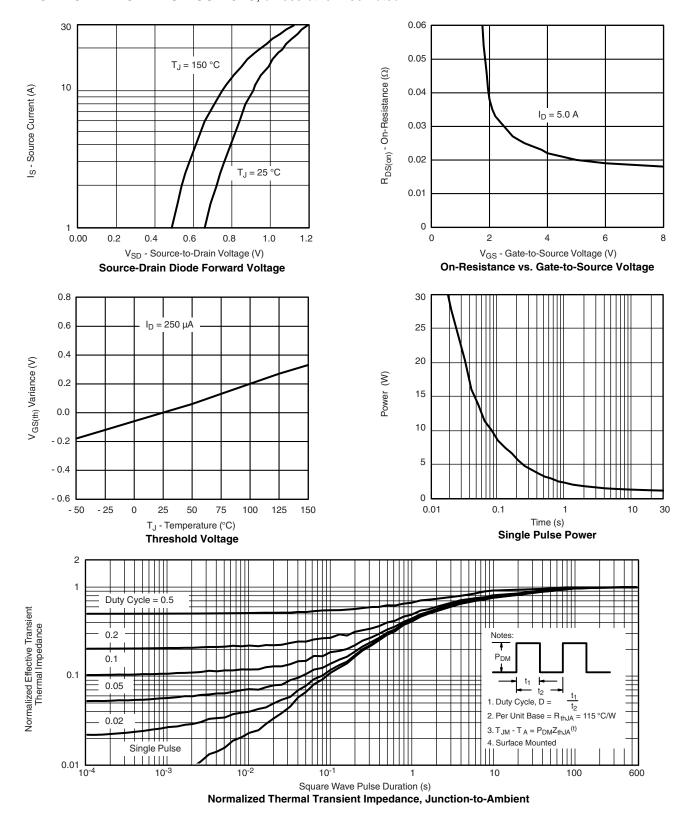


On-Resistance vs. Junction Temperature

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70811.



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