



## Product Change Notification (PCN)

PCN Number: PCN014

ECO Number: NA

Date: 29-Nov-16

Subject of Change: Change in method for storing chip and lot ID in each IC's OTP.

Products Affected:

- DW1000 IC
- DWM1000
- EVK1000
- TREK1000
- Decawave Software
- Decawave Documentation

Change Class:

- Class I PCN
- Class II PCN
- Class III

Reason for Change: Adoption of an ID scheme which allow for the assigning of unique chip ID's across multiple test sites.

### Description of Change:

Existing scheme:

The lot ID is a unique 7 digit number with the first digit identifying the test location, which is blown into OTP address 0x007.

The chip ID is a 6 digit number which is simply a counter of passing devices coming off the tester i.e. first passing device will be assigned 000001, 2nd 000002 etc.

New Scheme:

Decawave tests IC's at a number of test locations and we need to ensure that the method for writing the lot and chip ID is the same at all locations.

The lot ID written to the OTP, address 0x007, will match the core foundry lot ID as identified on the package marking, line 4. By core foundry lot ID we mean 6 characters, the first identifying the foundry, N in our case, and 5 alpha or numeric excluding any numbers after the full stop. As Decawave IC's are only produced in one foundry we do not need to store this first character N as it is common to all lots. The alpha characters will be matched to numbers and then converted to Hex and Binary before being written to the OTP. Each character is assigned 6 bits. The first bit identifies if the character is alpha or numeric, the remaining 5 bits identifying the character. This conversion is outlined in fig 1.

As an example, Fig 2 shows the conversion and OTP writes for the fab lot number N05W74. The green blocks signify unused bits.

In addition to the lot ID, we will also identify each device which passes the production test. This will allow for a high level of traceability when working on customer RMA's. At the end of the test program, passing IC's will be assigned a chip ID of the following structure \$DDDHMMSS i.e. \$ = loadboard test site (0-3 for quad site), DDD = day of the year, 0-365, HH = hour (24 hour), MM = minute, SS = second. This chip ID will be written to address 0x006. Again the table in Fig 1 will be used to convert the numbers and as an example Fig 3 shows the conversion and OTP writes for the IC ID 3365235959.

Fab lots will be built and shipped in their entirety to a particular test location and so there will be no possibility of the same fab lot being tested at two different locations. Thus by adopting the scheme described we are assured that all IC's are identified uniquely.

**This change is effective for all lots tested from 01-Jan-2017**

<b>Prepared by:</b>	Andrew Flynn	<b>Date:</b>	29-Nov-16
<b>Checked by:</b>	Gerry O'Grady	<b>Date:</b>	29-Nov-16
<b>Approved by</b>	William McFadden	<b>Date:</b>	29-Nov-16



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Alpha	Numeric	Hex	Binary
a	0	0	0
b	1	1	1
c	2	2	10
d	3	3	11
e	4	4	100
f	5	5	101
g	6	6	110
h	7	7	111
i	8	8	1000
j	9	9	1001
k	10	A	1010
l	11	B	1011
m	12	C	1100
n	13	D	1101
o	14	E	1110
p	15	F	1111
q	16	10	10000
r	17	11	10001
s	18	12	10010
t	19	13	10011
u	20	14	10100
v	21	15	10101
w	22	16	10110
x	23	17	10111
y	24	18	11000
z	25	19	11001
	26	1A	11010
	27	1B	11011
	28	1C	11100
	29	1D	11101
	30	1E	11110
	31	1F	11111
	.	.	.
	.	.	.
	.	.	.
	.	.	.
	59	3B	111011
	.	.	.
	.	.	.
	.	.	.
	.	.	.
	365	16D	101101101

Fig 1



# Product Change Notification (PCN)

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NVM address 0x007

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1	1	0	0	0	0	1	1	1	0	0	0	1	0	0
A/N	0					A/N	5					A/N	W					A/N	7					A/N	4						

Fig 2

NVM address 0x006

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	0	1	1	0	1	1	0	1	0	1	0	1	1	1	0	1	1	1	0	1	1	0	1	1	1	0	1	1
3	365					23					59					59															

Fig 3