TS3USBCA4 USB Type-C SBU Multiplexer

1 Features

- USB Type-C™ 4:1 (TS3USBCA420) and 3:1 (TS3USBCA410) multiplexer (MUX) for analog audio MIC/AGND, DisplayPort AUX, and other signals
- General purpose MUX for 0 to 3.6 V differential or single-ended signals
- Ultra low R_{ON} of 60 mΩ for the AGND connections for low crosstalk performance
- Low Total Harmonic Distortion (THD)
- High bandwidth channels up to 500 MHz
- Supports both pin and I^2C configuration
- Supports operation from either 3.3-V ±10% regulated supply, or 2.4 to 5.5 V battery
- Industrial temperature range: –40ºC to 85ºC TS3USBCA420I and TS3USBCA410I
- Commercial temperature range: 0ºC to 70ºC TS3USBCA420 and TS3USBCA410
- 1.8 mm x 2.6 mm, 16-pin, 0.4 mm pitch QFN package

2 Applications

- Tablets
- Notebooks
- Desktops
- Gaming consoles
- VR modules
- Smartphones
- Monitors

3 Description

The TS3USBCA4 is a passive 4:1 (TS3USBCA420) and 3:1 (TS3USBCA410) MUX supporting various types of differential or single-ended signals on the SBU1/SBU2 terminals of a USB Type-C connector to different interfaces. Those signals can be differential DisplayPort auxiliary (AUX), analog audio MIC and AGND, PCIe differential clock, or any other supported generic differential or single-ended signals.

The audio path features ultra-low ON-state resistance (R_{ON}), low crosstalk and excellent total harmonic distortion (THD). The break-before-make feature prevents signal distortion during signal transfer from one channel to another. The high-speed paths support bandwidth as high as 500 MHz to provide adequate support for DisplayPort AUX, PCIe clock, and other similar signals. Together with low power consumption, these features make this device suitable for portable audio applications.

The TS3USBCA4 wide supply range from 2.4 V to 5.5 V gives users the flexibility of powering it from a single-cell battery, a 3.3-V regulator, or VBUS. It also provides options for both commercial and industrial temperature ranges.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3USBCA4	UQFN (16)	1.80 mm × 2.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

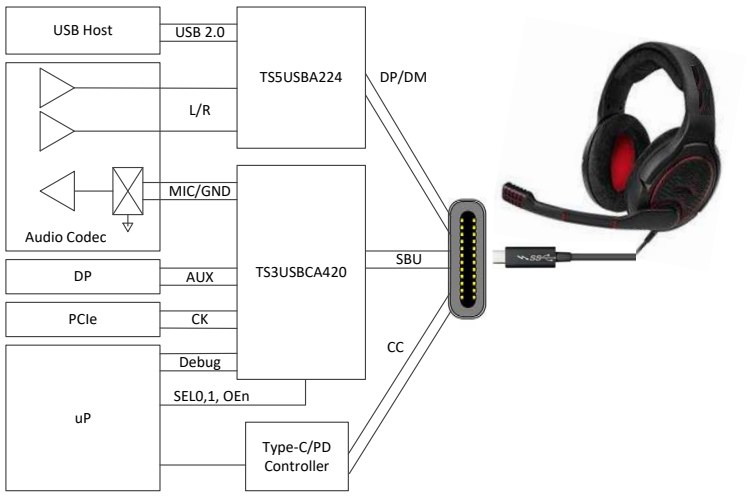


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics (3 V ≤ V_{CC} ≤ 3.6 V) ... 5
6.6 Electrical Characteristics (2.4 V ≤ V_{CC} ≤ 5.5 V) ... 7
6.7 Switching Characteristics (2.4 V ≤ V_{CC} ≤ 5.5 V) ... 9
6.8 Timing Requirements (3 V ≤ V_{CC} ≤ 3.6 V) ... 10
6.9 Timing Requirements (2.4 V ≤ V_{CC} ≤ 5.5 V) ... 10
6.10 Timing Diagrams ... 12
6.11 Typical Characteristics ... 13
7 Parameter Measurement Information ... 14
8 Detailed Description ... 24
8.1 Overview ... 24
8.2 Functional Block Diagram ... 24
8.3 Feature Description ... 25
8.4 Device Functional Modes ... 26
8.5 Programming ... 28
8.6 Register Maps ... 29
9 Application and Implementation ... 31
9.1 Application Information ... 31
9.2 Typical Application ... 31
10 Power Supply Recommendations ... 34
11 Layout ... 35
11.1 Layout Guidelines ... 35
11.2 Layout Example ... 35
12 Device and Documentation Support ... 36
12.1 Receiving Notification of Documentation Updates 36
12.2 Support Resources ... 36
12.3 Trademarks ... 36
12.4 Electrostatic Discharge Caution ... 36
12.5 Glossary ... 36
13 Mechanical, Packaging, and Orderable Information ... 36

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2019) to Revision C — **Page**

- Changed description for LaAp pin From: "as a negative polarity" To "as a positive polarity". ... 4

Changes from Revision A (August 2018) to Revision B — **Page**

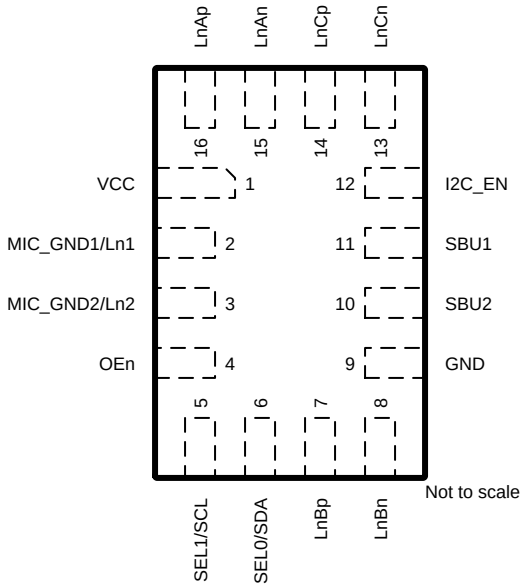
- Changed the I2C_EN pin Description From: This pin has an internal weak pull-up. To: This pin has an internal weak pull-down. ... 3

Changes from Original (February 2018) to Revision A — **Page**

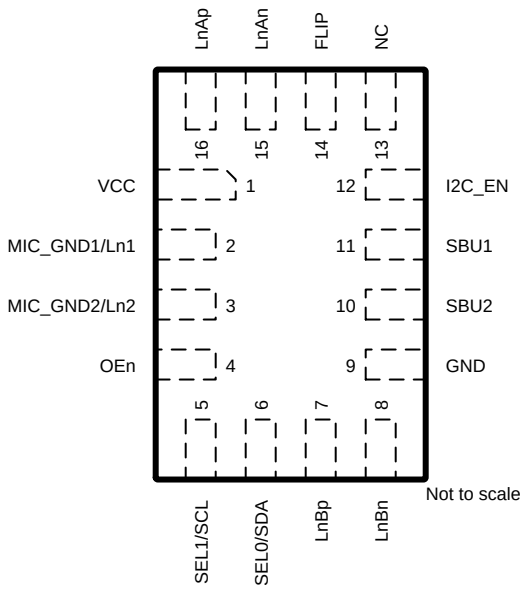
- Changed the device From: *Advanced Information* To: *Production data* ... 1

5 Pin Configuration and Functions

UQFN Package for TS3USBCA420
16-Pin (RSV)
Top View



UQFN Package for TS3USBCA410
16-Pin (RSV)
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TS3USBCA420	TS3USBCA410		
VCC	1	1	P	Power supply. External decoupling capacitors are required close to this pin.
MIC_GND1/Ln1	2	2	I/O, CMOS	Analog audio MIC/AGND signal connection to audio codec. This pin can also function as a general purpose I/O.
MIC_GND2/Ln2	3	3	I/O, CMOS	Analog audio MIC/AGND signal connection to audio codec. This pin can also function as a general purpose I/O.
OEn	4	4	2 Level I	Output Enable: L: Normal Operation H: Standby Mode, I^2C registers reset (Default) This pin has an internal weak pull-up.
SEL1/SCL	5	5	2 Level I (Failsafe)	In Pin Configuration Mode (I2C_EN = L), this pin functions as SEL1 which is used along with SEL0 pin to select switch configurations (Refer to Table 2). This pin has an internal weak pull-down. In I^2C Mode (I2C_EN = M or H), this pin functions as SCL pin for I^2C clock. When used for I^2C clock, pull it up to V_{I2C} with a resistor between 0.62 kΩ and 2.2 kΩ.
SEL0/SDA	6	6	2 Level I/O (Failsafe)	In Pin Configuration Mode (I2C_EN = L), this pin functions as SEL0 which is used along with SEL1 pin to select switch configurations (Refer to Table 2). This pin has an internal weak pull-down. In I^2C Mode (I2C_EN = M or H), this pin functions as SDA pin for I^2C data. When used for I^2C data, pull it up to V_{I2C} with a resistor between 0.62 kΩ and 2.2 kΩ.
LnBp	7	7	I/O, CMOS	This pin can be used in single-ended format or as a positive polarity differential pair partner to pin LnBn. It can be used for connection to any generic I/O signals such as for DisplayPort AUX, PCI Express clock, I^2C, UART, and debug interfaces.
LnBn	8	8	I/O, CMOS	This pin can be used in single-ended format or as a negative polarity differential pair partner to pin LnBp. It can be used for connection to any generic I/O signals such as for DisplayPort AUX, PCI Express clock, I^2C, UART, and debug interfaces.
GND	9	9	G	Primary ground connection for the TS3USBCA4. Must be connected to system ground.
SBU2	10	10	I/O, CMOS (Failsafe)	This pin should be DC coupled to the SBU2 pin of the Type-C receptacle. This pin has an internal nominally 1.6-MΩ pull-down resistor.
SBU1	11	11	I/O, CMOS (Failsafe)	This pin should be DC coupled to the SBU1 pin of the Type-C receptacle. This pin has an internal nominally 1.6-MΩ pull-down resistor.
I2C_EN	12	12	3 Level I	This pin enables I^2C Mode and sets I^2C mode addresses (Refer to Table 5) depending on the pin level defined in Table 1. L: Pin Configuration Mode M: I^2C Mode enabled with I^2C address ADDR0 H: I^2C Mode enabled with I^2C address ADDR1 This pin has an internal weak pull-down.

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	TS3USBCA420	TS3USBCA410		
LnCn	13		I/O, CMOS	This pin can be used in single-ended format or as a negative polarity differential pair partner to pin LnCp. It can be used for connection to any generic I/O signals such as for DisplayPort AUX, PCI Express clock, I^2C, UART, and debug interfaces.
LnCp	14		I/O, CMOS	This pin can be used in single-ended format or as a positive polarity differential pair partner to pin LnCn. It can be used for connection to any generic I/O signals such as for DisplayPort AUX, PCI Express clock, I^2C, UART, and debug interfaces.
NC		13		Not connected.
FLIP		14	I/O, CMOS	This pin flips the switches based on type-C plug orientation in pin configuration mode (I2C_EN=L). L: Normal orientation. H: Flipped orientation. This pin has an internal weak pull-down.
LnAn	15	15	I/O, CMOS	This pin can be used in single-ended format or as a negative polarity differential pair partner to pin LnAp. This pin is preferred for connection to DisplayPort AUX. It can also be used for connection to any generic I/O signals such as for PCI Express clock, I^2C, UART, and debug interfaces.
LnAp	16	16	I/O, CMOS	This pin can be used in single-ended format or as a positive polarity differential pair partner to pin LnAn. This pin is preferred for connection to DisplayPort AUX. It can also be used for connection to any generic I/O signals such as for PCI Express clock, I^2C, UART, and debug interfaces.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted.(1)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage Range (2)	-0.5	6	V
V_{IN_DIFF}	Differential Voltage at Differential Inputs	-4	4	V
V_{IN_SE}	Input Voltage at Differential Inputs (2)	-0.5	6	V
V_{IN_CMOS}	Input Voltage at CMOS Inputs other than SBU1/SBU2 Pins (2)	-0.5	6	V
V_{IN_SBU}	Input Voltage at SBU1/SBU2 Input-output Pins (2)	-0.5	6	V
T_J	Junction Temperature		105	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminal.

6.2 ESD Ratings

PARAMETER			VALUE	UNIT
V_{HBM}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
V_{CDM}	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range unless otherwise noted.

		MIN	NOM	MAX	UNIT
T_A	Ambient temperature for TS3USBCA410 and TS3USBCA420	0		70	°C
T_A	Ambient temperature for TS3USBCA410I and TS3USBCA420I	-40		85	°C
V_{CC}	Supply voltage	2.4	5.0	5.5	V
V_{I2C}	Supply that external resistors on SDA and SCL are pulled up too	1.7		3.6	V
V_{I/O_DIFF}	Differential Input-output Voltage	0		1.8	V
V_{PSN}	Power supply noise			100	mV

6.4 Thermal Information

THERMAL METRIC		TS3USBCA4 RSV (R-PUQFN-N16) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	107.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (2)	41.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (3)	43.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter (4)	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (5)	43.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance (6)	N/A	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψJT, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θJA, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψJB, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θJA, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics ($3\ V \le V_{CC} \le 3.6\ V$)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 3.0 V/3.6 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
I_{CC}	Supply Current	OEn = L, DEVICE_ENABLE = 1		45	70	µA
I_{OFF_I2C}	Device Shutdown Current	OEn = L, DEVICE_ENABLE = 0		17	30	µA
I_{OFF_OEN}	Device Shutdown Current	OEn = 3.6 V		0.05	3.5	µA
	Device Shutdown Current	OEn = 1.4 V		4	12	µA
SEL0, SEL1						
V_{IH}	Input-high voltage		1.4			V
V_{IL}	Input-low voltage				0.4	V
I_{IH}	Input-high current	$V_{IN} = V_{CC}$			2.5	µA
I_{IL}	Input-low current	V_{IN} = 0 V			1	µA
R_{PD}	Pull-down resistor		1.6	3.0	5.8	MΩ
FLIP						
V_{IH}	Input-high voltage		1.4			V
V_{IL}	Input-low voltage				0.4	V
I_{IH}	Input-high current	$V_{IN} = V_{CC}$			2.5	µA
I_{IL}	Input-low current	V_{IN} = 0 V			1	µA
R_{PD}	Pull-down resistor		1.6	3	5.8	MΩ
OEn						
V_{IH}	Input-high voltage		1.4			V
V_{IL}	Input-low voltage				0.4	V
I_{IH}	Input-high current	$V_{IN}=V_{CC}$			0.6	µA
I_{IL}	Input-low current	V_{IN}=0 V			6	µA
R_{PU}	Pull-up resistor		0.6	1.1	2.5	MΩ
I2C_EN						
V_{IH}	Input-high voltage		0.85			V_{CC}

Electrical Characteristics (3 V ≤ V_{CC} ≤ 3.6 V) (continued)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 3.0 V/3.6 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IMH}	Upper bound of mid-level input voltage. Higher input may be intepreted as logic HIGH.		0.6			V_{CC}
V_{IML}	Lower bound of mid-level input voltage. Lower input may be intepreted as logic LOW.				0.4	V_{CC}
V_{IL}	Input-low voltage				0.15	V_{CC}
I_{IH}	Input-high current				2.5	µA
I_{IM}	Mid-level input current				1.2	µA
I_{IL}	Input-low current				1	µA
R_{PD}	Pull-down resistor		1.6	3.0	5.8	MΩ
I^2C Control Pins SCL, SDA						
V_{IH_I2C}	High-level input voltage	I^2C mode	1.3		V_{I2C}	V
V_{IL_I2C}	Low-level input voltage	I^2C mode	0		0.5	V
V_{OL_I2C}	Low-level output voltage	I^2C mode; I_{OL_I2C} = 3 mA	0		0.4	V
I_{OL_I2C}	Low-level output current	I^2C mode; V_{OL_I2C} = 0.4 V	6			mA
I_{I_I2C}	Input current on SDA pin	0.1*V_{I2C} < Input voltage < 3.6 V	-5		5	µA
C_{I_I2C}	Input capacitance		0.5		10	pF
$C_{(I2C\_FM\_BUS)}$	I^2C bus capacitance for FM (400 kHz)				150	pF
$R_{(EXT\_I2C\_FM)}$	External pull up resistors on both SDA and SCL for FM (400 kHz)	$C_{(I2C\_FM\_BUS)}$ = 150 pF	620	1500	2200	Ω
SBU1, SBU2						
C_{SBU_HS}	Single-ended capacitance at 500MHz looking into SBU pin	V_{IN} = 0 V, outputs open, high-speed path enabled	4	11	13	pF
C_{SBU_AUDIO}	Single-ended capacitance at 500MHz looking into SBU pin	V_{IN} = 0 V, outputs open, audio path enabled; T_A = 25°C; V_{CC} = 3.3 V	8	10	14	pF
C_{SBU_OFF}	Single-ended capacitance at 500MHz looking into SBU pin	V_{IN} = 0 V, outputs open, OEn=H; T_A = 25°C; V_{CC} = 3.3 V	11	14	17	pF
R_{PD}	Pull-down resistor		0.8	1.6	3.3	MΩ
LnA, LnB, LnC: HIGH-SPEED PATH						
V_{I_HS}	Single-ended HS input voltage		-0.3		3.6	V
C_{HS_ON}	Single-ended capacitance at 500 MHz looking into HS pins	V_{IN} = 0 V, outputs open, high-speed path enabled		8.5	10.5	pF
C_{HS_AUDIO}	Single-ended capacitance at 500 MHz looking into HS pins	V_{IN} = 0 V, outputs open, audio path enabled; T_A = 25°C; V_{CC} = 3.3 V		1.7	2	pF
C_{HS_OFF}	Single-ended capacitance at 500 MHz looking into HS pins	V_{IN} = 0 V, outputs open, OEn=H; T_A = 25°C; V_{CC} = 3.3 V		1.7	2	pF
R_{ON_HS}	ON resistance	V_{IN} = 0 V, I_O = -40 mA		4.9	7.1	Ω
ΔR_{ON_HS}	ON resistance match between pairs of the same channel	V_{IN} ≤ 0 V, I_O = -40 mA			0.5	Ω
$R_{ON\_FLAT\_HS}$	ON resistance flatness ($R_{ON\_HS(MAX)}$ - $R_{ON\_HS(MIN)}$)	0 V ≤ V_{IN} ≤ 3.6 V, I_O = -40 mA		1.35		Ω
BW_{HS}	-3-dB bandwidth	R_L = 50 Ω, V_{IN} = 0 V, MIC_GND1 pin open, MIC_GND1 pin open; T_A = 25°C; V_{CC} = 3.3 V	460	510	550	MHz
RJ_{HS}	Additive random jitter	R_L = 50 Ω, 10 kHz to 20 MHz offset, f = 100 MHz; T_A = 25°C; V_{CC} = 3.3 V		0.012		ps-RMS
MIC_GND1, MIC_GND2: AUDIO PATH						
V_{I_MIC}	MIC input voltage		-0.3		3.6	V

Electrical Characteristics (3 V ≤ V_{CC} ≤ 3.6 V) (continued)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 3.0 V/3.6 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{AUDIO_ON}	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V_{IN} = 0 V, outputs open, audio path enabled; T_A = 25°C; V_{CC} = 3.3 V		9.5	12	pF
C_{AUDIO_HS}	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V_{IN} = 0 V, outputs open, high-speed path enabled; T_A = 25°C; V_{CC} = 3.3 V		11.5	16	pF
C_{AUDIO_OFF}	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V_{IN} = 0 V, outputs open, OEn=H; T_A = 25°C; V_{CC} = 3.3 V		12.5	14.5	pF
R_{ON_AUDIO}	ON resistance for AUDIO path	V_{IN} = 0 V, I_O = -75 mA		50	80	mΩ
BW_{AUDIO}	-3-dB bandwidth	R_L = 50 Ω, V_{IN} = 0 V; T_A = 25°C; V_{CC} = 3.3 V	580	630	700	MHz
PSR_{217}	Power supply rejection	R_L = 50 Ω, V_{IN} = 3.3 V ± 200 mV_{PP}, f = 217 Hz		-105	-100	dB
PSR_{1K}		R_L = 50 Ω, V_{IN} = 3.3 V ± 200 mV_{PP}, f = 1 kHz		-96	-92	dB
PSR_{20K}		R_L = 50 Ω, V_{IN} = 3.3 V ± 200 mV_{PP}, f = 20 kHz		-85	-81	dB
THD_{200_MIC}	Total harmonic distortion	R_S=600Ω, R_L=600Ω, V_{IN}=1.8V±200mV_{PP}, f=20Hz~20kHz; T_A = 25°C; V_{CC} = 3.3 V		0.006		%
THD_{500_MIC}	Total harmonic distortion	R_S=600Ω, R_L=600Ω, V_{IN}=1.8V±500mV_{PP}, f=20Hz~20kHz; T_A = 25°C; V_{CC} = 3.3 V		0.003		%
X_{TALK_MICGND}	Crosstalk between MIC and AGND	V_{IN} = 200 mV_{PP}, f = 20 Hz – 20 kHz, R_L = 50 Ω; T_A = 25°C;		-110	-90	dB
ISO_{OFF_MICGND}	OFF isolation	V_{IN} = 200 mV_{PP}, f = 20 Hz – 20 kHz, R_L = 50 Ω; T_A = 25°C;		-73	-67	dB

6.6 Electrical Characteristics (2.4 V ≤ V_{CC} ≤ 5.5 V)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
I_{CC}	Supply Current	OEn = L, DEVICE_ENABLE = 1		45	75	µA
I_{OFF_I2C}	Device Shutdown Current	OEn = L, DEVICE_ENABLE = 0		17	40	µA
I_{OFF_OEN}	Device Shutdown Current	OEn = 3.6 V		0.05	5.5	µA
	Device Shutdown Current	OEn = 1.4 V		4	80	µA
SEL0, SEL1						
V_{IH}	Input-high voltage		1.4			V
V_{IL}	Input-low voltage				0.4	V
I_{IH}	Input-high current	V_{IN} = V_{CC}			3.5	µA
I_{IL}	Input-low current	V_{IN} = 0 V			1	µA
R_{PD}	Pull-down resistor		1.6	3.0	5.8	MΩ
FLIP						
V_{IH}	Input-high voltage		1.4			V
V_{IL}	Input-low voltage				0.4	V
I_{IH}	Input-high current	V_{IN} = V_{CC}			3.5	µA
I_{IL}	Input-low current	V_{IN} = 0 V			1	µA
R_{PD}	Pull-down resistor		1.6	3.0	5.8	MΩ
OEn						
V_{IH}	Input-high voltage		1.5			V

Electrical Characteristics (2.4 V ≤ V_{CC} ≤ 5.5 V) (continued)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input-low voltage				0.4	V
I_{IH}	Input-high current	V_{IN}=V_{CC}			1	µA
I_{IL}	Input-low current	V_{IN}=0 V			8	µA
R_{PU}	Pull-up resistor		0.6	1.1	2.5	MΩ
I2C_EN						
V_{IH}	Input-high voltage		0.9			V_{CC}
V_{IMH}	Upper bound of mid-level input voltage. Higher input may be intepreted as logic HIGH.		0.58			V_{CC}
V_{IML}	Lower bound of mid-level input voltage. Lower input may be intepreted as logic LOW.				0.42	V_{CC}
V_{IL}	Input-low voltage				0.14	V_{CC}
I_{IH}	Input-high current				3.5	µA
I_{IM}	Mid-level input current				1.6	µA
I_{IL}	Input-low current				1	µA
R_{PD}	Pull-down resistor		1.6	3.0	5.8	MΩ
I^2C Control Pins SCL, SDA						
V_{IH_I2C}	High-level input voltage	I^2C mode	1.3		V_{I2C}	V
V_{IL_I2C}	Low-level input voltage	I^2C mode	0		0.5	V
V_{OL_I2C}	Low-level output voltage	I^2C mode; I_{OL_I2C} = 3 mA	0		0.4	V
I_{OL_I2C}	Low-level output current	I^2C mode; V_{OL_I2C} = 0.4 V	4			mA
I_{I_I2C}	Input current on SDA pin	0.1*V_{I2C} < Input voltage < 3.6 V	-5		5	µA
C_{I_I2C}	Input capacitance		0.5		10	pF
$C_{(I2C\_FM\_BUS)}$	I^2C bus capacitance for FM (400 kHz)				150	pF
$R_{(EXT\_I2C\_FM)}$	External pull up resistors on both SDA and SCL for FM (400 kHz)	$C_{(I2C\_FM\_BUS)}$ = 150 pF	620	1500	2200	Ω
SBU1, SBU2						
C_{SBU_HS}	Single-ended capacitance at 500MHz looking into SBU pin	V_{IN} = 0 V, outputs open, high-speed path enabled	4	11	13	pF
C_{SBU_AUDIO}	Single-ended capacitance at 500MHz looking into SBU pin	V_{IN} = 0 V, outputs open, audio path enabled; T_A = 25°C; V_{CC} = 3.3 V	8	10	14	pF
C_{SBU_OFF}	Single-ended capacitance at 500MHz looking into SBU pin	V_{IN} = 0 V, outputs open, OEn=H; T_A = 25°C; V_{CC} = 3.3 V	11	14	17	pF
R_{PD}	Pull-down resistor		0.8	1.6	3.3	MΩ
LnA, LnB, LnC: HIGH-SPEED PATH						
V_{I_HS}	Single-ended HS input voltage		-0.3		3.6	V
C_{HS_ON}	Single-ended capacitance at 500 MHz looking into HS pins	V_{IN} = 0 V, outputs open, high-speed path enabled		8.5	10.5	pF
C_{HS_AUDIO}	Single-ended capacitance at 500 MHz looking into HS pins	V_{IN} = 0 V, outputs open, audio path enabled; T_A = 25°C; V_{CC} = 3.3 V		1.7	2	pF
C_{HS_OFF}	Single-ended capacitance at 500 MHz looking into HS pins	V_{IN} = 0 V, outputs open, OEn=H; T_A = 25°C; V_{CC} = 3.3 V		1.7	2	pF
R_{ON_HS}	ON resistance	V_{IN} = 0 V, I_O = -40 mA		4.9	7.5	Ω
ΔR_{ON_HS}	ON resistance match between pairs of the same channel	V_{IN} ≤ 0 V, I_O = -40 mA			0.65	Ω
$R_{ON\_FLAT\_HS}$	ON resistance flatness ($R_{ON\_HS(MAX)}$ - $R_{ON\_HS(MIN)}$)	0 V ≤ V_{IN} ≤ 3.6 V, I_O = -40 mA		1.35		Ω

Electrical Characteristics (2.4 V ≤ V_{CC} ≤ 5.5 V) (continued)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW_{HS}	-3-dB bandwidth	R_L = 50 Ω, V_{IN} = 0 V; T_A = 25°C; V_{CC} = 3.3 V	450	510	670	MHz
RJ_{HS}	Additive random jitter	R_L = 50 Ω, 10 kHz to 20 MHz offset, f = 100 MHz; T_A = 25°C; V_{CC} = 3.3 V		0.012		ps-RMS
MIC_GND1, MIC_GND2: AUDIO PATH						
V_{I_MIC}	MIC input voltage		-0.3		3.6	V
C_{AUDIO_ON}	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V_{IN} = 0 V, outputs open, audio path enabled; T_A = 25°C; V_{CC} = 3.3 V		9.5	12	pF
C_{AUDIO_HS}	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V_{IN} = 0 V, outputs open, high-speed path enabled; T_A = 25°C; V_{CC} = 3.3 V		11.5	16	pF
C_{AUDIO_OFF}	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V_{IN} = 0 V, outputs open, OEn=H; T_A = 25°C; V_{CC} = 3.3 V		12.5	14.5	pF
R_{ON_AUDIO}	ON resistance for AUDIO path	V_{IN} = 0 V, I_O = -75 mA		50	80	mΩ
BW_{AUDIO}	-3-dB bandwidth	R_L = 50 Ω, V_{IN} = 0 V; T_A = 25°C; V_{CC} = 3.3 V	580	630	720	MHz
PSR_{217}	Power supply rejection	R_L = 50 Ω, V_{IN} = 3.3 V ± 200 mV_{PP}, f = 217 Hz		-105	-96	dB
PSR_{1K}		R_L = 50 Ω, V_{IN} = 3.3 V ± 200 mV_{PP}, f = 1 kHz		-96	-90	dB
PSR_{20K}		R_L = 50 Ω, V_{IN} = 3.3 V ± 200 mV_{PP}, f = 20 kHz		-85	-81	dB
THD_{200_MIC}	Total harmonic distortion	R_S=600Ω, R_L=600Ω, V_{IN}=1.8V±200mV_{PP}, f=20H_Z~20kHz; T_A = 25°C; V_{CC} = 3.3 V		0.006		%
THD_{500_MIC}	Total harmonic distortion	R_S=600Ω, R_L=600Ω, V_{IN}=1.8V±500mV_{PP}, f=20Hz~20kHz; T_A = 25°C; V_{CC} = 3.3 V		0.003		%
X_{TALK_MICGND}	Crosstalk between MIC and AGND	V_{IN} = 200 mV_{PP}, f = 20 Hz – 20 kHz, R_L = 50 Ω; T_A = 25°C;		-110	-90	dB
ISO_{OFF_MICGND}	OFF isolation	V_{IN} = 200 mV_{PP}, f = 20 Hz – 20 kHz, R_L = 50 Ω; T_A = 25°C;		-73	-67	dB

6.7 Switching Characteristics (2.4 V ≤ V_{CC} ≤ 5.5 V)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C						
f_{SCL}	I2C clock frequency				400	kHz
t_{BUF}	Bus free time between START and STOP conditions		1.3			µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated		0.6			µs
t_{LOW}	Low period of the I2C clock		1.3			µs
t_{HIGH}	High period of the I2C clock		0.6			µs
t_{SUSTA}	Setup time for a repeated START condition		0.6			µs
t_{HDDAT}	Data hold time		0			µs
t_{SUDAT}	Data setup time		150			ns
t_R	Rise time of both SDA and SCL signals				300	ns

Switching Characteristics (2.4 V ≤ V_{CC} ≤ 5.5 V) (continued)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_F	Fall time of both SDA and SCL signals		20 × (V_{I2C}/5.5 V)		300	ns
t_{SUSTO}	Setup time for STOP condition		0.6			µs

6.8 Timing Requirements (3 V ≤ V_{CC} ≤ 3.6 V)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 3.0 V/3.6 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{ON_MICGND}	Switch ON time for MIC/AGND path	V_{PU}=1.8V, R_{PU}=2100Ω, C_L=50pF			10	µs
t_{OFF_MICGND}	Switch OFF time for MIC/AGND path	V_{PU}=1.8V, R_{PU}=2100Ω, C_L=50pF			5	µs
t_{ON_HS}	Switch ON time for high-speed path	R_S=50Ω, R_L =50Ω			1.1	µs
t_{OFF_HS}	Switch OFF time for high-speed path	R_S=50Ω, R_L =50Ω			725	ns
t_{BBM}	Break before make off time for MIC/AGND path	V_{PU}=1.8V, R_{PU}=2100Ω, R_L=50Ω, C_L=50pF	1300			ns
t_{FLIP}	Response time for the FLIP pin	R_S=50Ω, R_L=50Ω			1	µs
t_{DEV_ENABLE}	Device enable time from OEn = L to device ready	OEn=L			350	µs
$t_{DEV\_DISABLE}$	Device disable time from OEn = H to device shutdown	OEn=H			175	ns
t_{D_PG}	$V_{CC\ (MIN)}$ to Internal Power Good asserted high (Refer to Figure 1)	OEn=L			250	µs
t_{CFG_DB}	Debounce time for SEL[1:0] and I2C_EN configuration pins (Refer to Figure 1)	OEn=L	150			ns
t_{VCC_RAMP}	V_{CC} power supply (0 – 100%) ramp time requirement (Refer to Figure 1)		0.1		100	ms

6.9 Timing Requirements (2.4 V ≤ V_{CC} ≤ 5.5 V)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{ON_MICGND}	Switch ON time for MIC/AGND path	V_{PU}=1.8V, R_{PU}=2100Ω, C_L=50pF			12	µs
t_{OFF_MICGND}	Switch OFF time for MIC/AGND path	V_{PU}=1.8V, R_{PU}=2100Ω, C_L=50pF			6	µs
t_{ON_HS}	Switch ON time for high-speed path	R_S=50Ω, R_L =50Ω			1.2	µs
t_{OFF_HS}	Switch OFF time for high-speed path	R_S=50Ω, R_L =50Ω			780	ns
t_{BBM}	Break before make off time for MIC/AGND path	V_{PU}=1.8V, R_{PU}=2100Ω, R_L=50Ω, C_L=50pF	1300			ns
t_{FLIP}	Response time for the FLIP pin	R_S=50Ω, R_L=50Ω			1.1	µs
t_{DEV_ENABLE}	Device enable time from OEn = L to device ready	OEn=L			450	µs

Timing Requirements (2.4 V ≤ V_{CC} ≤ 5.5 V) (continued)

All minimum/maximum specifications are at T_A = -40/85°C, V_{CC} = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{DEV\_DISABLE}$	Device disable time from OEn = H to device shutdown	OEn=H			200	ns
t_{D_PG}	$V_{CC\ (MIN)}$ to Internal Power Good asserted high (Refer to Figure 1)	OEn=L			250	µs
t_{CFG_DB}	Debounce time for SEL[1:0] and I2C_EN configuration pins (Refer to Figure 1)	OEn=L	140			ns
t_{VCC_RAMP}	V_{CC} power supply (0 – 100%) ramp time requirement (Refer to Figure 1)		0.1		100	ms

6.10 Timing Diagrams

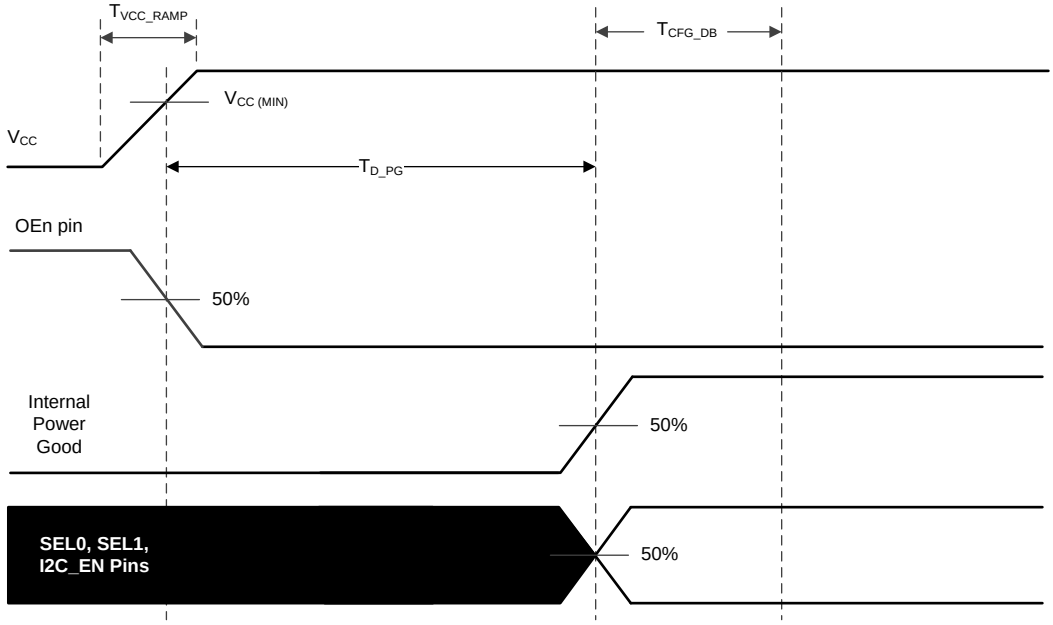


Figure 1. Power-Up Timing

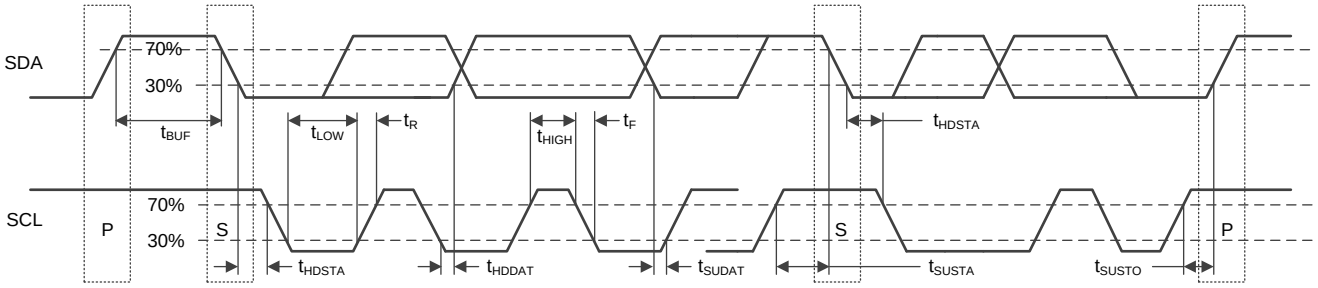


Figure 2. I²C Timing Diagram Definitions

6.11 Typical Characteristics

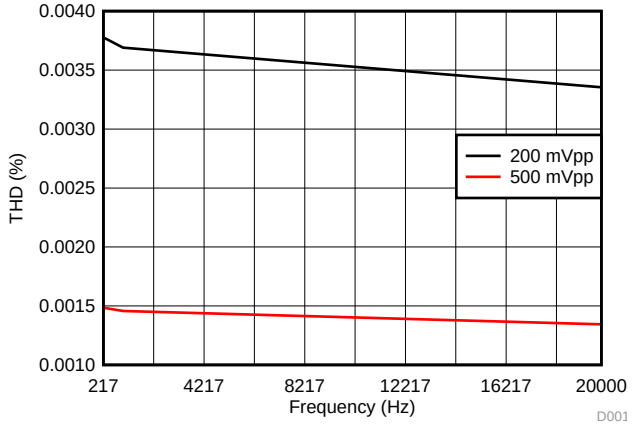


Figure 3. S3PX Total Harmonic Distortion

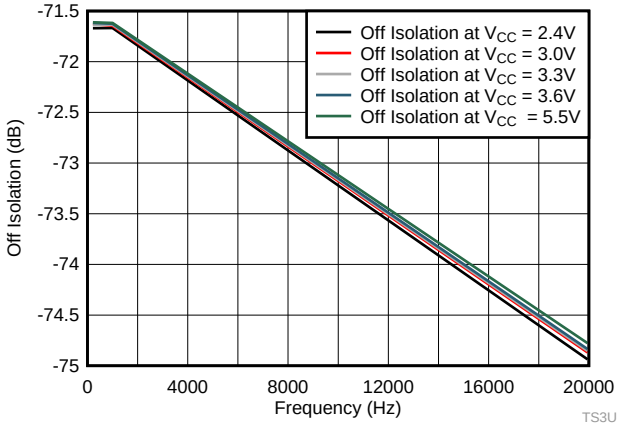


Figure 4. Off Isolation

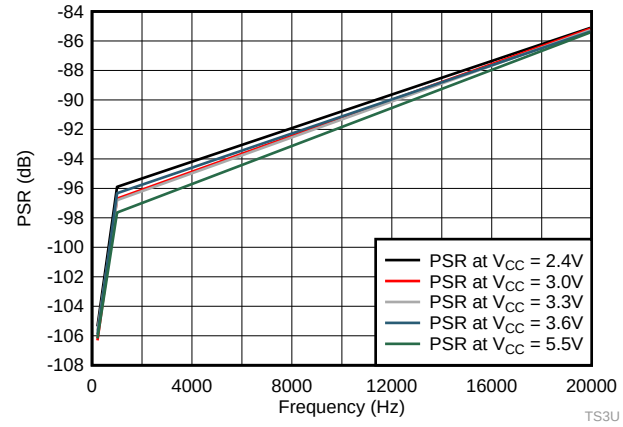


Figure 5. Power Supply Rejection

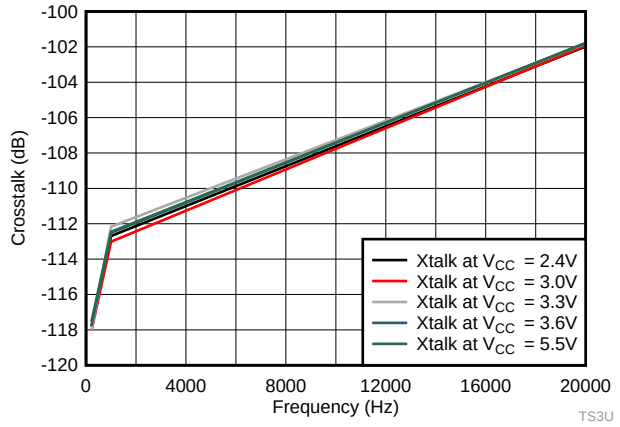


Figure 6. Crosstalk

7 Parameter Measurement Information

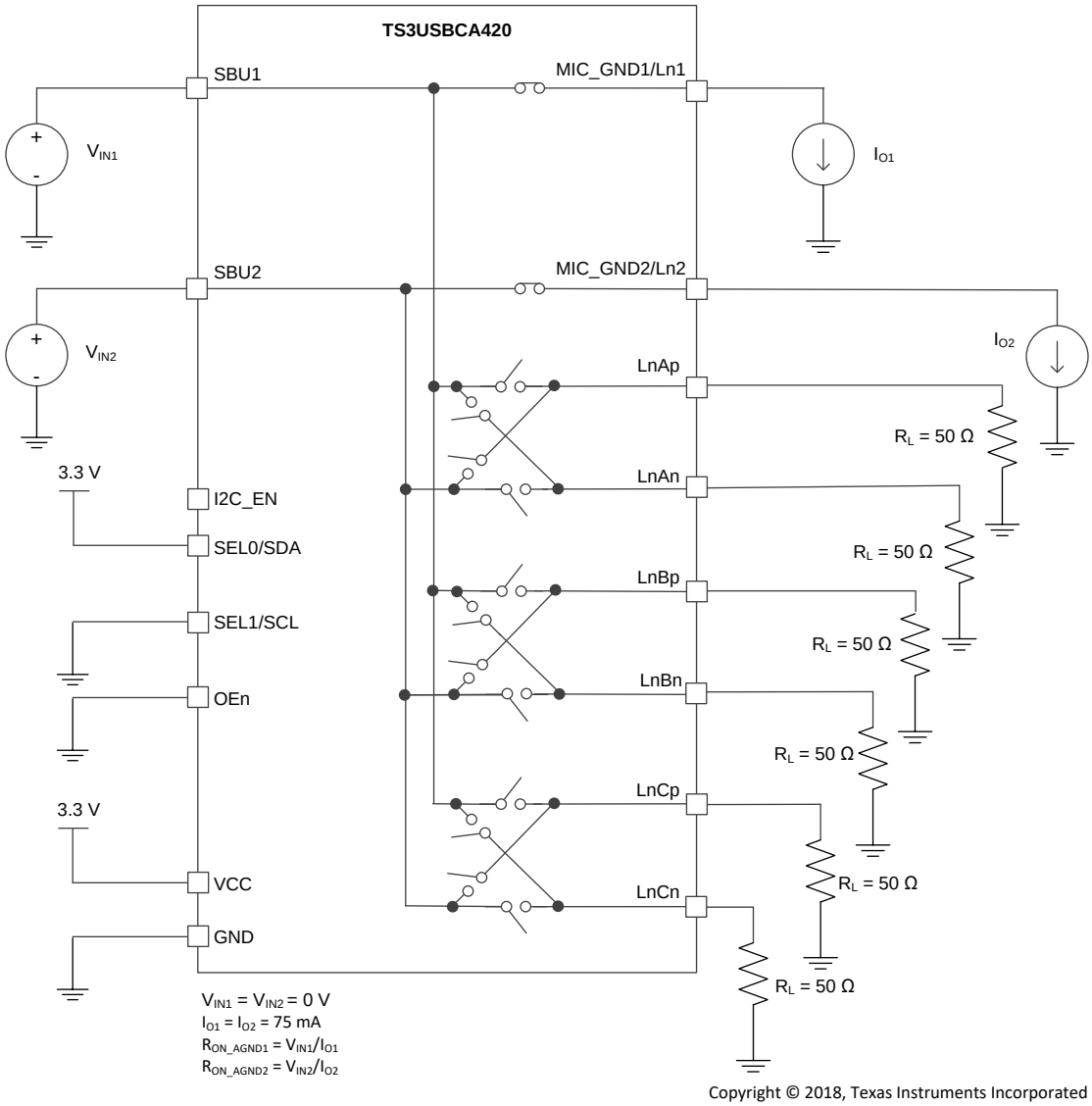


Figure 7. ON-State Resistance for the Analog Audio GND (R_{ON_AGND})

Parameter Measurement Information (continued)

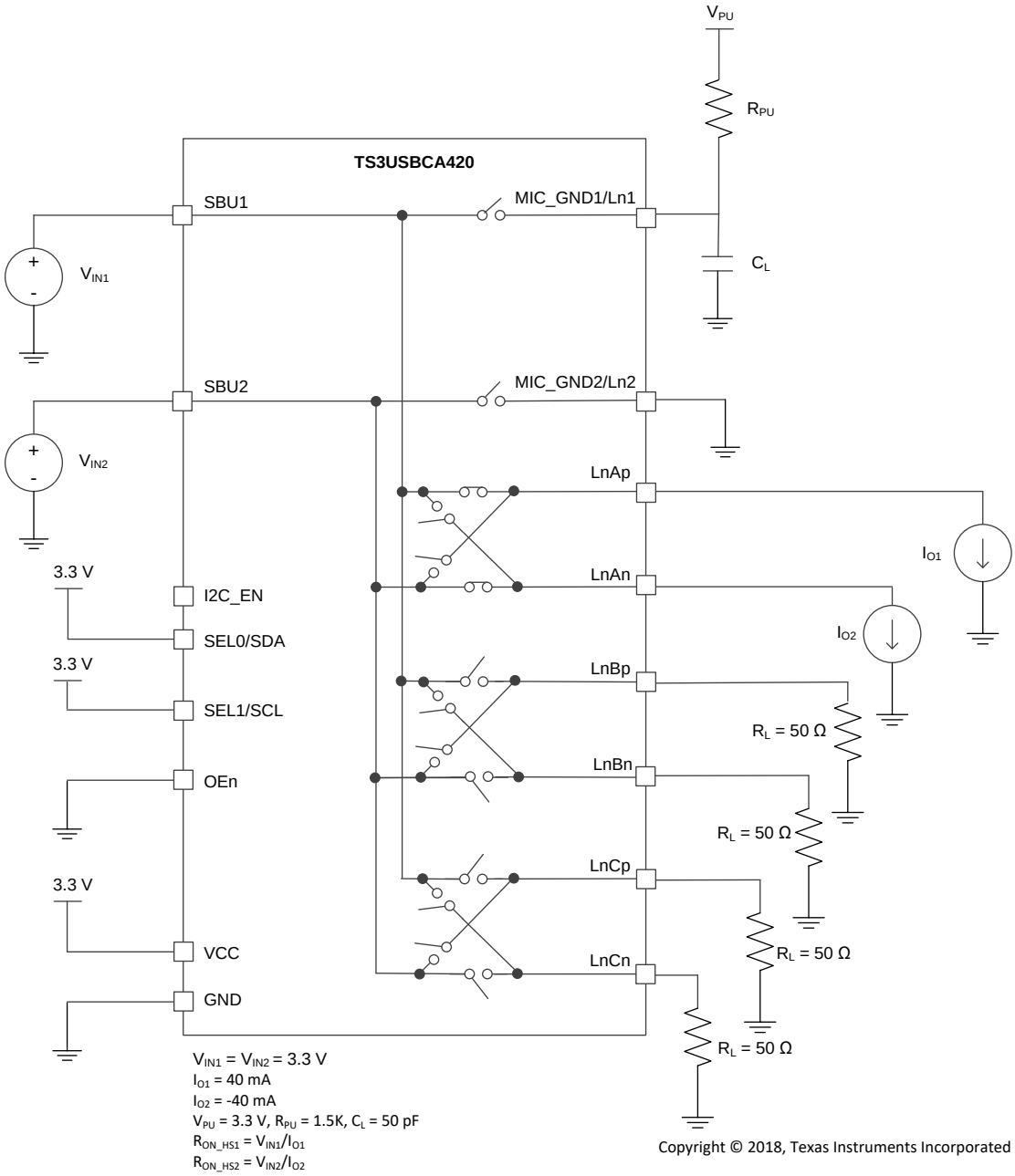


Figure 8. ON-State Resistance for High-Speed Data Paths (R_{ON_HS})

Parameter Measurement Information (continued)

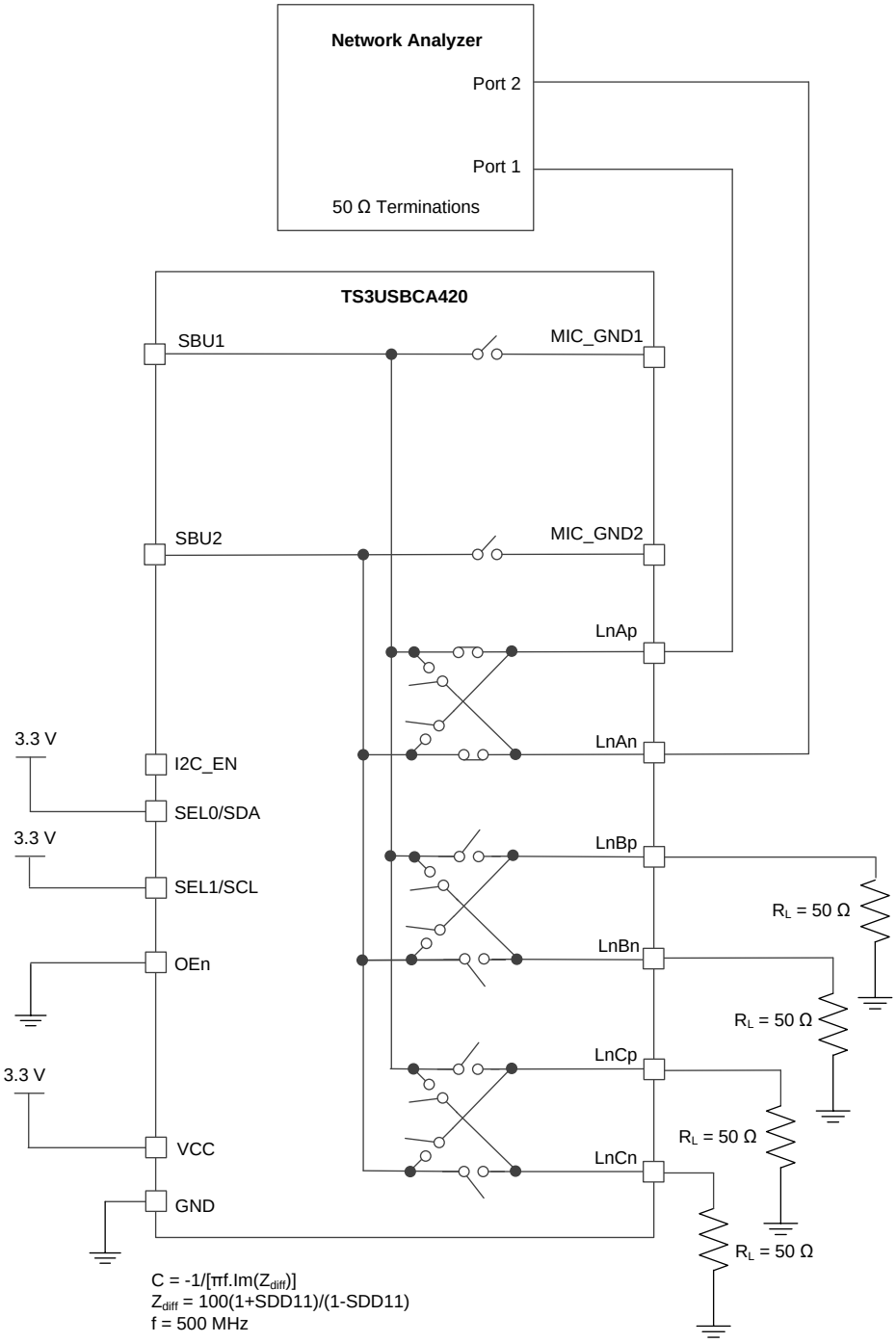


Figure 9. ON-State and OFF-State Output Capacitance for High-Speed Data Paths (C_{ON_HS}, C_{OFF_HS})

Parameter Measurement Information (continued)

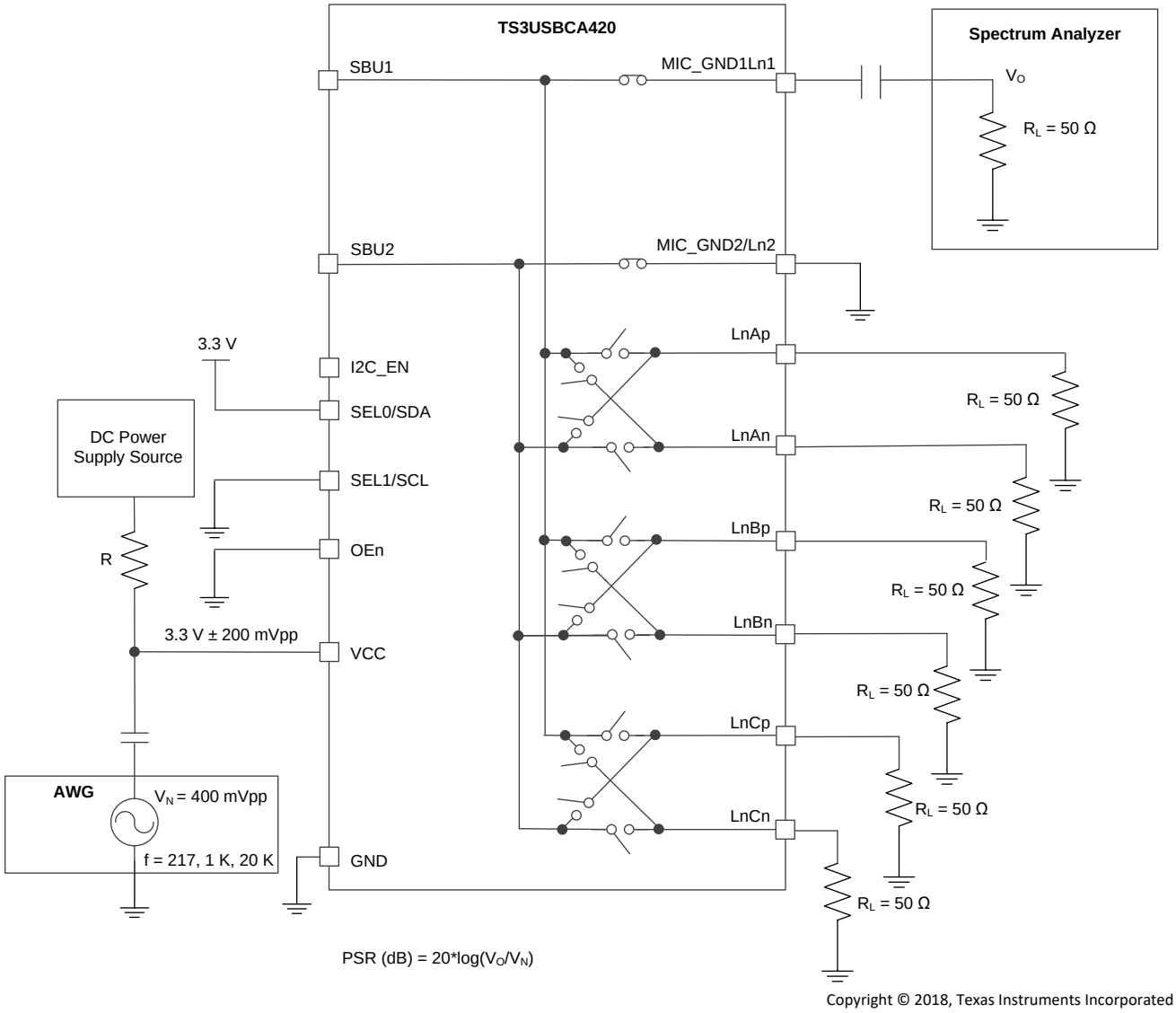


Figure 10. Power Supply Rejection (PSR)

Parameter Measurement Information (continued)

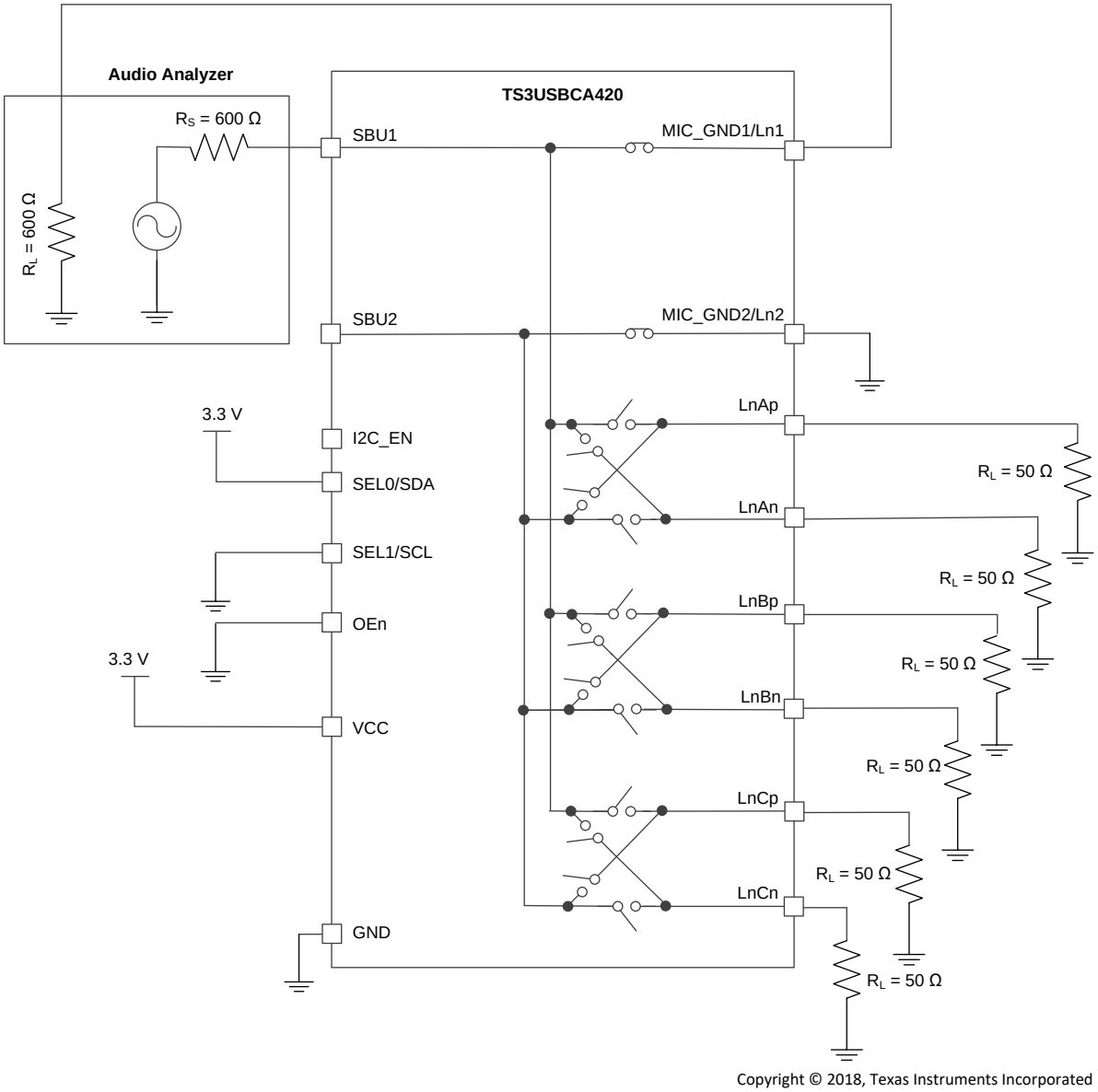


Figure 11. Total Harmonic Distortion (THD)

Parameter Measurement Information (continued)

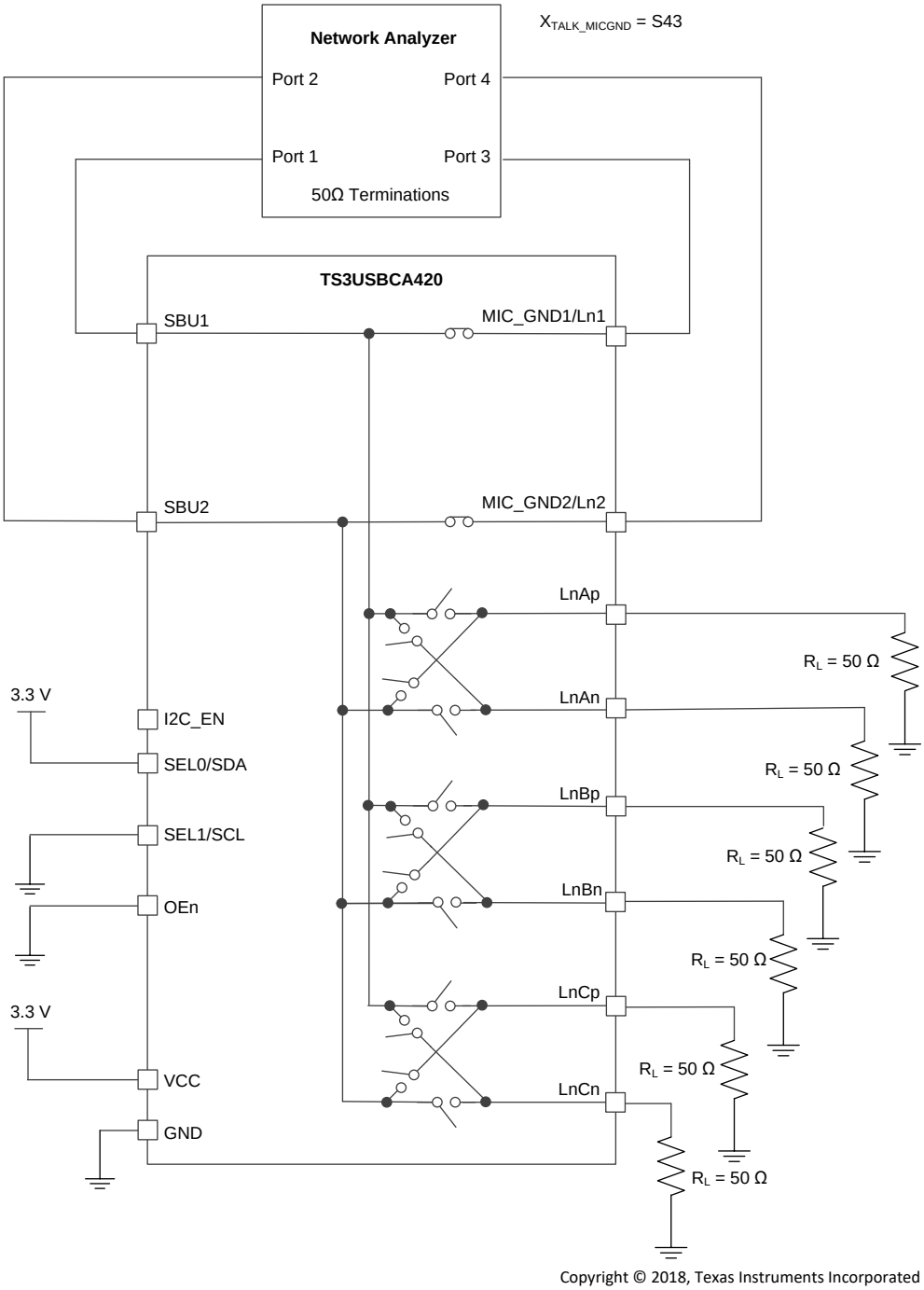


Figure 12. Crosstalk Between MIC and AGND ($XTALK_{MICGND}$)

Parameter Measurement Information (continued)

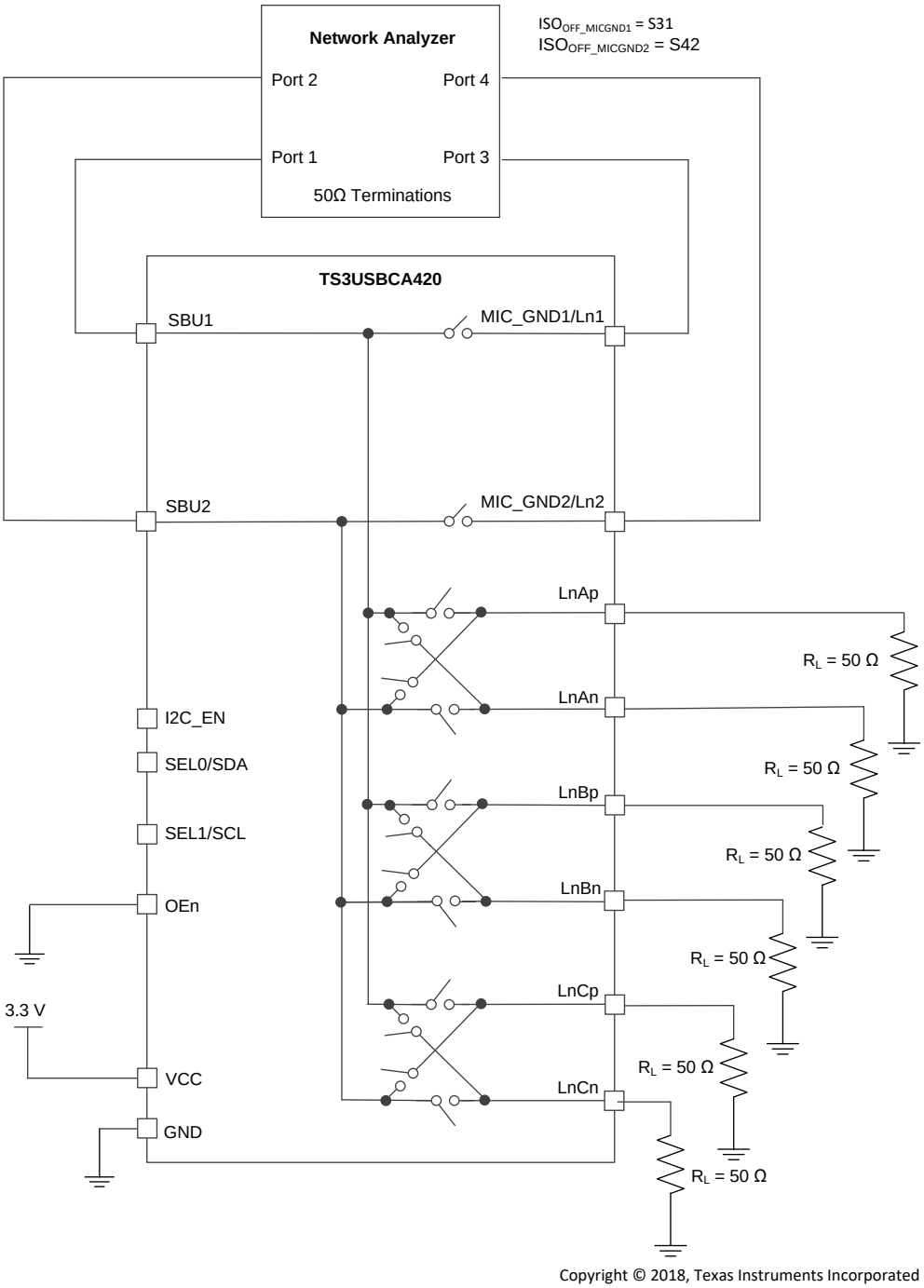


Figure 13. OFF Isolation (ISO_{OFF_MICGND})

Parameter Measurement Information (continued)

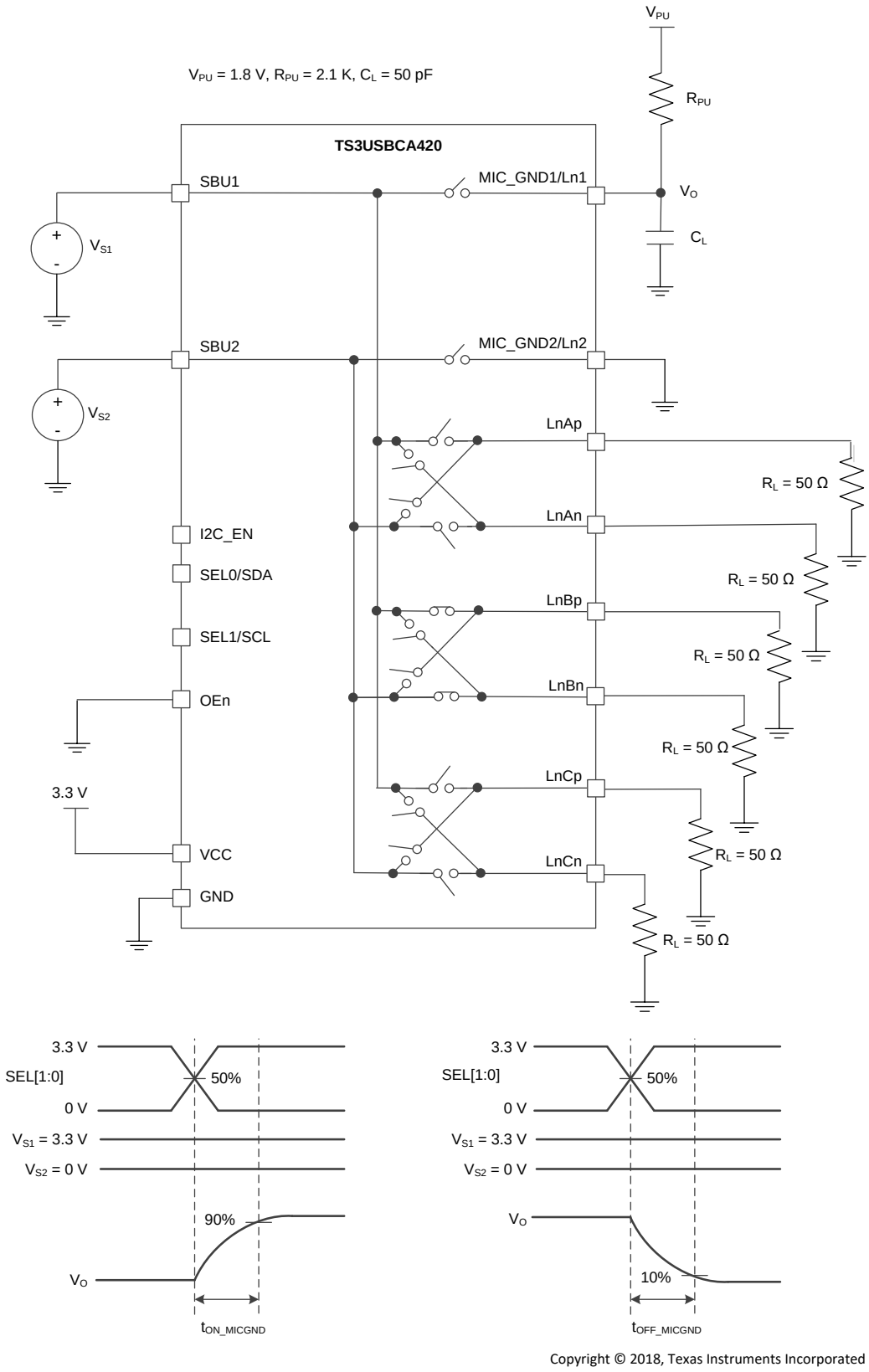


Figure 14. Turn-ON time (t_{ON}) and Turn-OFF time (t_{OFF}) for MIC and AGND

Parameter Measurement Information (continued)

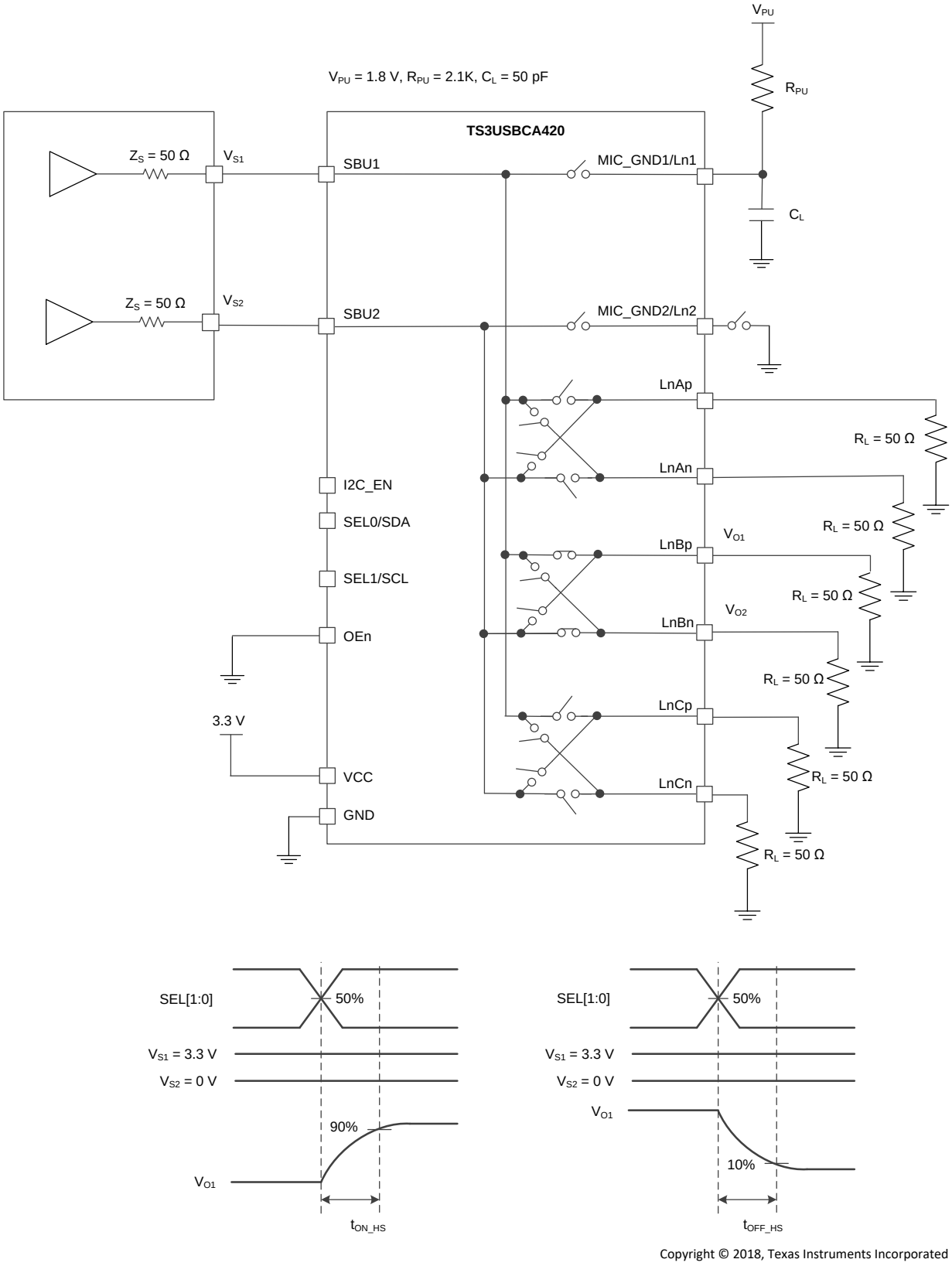


Figure 15. Turn-ON time (t_{ON}) and Turn-OFF time (t_{OFF}) for High-Speed Data Paths

Parameter Measurement Information (continued)

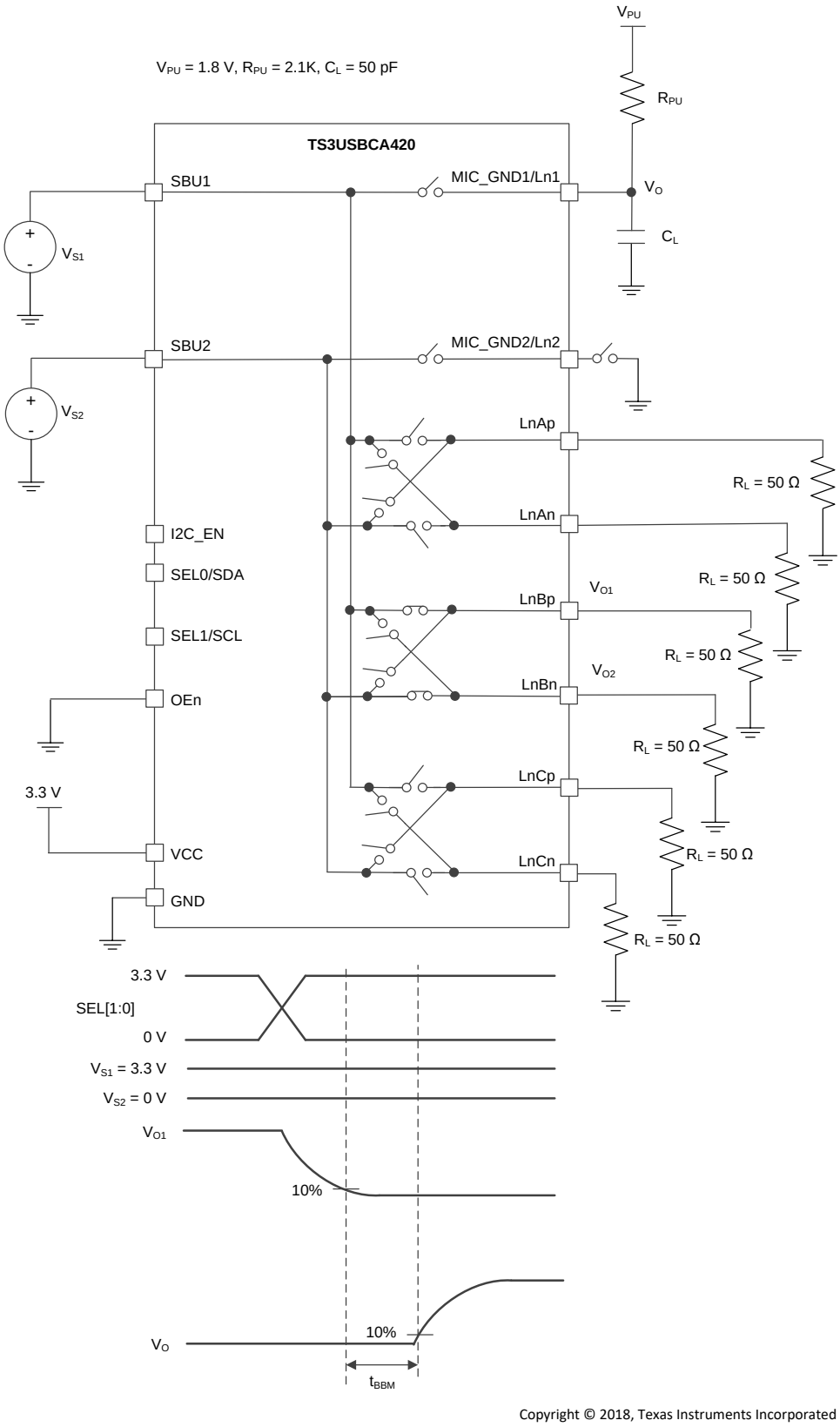


Figure 16. Break-Before-Make Time (t_{BBM})

8 Detailed Description

8.1 Overview

The TS3USBCA4 is a passive 4:1 (TS3USBCA420) and 3:1 (TS3USBCA410) MUX. It supports differential or single-ended signals on the SBU1/SBU2 terminals of a USB Type-C connected to different interfaces. The signals can be DisplayPort auxiliary (AUX), analog audio MIC and AGND, PCIe differential clock, or any other supported generic differential or single-ended signals.

The audio path features ultra-low ON-state resistance (R_{ON}), low crosstalk and excellent total harmonic distortion (THD). The break-before-make feature prevents signal distortion during signal transfer from one channel to another. The high-speed paths support bandwidth as high as 500 MHz to provide adequate support for DisplayPort AUX, PCIe clock, and other similar signals. Together with low power consumption, these features make this device suitable for portable audio applications.

The TS3USBCA4 supports operation from a wide V_{CC} range between 2.4 V and 5.5 V, which gives the system designer the flexibility of powering the device from various sources, such as a regulator, a single-cell battery, or VBUS. The TS3USBCA4 provides options for both commercial and industrial temperature ranges.

8.2 Functional Block Diagram

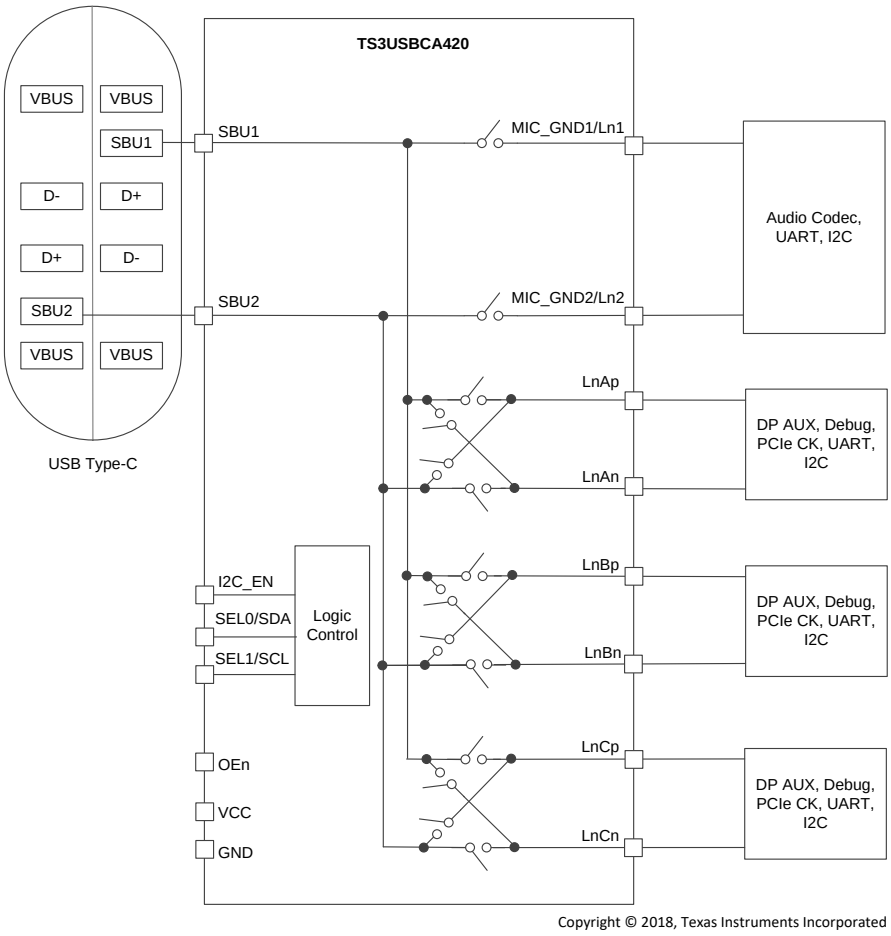


Figure 17. Functional Block Diagram

8.3 Feature Description

8.3.1 Analog Audio Path

The TS3USBCA4 supports analog audio switching between the SBU1 and SBU2 pins on one side of the switch. It supports the MIC_GND1 and MIC_GND2 pins on the other side of the switch. This audio path has an ultra-low ON resistance and low total harmonic distortion for better audio performance.

The MIC and AGND paths are identical by design, with both providing ultra-low R_{ON}. The audio path does not support flipping MIC and AGND. The audio codec should provide this function.

8.3.2 High-Speed Paths

The TS3USBCA4 supports three (TS3USBCA420) or two (TS3USBCA410) high-speed paths between the SBU1 and SBU2 pins on one side of the switch. The LnAp/LnAn, LnBp/LnBn or LnCp/LnCn pins on the other side of the switch. The high-speed paths are identical by design. All high-speed paths have a 500-MHz bandwidth, a low ON-state resistance, and low additive random jitter for signal integrity. For different USB Type-C plug orientations, the polarity of each high-speed lane can be flipped through the I^2C interface in TS3USBCA420, or though either the I^2C interface or pin control in TS3USBCA410.

8.3.3 3-level Input

The 3-level input pin I2C_EN is used to enable the I^2C interface and to choose between two I^2C slave addresses to avoid address conflict. The settings for the three levels are shown in Table 1.

Table 1. 3-Level Control Pin Settings

Level	I2C_EN Pin Settings	Configuration Mode
L	Tied directly to GND or left floating	Pin-configuration mode
M	Tied directly to $V_{CC}/2$	I^2C-configuration mode with ADDR0
H	Tied directly to V_{CC}	I^2C-configuration mode with ADDR1

8.4 Device Functional Modes

Switch selection and flipping can be controlled either through the I²C interface in I²C-configuration mode or through the control pins (SEL0, SEL1, and FLIP when applicable) in pin-configuration mode, according to Table 1. Table 2 and Table 3 show the configuration truth table for TS3USBCA420 and TS3USBCA410, respectively. Note in TS3USBCA420 the flipping capability is available only in I²C-configuration mode.

Table 2. TS3USBCA420 Switch Configuration Truth Table(1)

{SWSEL[1:0], FLIPSEL} (I²C-Configuration Mode)	{SEL1, SEL0} (Pin-Configuration Mode)	Input Pin	Output Pin
000	LL	SBU1	LnBp
		SBU2	LnBn
001		SBU1	LnBn
		SBU2	LnBp
010	LH	SBU1	MIC_GND1/Ln1
		SBU2	MIC_GND2/Ln2
011		SBU1	MIC_GND1/Ln1
		SBU2	MIC_GND2/Ln2
100	HL	SBU1	LnCp
		SBU2	LnCn
101		SBU1	LnCp
		SBU2	LnCn
110	HH	SBU1	LnAp
		SBU2	LnAn
111		SBU1	LnAn
		SBU2	LnAp

(1) For normal operation, drive OEn low (and in I²C mode set DEVICE_ENABLE = 1'b1). Driving the OEn pin high (or in I²C mode setting DEVICE_ENABLE = 1'b0) disables the switch. Note: The ports which are not selected by the control lines are in high impedance state

Table 3. TS3USBCA410 Switch Configuration Truth Table(1)

{SWSEL[1:0], FLIPSEL} (I²C-Configuration Mode)	{SEL1, SEL0, FLIP} (Pin-Configuration Mode)	Input Pin	Output Pin
000	LLL	SBU1	LnBp
		SBU2	LnBn
001	LLH	SBU1	LnBn
		SBU2	LnBp
010	LHL	SBU1	MIC_GND1/Ln1
		SBU2	MIC_GND2/Ln2
011	LHH	SBU1	MIC_GND1/Ln1
		SBU2	MIC_GND2/Ln2
100	HLL	SBU1	
		SBU2	
101	HLH	SBU1	
		SBU2	
110	HHL	SBU1	LnAp
		SBU2	LnAn
111	HHH	SBU1	LnAn
		SBU2	LnAp

(1) For normal operation, drive OEn low (and in I²C mode set DEVICE_ENABLE = 1'b1). Driving the OEn pin high (or in I²C mode setting DEVICE_ENABLE = 1'b0) disables the switch. Note: The ports which are not selected by the control lines are in high impedance state

In addition to switch control, the I^2C-configuration mode also allows enabling and disabling the device through the *DEVICE_ENABLE* register. Table 4 shows the details.

Table 4. TS3USBCA4 Enable/Disable Truth Table

OEn	DEVICE_ENABLE	Device Behavior
L	0	Device is shut down with I_{OFF_I2C}. On-chip bandgap and IO buffers are still on. I^2C is functional.
L	1	Normal operation.
H	X	Device is under reset with I_{OFF_OEN}. On-chip bandgap and IO buffers are off. I^2C is not functional.

8.5 Programming

The TS3USBCA4 can be controlled using I^2C. The SCL and SDA terminals are used for I^2C clock and I^2C data respectively.

Table 5. TS3USBCA4 I^2C Slave Address

ADDR	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
ADDR0	1	0	1	1	1	0	0	0/1
ADDR1	1	0	1	1	1	0	1	0/1

The following procedure should be followed to write to TS3USBCA4 I^2C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TS3USBCA4 7-bit address and a zero-value “W/R” bit to indicate a write cycle
2. The TS3USBCA4 acknowledges the address cycle.
3. The master presents the sub-address (I^2C register within TS3USBCA4) to be written, consisting of one byte of data, MSB-first.
4. The TS3USBCA4 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I^2C register.
6. The TS3USBCA4 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TS3USBCA4.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure should be followed to read the TS3USBCA4 I^2C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TS3USBCA4 7-bit address and a one-value “W/R” bit to indicate a read cycle
2. The TS3USBCA4 acknowledges the address cycle.
3. The TS3USBCA4 transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the I^2C.register occurred prior to the read, then the TS3USBCA4 shall start at the sub-address specified in the write.
4. The TS3USBCA4 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I^2C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TS3USBCA4 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure should be followed for setting a starting sub-address for I^2C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the TS3USBCA4 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TS3USBCA4 acknowledges the address cycle.
3. The master presents the sub-address (I^2C register within TS3USBCA4) to be written, consisting of one byte of data, MSB-first.
4. The TS3USBCA4 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

NOTE

Upon reset, the TS3USBCA4 sub-address is always set to 0x00. The TS3USBCA4 increments the sub-address by one after each successful read or write transaction, so that the next read transaction that does not explicitly specify the sub-address will start from the next register.

8.6 Register Maps

8.6.1 TS3USBCA4 Registers

Table 6 lists the memory-mapped registers for the TS3USBCA4 registers. All register offset addresses not listed in Table 6 should be considered as reserved locations and the register contents should not be modified.

Table 6. TS3USBCA4 Registers

Offset	Acronym	Register Name	Section
9h	Revision_ID	Revsion ID	Go
Ah	General_1	Enable and FLIPSEL control	Go
Bh	General_2	SWSEL control	Go

Complex bit access types are encoded to fit into small table cells. Table 7 shows the codes that are used for access types in this section.

Table 7. TS3USBCA4 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 Revision_ID Register (Offset = 9h) [reset = 0h]

Revision_ID is shown in Figure 18 and described in Table 8.

Return to Summary Table.

Figure 18. Revision_ID Register

7	6	5	4	3	2	1	0
RESERVED				REVISION_ID			
R-0h				R-0h			

Table 8. Revision_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	REVISION_ID	R	0h	Silicon revision.

8.6.1.2 General_1 Register (Offset = Ah) [reset = 0h]

General_1 is shown in Figure 19 and described in Table 9.

Return to Summary Table.

Figure 19. General_1 Register

7	6	5	4	3	2	1	0
RESERVED						DEVICE_ENABLE	FLIPSEL
R-0h						R/W-0h	R/W-0h

Table 9. General_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	DEVICE_ENABLE	R/W	0h	Controls the switch enable. 0h = Disabled 1h = Enabled
0	FLIPSEL	R/W	0h	Controls the USB-C orientation. 0h = Normal Orientation 1h = Flip orientation.

8.6.1.3 General_2 Register (Offset = Bh) [reset = 0h]

General_2 is shown in Figure 20 and described in Table 10.

Return to Summary Table.

Figure 20. General_2 Register

7	6	5	4	3	2	1	0
RESERVED						SWSEL	
R-0h						R/W-0h	

Table 10. General_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	SWSEL	R/W	0h	This field along with FLIPSEL controls the SBU switch connections. 0h = SBU to LnB 1h = SBU to MICGND 2h = SBU to LnC 3h = SBU to LnA

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SBU1 and SBU2 pins of a USB type-C connector can be re-purposed in different applications. Examples include DisplayPort AUX, analog audio MIC and AGND, and debug signals. The TS3USBCA4 is controlled by a micro-processor (that is, an application processor in a smartphone) that routes SBU1 and SBU2 to the desired destination, such as a DisplayPort source or sink, an audio codec, or a processor. The TS3USBCA4 provides cross-switch capability for different USB type-C plug orientations.

9.2 Typical Application

Figure 21 shows the typical application of TS3USBCA420 in I^2C-configuration mode from a 3.3-V supply. The I^2C slave address is set to ADDR1. V_{IO_uP} is the supply for the micro-processor IOs.

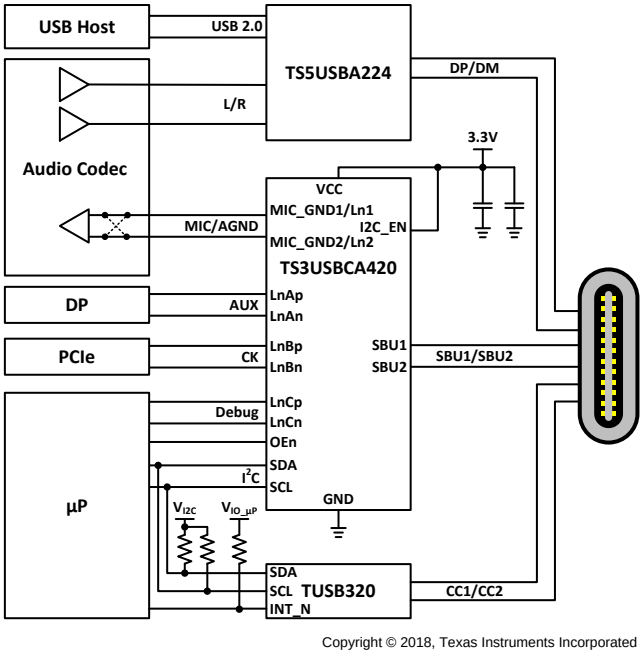


Figure 21. Application of TS3USBCA420 in I^2C-Configuration Mode

Figure 22 shows the typical application of TS3USBCA420 in pin-configuration mode from VBUS. V_{IO_uP} is the supply for the micro-processor IOs.

Typical Application (continued)

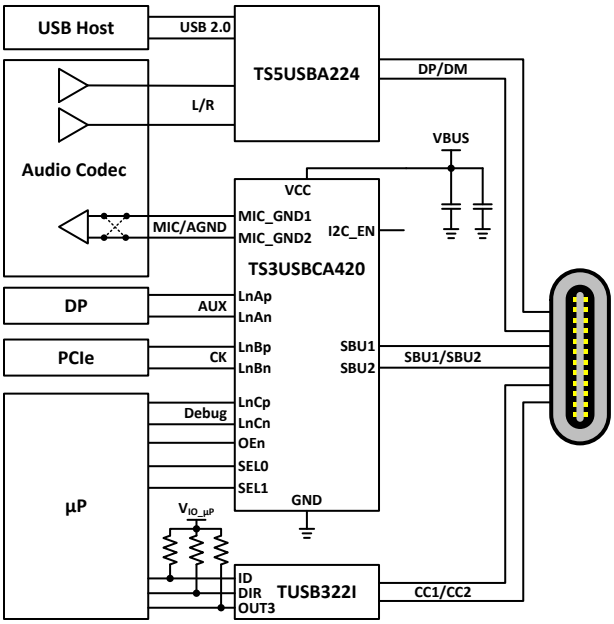


Figure 22. Application of TS3USBCA420 in Pin-Configuration Mode

Figure 21 shows the typical application of TS3USBCA410 in I^2C-configuration mode from V_{BAT}. The I^2C slave address is set to ADDR0. V_{IO_uP} is the supply for the micro-processor IOs.

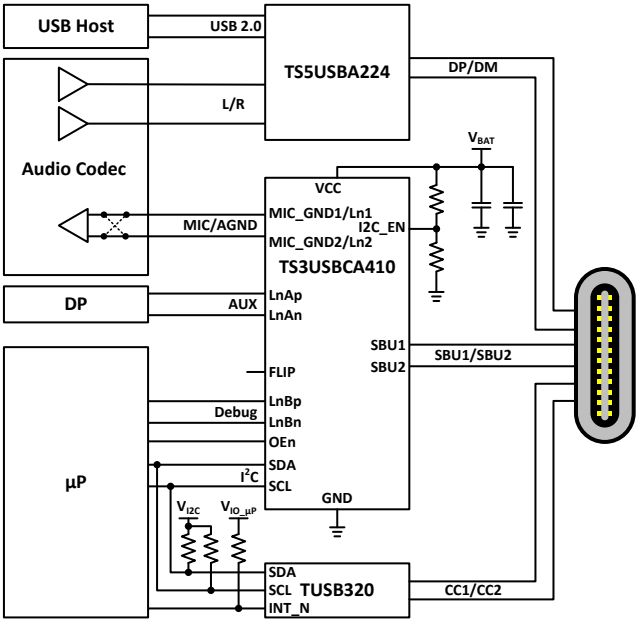


Figure 23. Application of TS3USBCA410 in I^2C-Configuration Mode

Figure 22 shows the typical application of TS3USBCA410 in pin-configuration mode from VBUS. V_{IO_uP} is the supply for the micro-processor IOs.

Typical Application (continued)

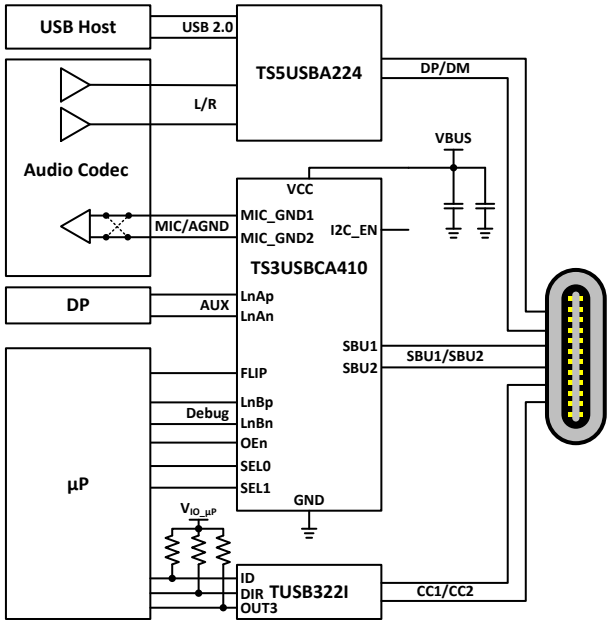


Figure 24. Application of TS3USBCA410 in Pin-Configuration Mode

9.2.1 Design Requirements

Design requirements of USB type-C and other relevant standards (DisplayPort, analog audio, etc.) must be followed.

9.2.2 Detailed Design Procedure

The design procedure starts with the choice of supply. TS3USBCA4 wide supply range from 2.4 V to 5.5 V gives the designer flexibility when selecting a supply. Examples include, but are not limited to, a single-cell battery, a 3.3-V regulator, or VBUS. The designer must account for the parametric variation of TS3USBCA4 with supply range, the supply range of other components in the system, the IO voltage levels of companion devices, and cost. For example, a regulated 3.3-V V_{CC} has the advantage of smaller variation of TS3USBCA4 performance compared to a single-cell batter between 2.7 V and 4.3 V. This regulator may add to the system cost and board area.

The next step in the design procedure is to choose between I^2C- and pin-configuration mode. The I^2C-configuration mode is preferred because it reduces the number of IOs needed from the micro-processor. Note that in TS3USBCA420 the flip functionality is only available in the I^2C-configuration mode. The designer can choose from two I^2C slave addresses through pin-strapping of I2C_EN to avoid address conflict. The IOs of TS3USBCA4 have well-controlled V_{IH} and V_{IL} and are supposed to work with a wide range of IO voltage levels of the micro-processor. However, the designer needs to check the compatibility of the IOs between the micro-processor and TS3USBCA4, and insert level translators when necessary.

In I^2C-configuration mode, when it is necessary to set I2C_EN to the middle level to avoid slave address conflict, it is desirable to use as high a resistor value as possible for the resistor divider to minimize the static current through the resistor divider. However, the designer needs to take into account the resistor tolerance and the effect of the on-chip pull-down resistor to ensure a satisfactory voltage margin for V_{IM} of the I2C_EN pin.

It should be noted that the bandwidth of the high-speed lanes is defined with the audio channel open. Due to the low R_{ON} of the audio channel, big parasitic capacitance exists between the audio output port and the SBU port. The load (capacitive and/or resistive) at the audio output port may significantly impact the bandwidth of the high-speed lanes. If bandwidth is importance, the audio channel is preferred. If certain high-speed signals have to go through the high-speed lanes, care should be taken to minimize the load at the audio output port, including the traces.

Typical Application (continued)

9.2.3 Application Curves

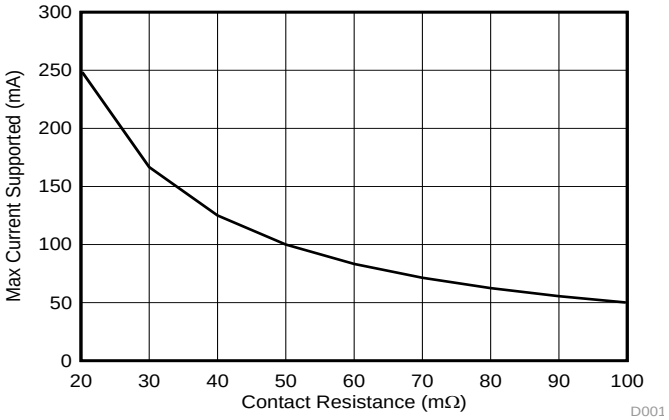


Figure 25. Max Current vs Contact Resistance

10 Power Supply Recommendations

The TS3USBCA4 is designed to operate from a V_{CC} range between 2.4 V and 5.5 V. The supply is recommended to be decoupled to ground via two de-coupling capacitors of 0.1 µF and 1 µF placed as close as possible to the TS3USBCA4. To ensure a POR trip during a power-down and power-on event the power supply should follow the minimum and maximum V_{CC} rise and fall times specified in the electrical specifications section.

11 Layout

11.1 Layout Guidelines

- The V_{CC} pin must have de-coupling capacitors placed as closely to the device as possible. Typically recommended capacitors are a 0.1-µF and a 1-µF capacitor.
- The total resistance from SBU1 and SBU2 pins of the type-C connector to the MIC_GND1 and MIC_GND2 pins of the audio codec should be kept low to avoid degrading the crosstalk performance.
- Route the I^2C and digital signals away from the audio signals to prevent coupling onto the audio lines.

11.2 Layout Example

Figure 26 shows a layout example of TS3USBCA420.

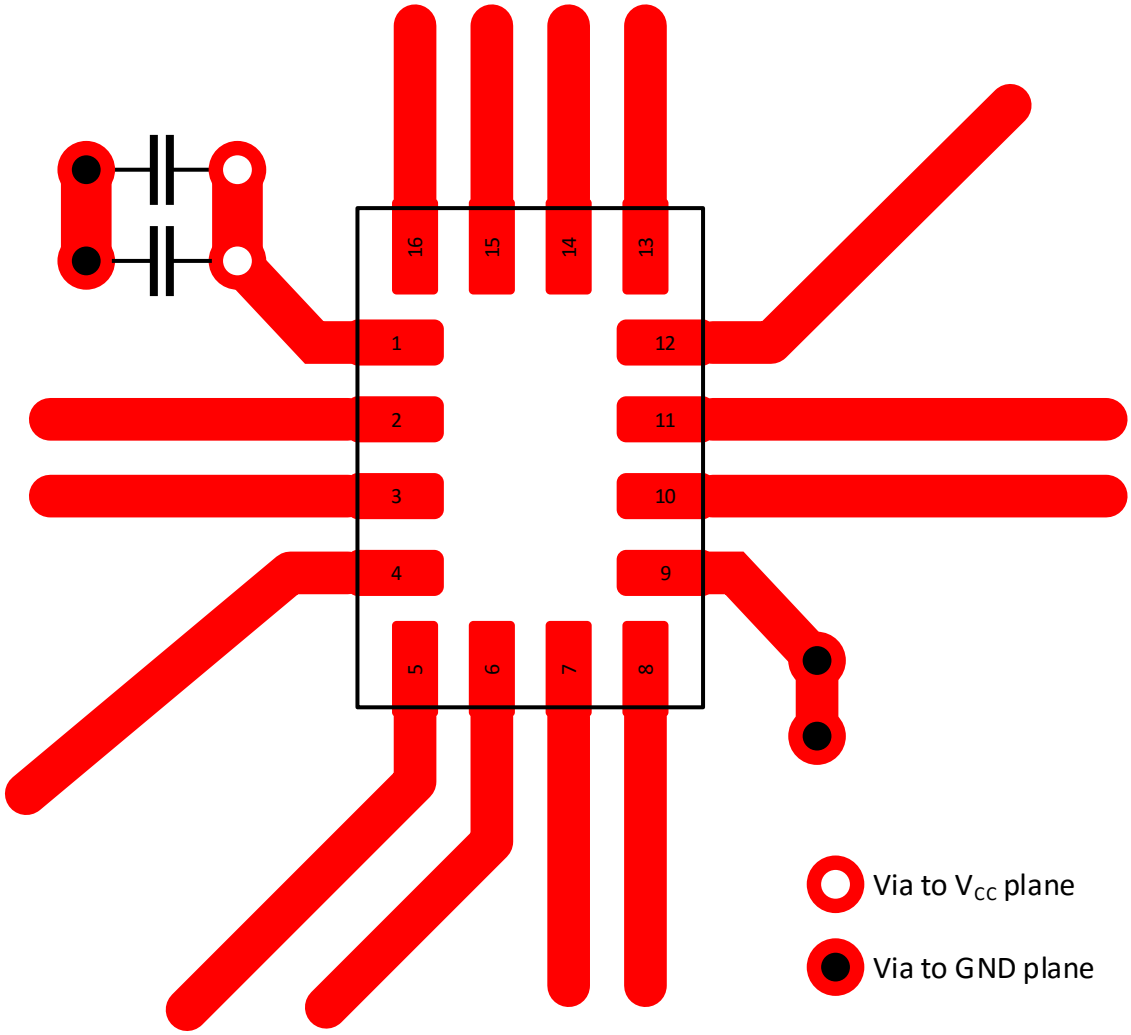


Figure 26. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

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USB Type-C is a trademark of USB Implementers Forum.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USBCA410IRSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	410	Samples
TS3USBCA410IRSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	410	Samples
TS3USBCA410RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	410	Samples
TS3USBCA410RSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	410	Samples
TS3USBCA420IRSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	420	Samples
TS3USBCA420IRSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	420	Samples
TS3USBCA420RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	420	Samples
TS3USBCA420RSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	420	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

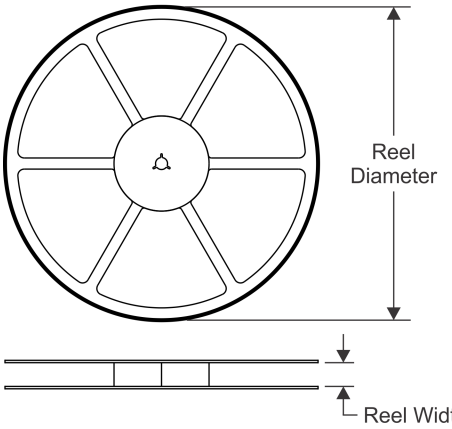
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

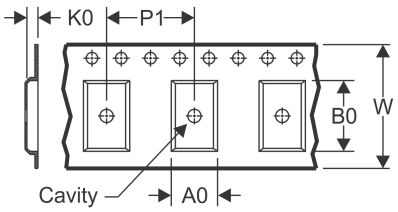
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

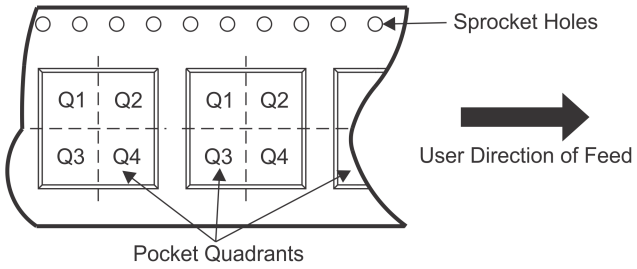


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

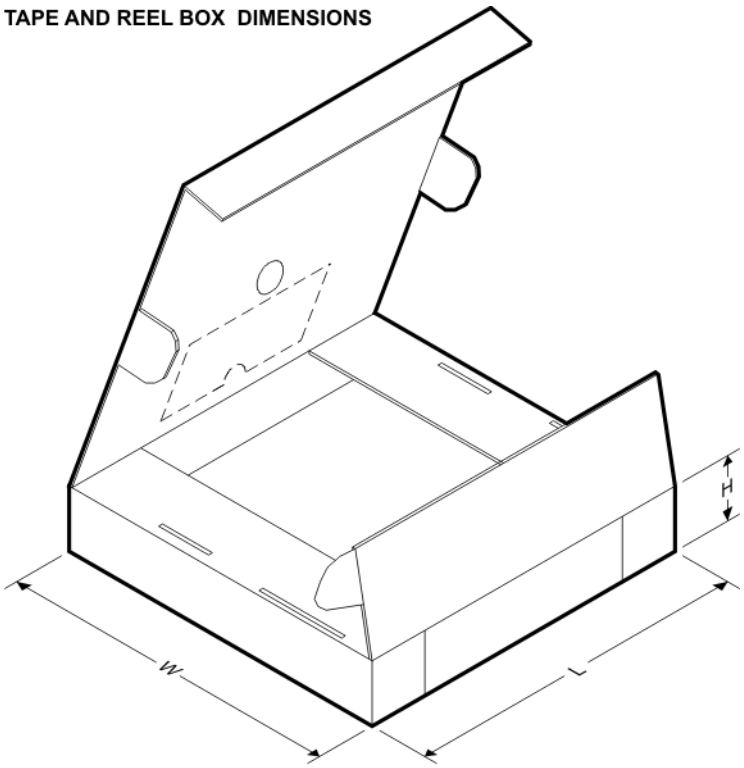
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USBCA410IRSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA410IRSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA410RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA410RSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA420IRSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA420IRSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA420RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA420RSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

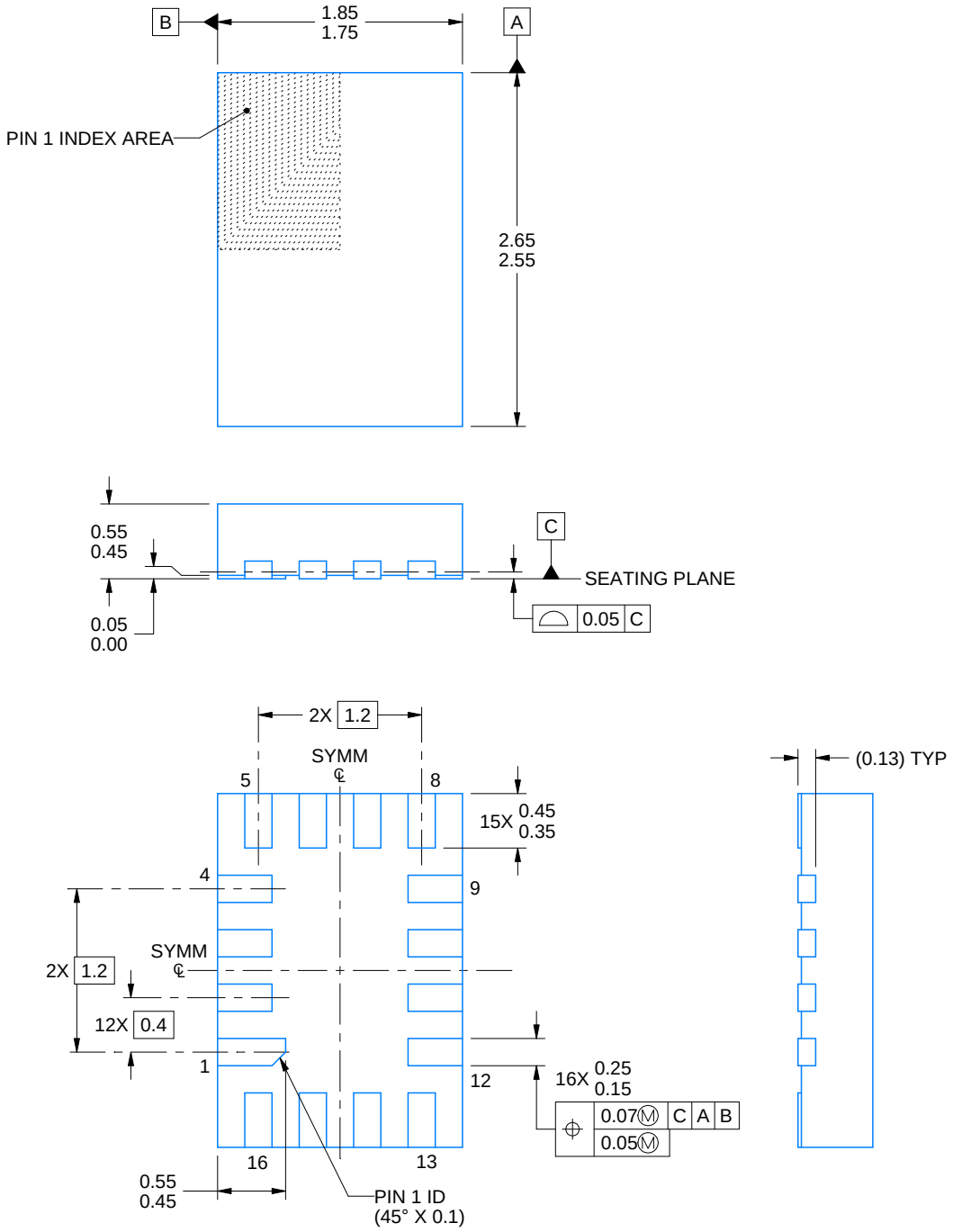
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USBCA410IRSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TS3USBCA410IRSVT	UQFN	RSV	16	250	189.0	185.0	36.0
TS3USBCA410RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TS3USBCA410RSVT	UQFN	RSV	16	250	189.0	185.0	36.0
TS3USBCA420IRSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TS3USBCA420IRSVT	UQFN	RSV	16	250	189.0	185.0	36.0
TS3USBCA420RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TS3USBCA420RSVT	UQFN	RSV	16	250	189.0	185.0	36.0

RSV0016A

PACKAGE OUTLINE

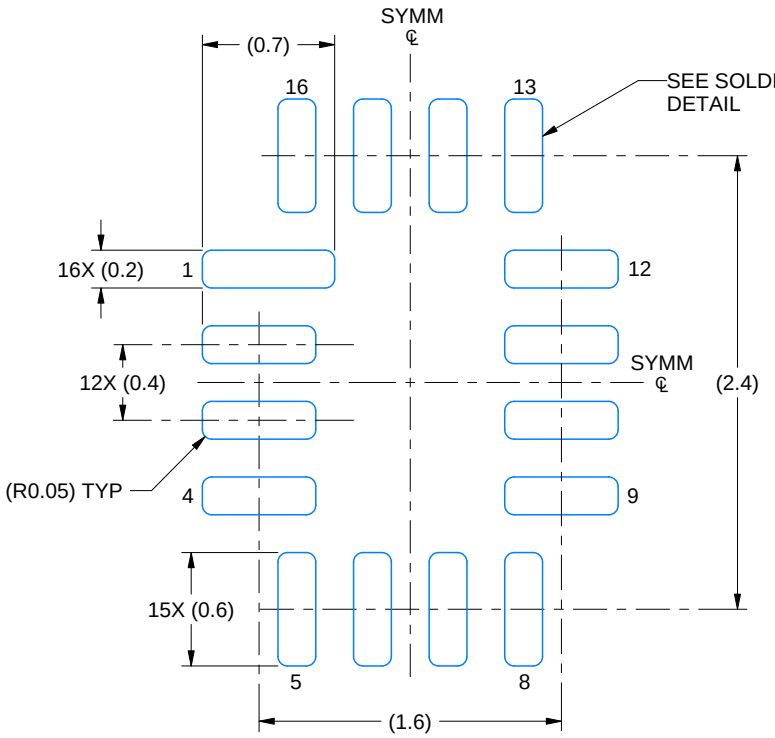
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

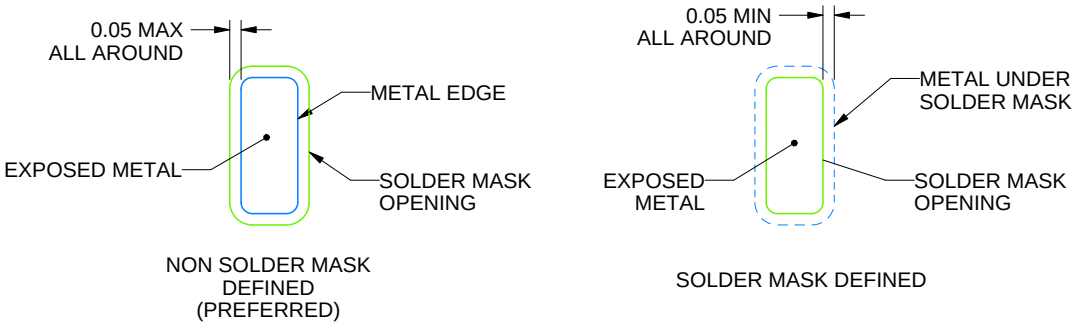


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

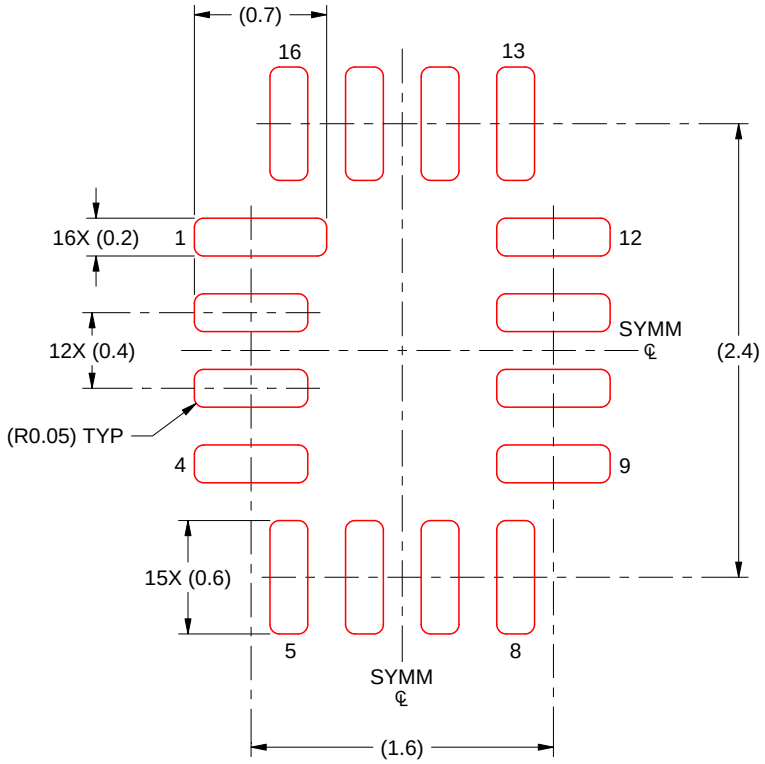


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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