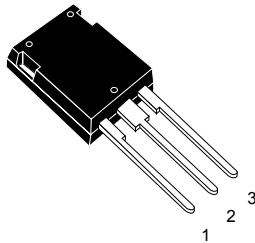
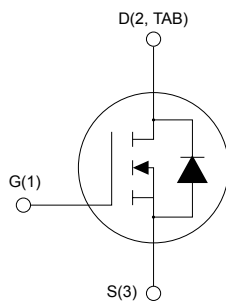


N-channel 650 V, 19 mΩ typ., 96 A MDmesh M5 Power MOSFET in a Max247 package



Max247



AM01475v1_no2en



Features

Order code	V_{DS} at T_J max.	$R_{DS(on)}$ max.	I_D
STY112N65M5	710 V	22 mΩ	96 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link

[STY112N65M5](#)

Product summary

Order code	STY112N65M5
Marking	112N65M5
Package	Max247
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	96	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	61	
$I_{DM}^{(1)}$	Drain current (pulsed)	384	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	625	W
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	12	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	2400	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 96\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.2	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	30	°C/W

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			10	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 48\text{ A}$		19	22	m Ω

1. Specified by design, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	16870	-	pF
C_{oss}	Output capacitance		-	365	-	pF
C_{rss}	Reverse transfer capacitance		-	7	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	1333	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	350	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.26	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 48\text{ A}$	-	350	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	97	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	118	-	nC

- $C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.
- $C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 64\text{ A}$,	-	267	-	ns
$t_{r(v)}$	Voltage rise time	$R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	79	-	ns
$t_{f(i)}$	Current fall time	(see Figure 15. Test circuit for inductive load switching and diode recovery times and Figure 18. Switching time waveform)	-	53	-	ns
$t_{c(off)}$	Crossing time		-	140	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		96	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		384	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 96 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 96 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	570		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100 \text{ V}$	-	17		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	60		A
t_{rr}	Reverse recovery time	$I_{SD} = 96 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	695		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	26		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	73		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

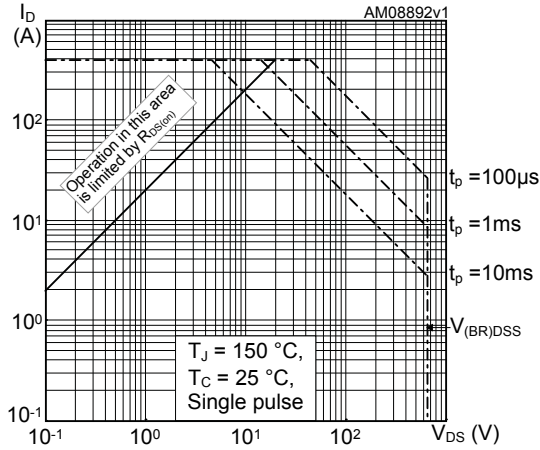


Figure 2. Normalized transient thermal impedance

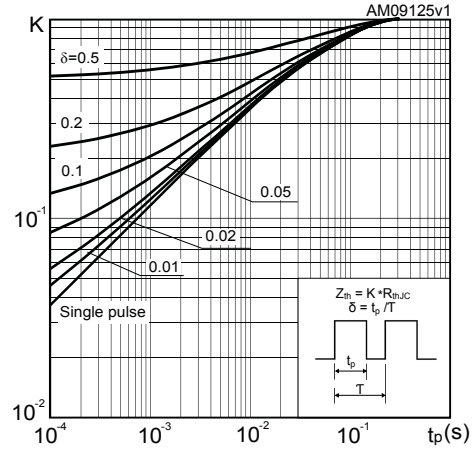


Figure 3. Typical output characteristics

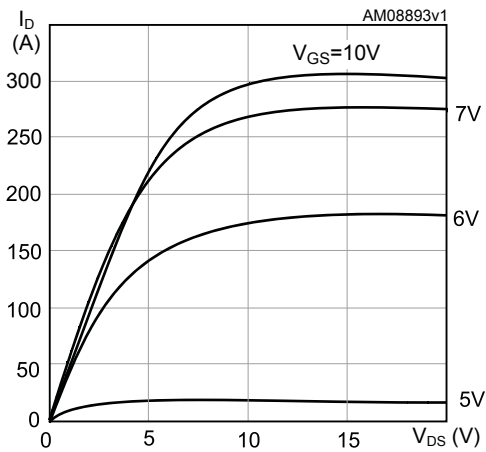


Figure 4. Typical transfer characteristics

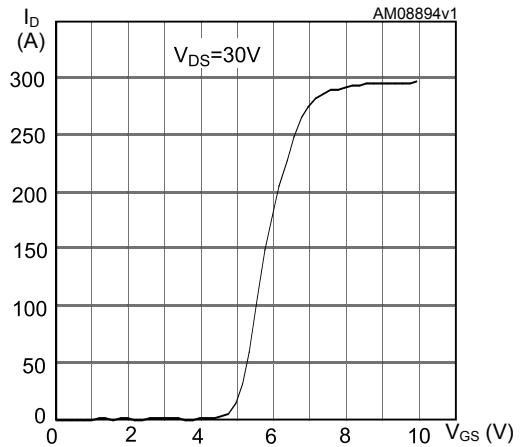


Figure 5. Normalized breakdown voltage vs temperature

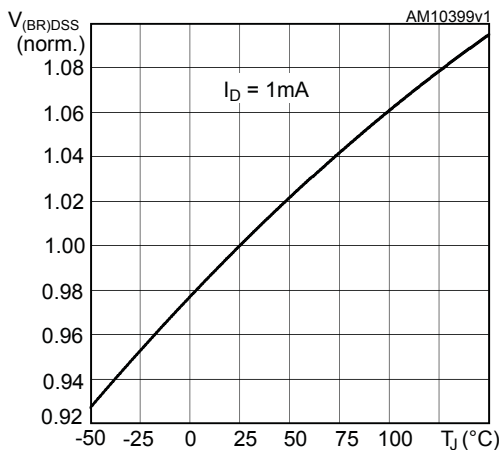


Figure 6. Typical drain-source on-resistance

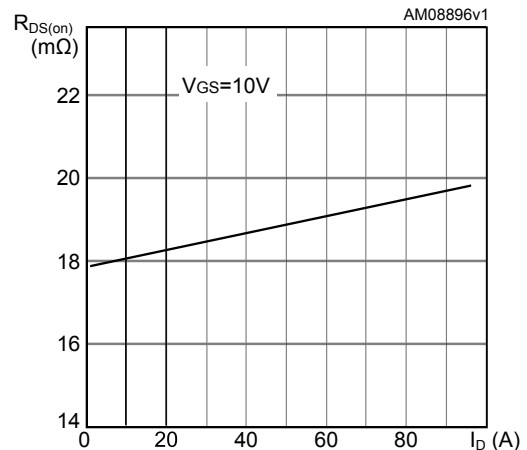


Figure 7. Typical gate charge characteristics

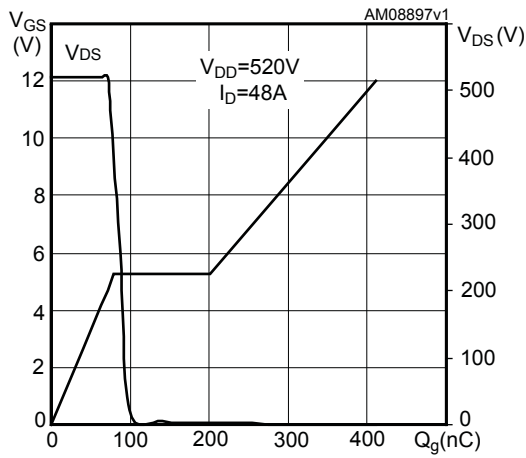


Figure 8. Typical capacitance characteristics

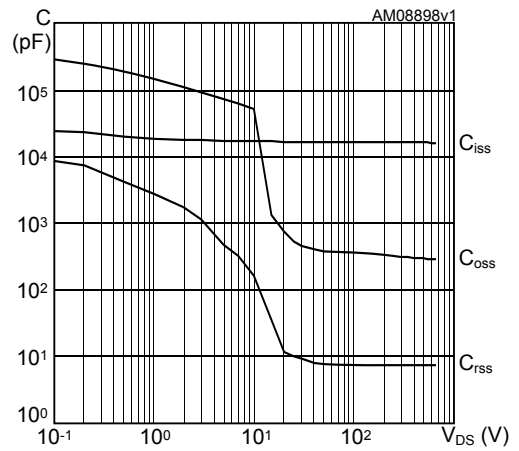


Figure 9. Normalized gate threshold vs temperature

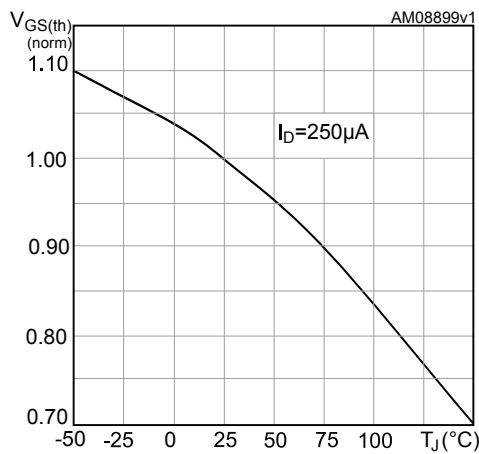


Figure 10. Normalized on-resistance vs temperature

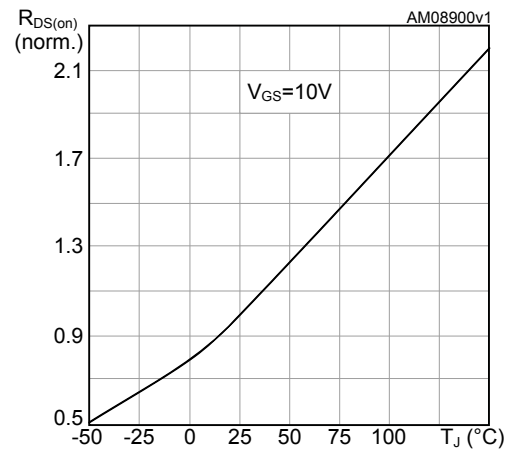


Figure 11. Typical output capacitance stored energy

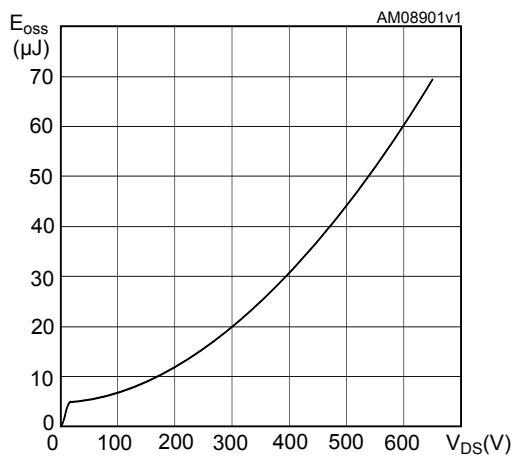
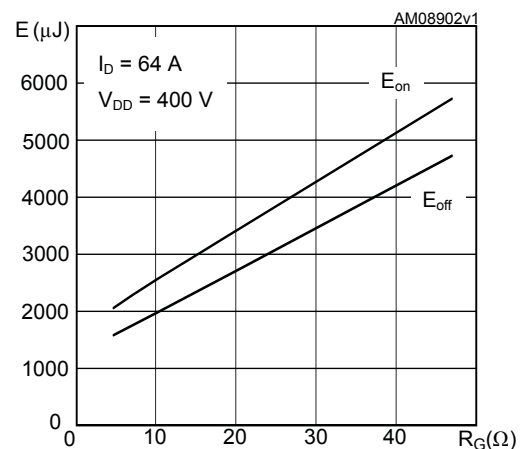


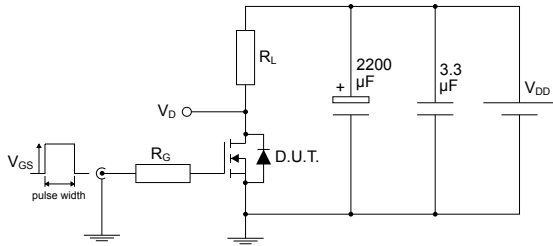
Figure 12. Typical switching energy vs gate resistance



Note: E_{on} including reverse recovery of a SiC diode.

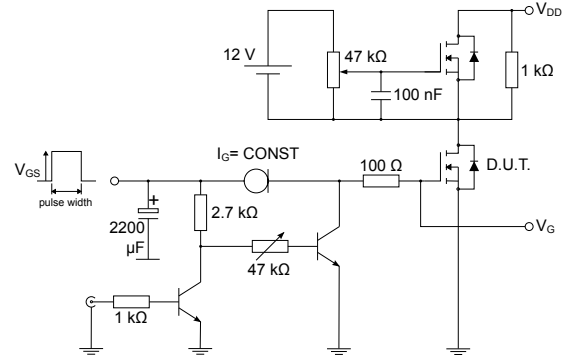
3 Test circuits

Figure 13. Test circuit for resistive load switching times



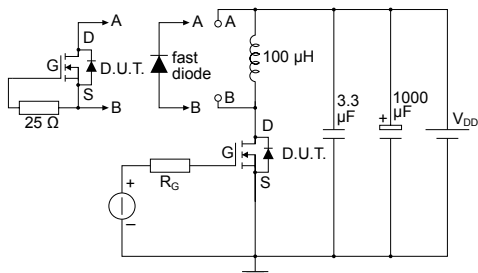
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Figure 14. Test circuit for gate charge behavior



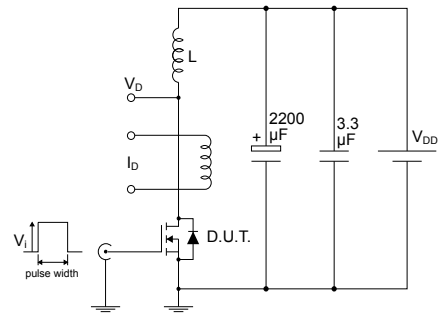
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Figure 15. Test circuit for inductive load switching and diode recovery times



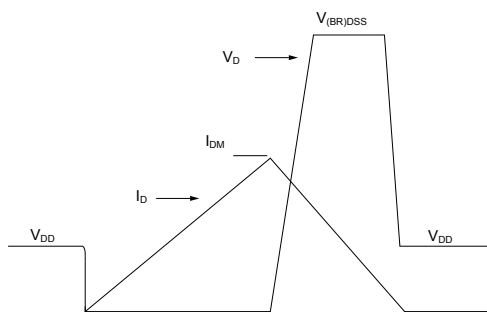
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Figure 16. Unclamped inductive load test circuit



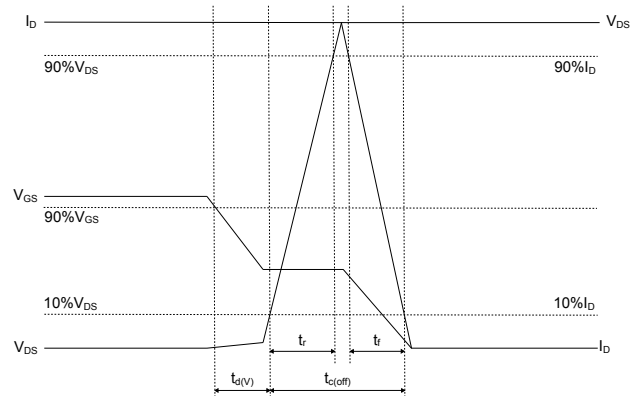
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



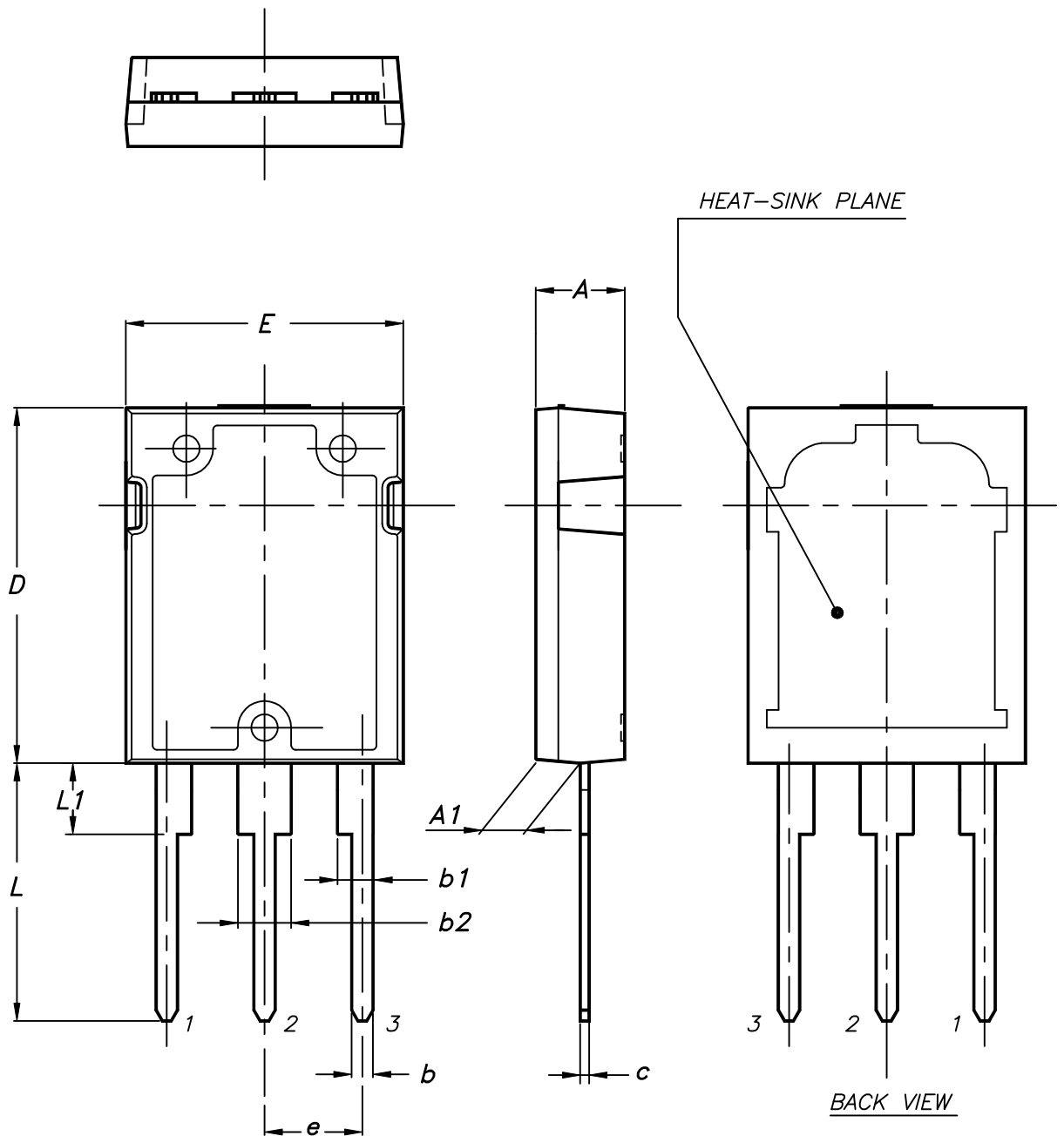
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 Max247 package information

Figure 19. Max247 package outline



0094330_5

Table 7. Max247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.70	-	5.30
A1	2.20	-	2.60
b	1.00	-	1.40
b1	2.00	-	2.40
b2	3.00	-	3.40
c	0.40	-	0.80
D	19.70	-	20.30
e	5.35	-	5.55
E	15.30	-	15.90
L	14.20	-	15.20
L1	3.70	-	4.30

Revision history

Table 8. Document revision history

Date	Revision	Changes
20-Jan-2009	1	First release.
20-May-2011	2	Document status promoted from preliminary data to datasheet.
03-May-2012	3	<i>Section 4: Package mechanical data</i> has been updated.
18-Jul-2022	4	Updated title, Internal schematic , Features and Description on cover page. Updated I_{AR} value in Table 1. Absolute maximum ratings and updated Table 2. Thermal data . Minor text changes.

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