2.4GHz wireless audio streamer nRF24Z1

FEATURES

- Low cost 0.18u CMOS process, 36 pin 6x6mm QFN package
- Single chip 2.4GHz RF transceiver
- 4Mbit/sec RF link
- Input/output sample rate up to 48kSPS, 24 bit
- Programmable latency
- Quality of Service engine supporting up to 1.536 Mbit/s LPCM audio
- S/PDIF interface for direct connection to PC soundcard and surround receivers
- I2S interface for glue-less audio support
- SPI or 2-wire interface for up to 12 kbit/s peak bi-directional digital control/AUX data
- On chip optional compression
- On chip voltage regulators
- Few external components
- Uses global 2.4GHz band

APPLICATIONS

- Compact Disk, CD quality headset
- MP3 / Mini Disk headset
- Speakers
- Surround speakers
- Microphone
- Musical instruments
- Audio streaming from PC soundcard to HiFi system
- Compressed video streaming

GENERAL DESCRIPTION

nRF24Z1 provides a true single chip system for CD quality audio streaming of up to16 bit 48 kSPS audio, supporting up to 24 bit 48 kSPS input. I2S and S/PDIF interfaces are supported for audio I/O. Seamless interfacing of low cost A/D and D/A for analog audio input and output. SPI or 2-wire (I2C compatible) control serial interfaces. Embedded voltage regulators yield maximum noise immunity and allows operation from a single 2.0V to 3.6V supply.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	2.0	V
Temperature range	-20 to +80	°C
Peak supply current in transmit @ -5dBm output power	15	mA
Peak supply current in receive mode	32	mA
Supply current in power down mode	5	µA
Maximum transmit output power	0	dBm
Audio sample rate	8 to 48	kSPS
Audio resolution	16	bit
Receiver sensitivity	-80	dBm

Table 1-1 nRF24Z1 quick reference data.

ORDERING INFORMATION

Type number	Description	Version
nRF24Z1	36L QFN 6x6 mm	C
nRF24Z1-EVKIT	Evaluation kit	1.0

Table 1-2 nRF24Z1 ordering information.

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1 Pin Assignment

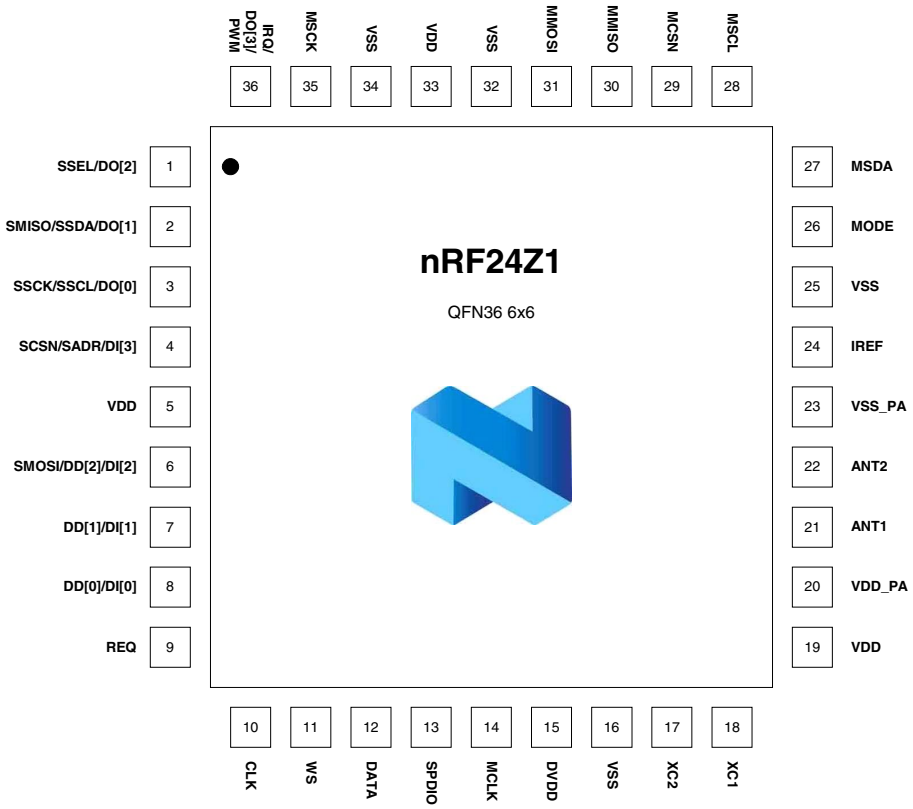


Figure 1-1 Pin assignment nRF24Z1

2 Pin Functions

Table 2-1 shows the nRF24Z1 pin functions. Note that pin functions depend on the functional mode of the device (ATX; audio source or ARX; audio recipient) and the interface of choice.

Pin No.	Pin name		Pin function		Description	
	Serial slave interface	ARX GPIO	Serial slave interface	ARX GPIO interface	ATX/ARX w. Serial slave interface	ARX w. GPIO interface
1	SSEL	DO[2]	Digital Input	Digital Output	Slave interface select 1: 2-wire, 0: SPI	GPIO out bit #2
2	SMISO /SSDA	DO[1]	Digital Output / Digital IO		Slave SPI serial out / Slave 2-wire data (bidir)	GPIO out bit #1
3	SSCK /SSCL	DO[0]	Digital Input	Digital Output	Slave SPI clock / Slave 2-wire clock	GPIO out bit #0
4	SCSN /SADR	DI[3]	Digital Input		Slave SPI slave select / Address select 2-wire slave	GPIO in bit #2
5	VDD		Power		Power Supply (2.0-3.6 V DC)	
6	SMOSI /DD[2]	DI[2]	Digital Input		Slave SPI serial in / Direct data in bit #2	GPIO in bit #3
7	DD[1]	DI[1]	Digital Input		Direct data in bit #1	GPIO in bit #1
8	DD[0]	DI[0]	Digital Input		Direct data in bit #0	GPIO in bit #0
			ATX	**ARX**		
9	REQ		Dig. Out	Dig. In	For ATX not connected, for ARX connect to VSS	
10	CLK		Dig. IO	Dig. Out	I2S bit clock	
11	WS		Dig. IO	Dig. Out	I2S word clock	
12	DATA		Dig. In	Dig. Out	I2S data signal	
13	SPDIO		Dig. In	Dig. Out	S/PDIF interface	
14	MCLK		Digital Output		256X sample rate clock to ADC or DAC	
15	DVDD		Regulator output		Digital voltage regulator output for decoupling	
16	VSS		Power		Ground (0V)	
17	XC2		Analog output		Crystal Pin 2	
18	XC1		Analog input		Crystal Pin 1	
19	VDD		Power		Power Supply (2.0-3.6 V DC)	
20	VDD_PA		Regulator output		DC output (+1.8V) for RF interface (ANT1, ANT2)	
21	ANT1		RF		Antenna interface 1	
22	ANT2		RF		Antenna interface 2	
23	VSS_PA		Power		Ground (0V)	
24	IREF		Analog input		Connection to external Bias reference resistor, or RESET if pulled to VDD	
25	VSS		Power		Ground (0V)	
26	MODE		Digital Input		nRF24Z1 function 1 : audio transmitter, 0: audio receiver	
27	MSDA		Digital IO		Master 2-wire bi-directional data	
28	MSCL		Digital IO		Master 2-wire bi-directional clock	
29	MCSN		Digital Output		Master SPI primary slave select (active low)	
30	MMISO		Digital Input		Master SPI serial input	
31	MMOSI		Digital Output		Master SPI serial output	
32	VSS		Power		Ground (0V)	
33	VDD		Power		Power Supply (2.0-3.6 V DC)	
34	VSS		Power		Ground (0V)	
35	MSCK		Digital Output		Master SPI clock	
36	IRQ	DO[3] / PWM	Digital Output		Interrupt request	GPIO out bit #3 / PWM output

Table 2-1 nRF24Z1 pin functions

3 Glossary of terms

Term	Description
ADC	Analog to Digital Converter
AFH	Adaptive Frequency Hopping
ARX	Audio Receiver
ATX	Audio Transmitter
BER	Bit Error Rate
BoM	Bill of Materials
CD	Carrier Detect
CPHA	SPI Clock Phase
CLK	Clock
CPOL	SPI Clock Polarity
CRC	Cyclic Redundancy Check
CSN	Chip Select Not
DAC	Digital to Analog Converter
DSP	Digital Signal Processor
EEPROM	Electrical Erasable Programmable Read Only Memory
FIFO	First In First Out
Flash	Flash Memory
GFSK	Gaussian Frequency Shift Keying
GPIO	General Purpose In Out
I2S	3-wire audio serial interface
ISM	Industrial-Scientific-Medical
kSPS	kilo Samples Per Second
Latency	Audio delay from ATX input to ARX output
LPCM	Linear PCM (pulse code modulation)
LSB	Least Significant Bit
Mbps	Megabits per second
MBZ	Must Be Zero
MCU	Micro Controller Unit
MP3	MPEG3, audio compression format
MSB	Most Significant Bit
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
QoS	Quality of Service
RX	Receive
S/PDIF	One-wire serial digital audio format
SPI	Serial Peripheral Interface
TX	Transmit
2-wire	2-wire serial interface compatible with I2C

Table 3-1 Glossary of terms.

4 Architectural Overview

nRF24Z1 is a 4 Mbit/s single chip RF transceiver that operates in the world wide 2.4 GHz license free ISM band. The nR24Z1 is based on the proven nRF24xx radio- and ShockBurst™ platforms from Nordic Semiconductor.

The device offers a wireless channel for seamless streaming of LPCM or compressed audio in parallel with a low data rate control channel. To enable this, the device offers the following features in addition to the nRF24xx RF platform:

- Standard digital audio interfaces (I2S, S/PDIF)
- Fully embedded Quality of Service engine handling all RF protocol and RF link tasks.
- SPI and 2-wire master and slave control interfaces
- GPIO pins

As all processing related to audio I/O, RF protocol and RF link management is embedded, the device offers a transparent audio channel with capacity of up to 1.54 Mbit/s, with no true time processing needed. The nRF24Z1 can be utilized in systems without external microcontroller or used in conjunction with a simple microcontroller that only need to handle low speed tasks over the serial or parallel ports (ex: volume up/down).

A block schematic of a typical nRF24Z1 based system is illustrated in Figure 4-1

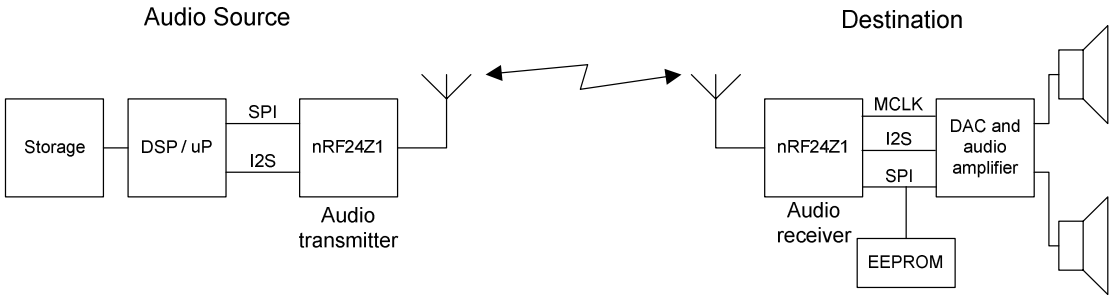


Figure 4-1 Typical audio application using nRF24Z1

In this system a DSP or micro controller feeds data from a storage device to an nRF24Z1 using standard audio format (I2S). An nRF24Z1 pair transfers audio data from the source and presents it to a stereo DAC on the receiving side. Application-wise, the nRF24Z1 link will appear as an open channel (like a cable).

Initial configuration of nRF24Z1 is done by the micro controller through an SPI or 2-wire control interface. On the destination side, peripherals like a DAC can be controlled from the audio source side through the control channel offered by nRF24Z1. In designs without an external micro controller, configuration data can be loaded into the nRF24Z1 from an optional EEPROM/FLASH memory, enabling it to operate stand alone with limited feature set.

4.1 Fundamental modes of operation

A wireless system streaming audio will have an asymmetrical load on the RF link as audio data is fed from an audio source (i.e. CD player) to a destination (i.e. loud speakers). From the destination back to the audio source only service and control communication is needed.

nRF24Z1 is used both on the audio source side (ex. in a CD player) transmitting audio data, and in the recipient (loud speaker) side receiving audio data. Due to the asymmetry, nRF24Z1 has two main modes set by external pin MODE, depending on whether it represents the transmitter or the receiver. The two modes have significant differences both in internal and I/O functionality.

To differentiate these two modes of operation, the following notation is introduced:

- Audio transmitter: *ATX;* nRF24Z1 on the audio source side, transmitting audio data
- Audio receiver: *ARX;* nRF24Z1 on the destination side, receiving audio data

In this context, the terms ‘transmitter’ and ‘receiver’ are referring to the directional flow of the audio; the nRF24Z1 radio transceiver is always operating in half-duplex (e.g. bi-directional) mode.

4.2 Communication and data transfer principle

4.2.1 Data channel definition

In order to differentiate between audio data and other control and status information, the data traffic between the ATX/ARX has been organized in two data channels in this text.

The *audio channel* is defined as the communication channel sourcing audio data from the ATX to the ARX. The audio data is divided into two categories; real time data from the audio source and retransmitted audio information. When audio information is lost, the ARX requests retransmission of the lost packets. Real time audio bit rate is constant, whereas the amount of retransmitted audio varies over time.

The nRF24Z1 *control channel* is a two way, low data rate channel superimposed on the audio stream. The audio transmitter is designated master, meaning that when an RF link is active, the 2-wire, SPI, GPIO and internal registers in the audio receiver can be seen and controlled as a virtual extension of the audio transmitters own I/O and registers. The implications of this is that external devices like audio DAC or volume control components connected to the audio receiver effectively can be controlled by input to the ATX. User actions (i.e. push of a button) on the audio receiver side are similarly fed back to and can be processed on the audio transmitter side.

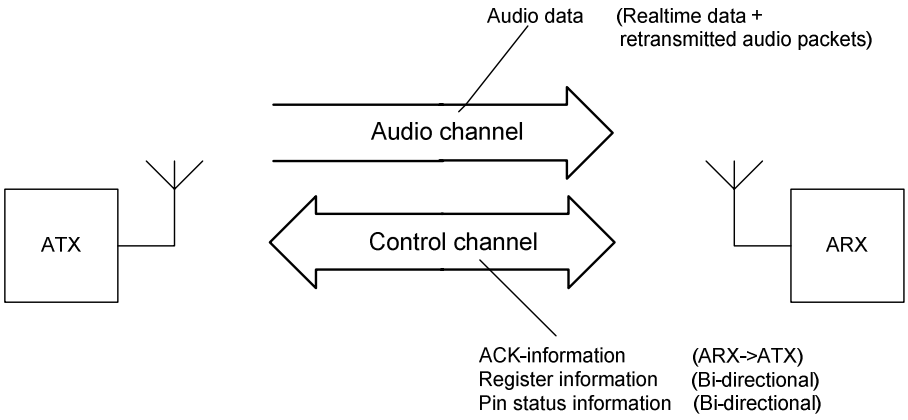


Figure 4-2 nRF24Z1 communication channel principle

4.2.2 Data flow- and organization

Figure 4-3 illustrates the communication principle of an nF24Z1 wireless link. Data is transmitted from the ATX to the ARX on a cyclic basis.

ATX data is organized in frames transmitted with frequency $1/t_p$. A data frame contains the real time audio data and retransmitted audio data requested by the ARX. Poor operating conditions (i.e. excessive range and/or high amount of interference) will result in a higher amount of retransmitted audio data a frame.

Figure 4-3 also illustrates how period length, frame size and retransmission capacity varies with sample rate and time.

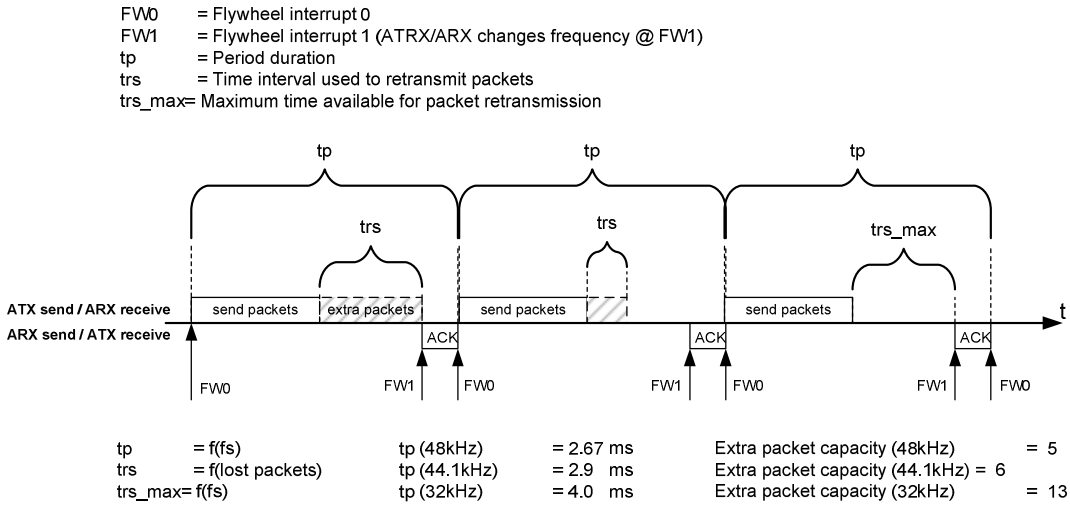


Figure 4-3 nRF24Z1 data streaming principle

Audio data is organized in *stereo samples* (SS). The stereo samples are in turn organized in *data packets* consisting of 16 stereo samples. A data packet also contain preamble, recipient address, packet id, compression information, CRC-string and a limited amount of control and register data.

A data *frame* consists of a segment of real time data. In addition, the frame contains audio packets requested by the ARX for retransmission. The maximum number of packets for retransmission depends on the sample rate of choice.

When the ARX has received the data frame, an *acknowledge packet* is generated and sent to the ATX. This packet consists of acknowledge information (requesting retransmission of corrupt/lost packets) and control and status information.

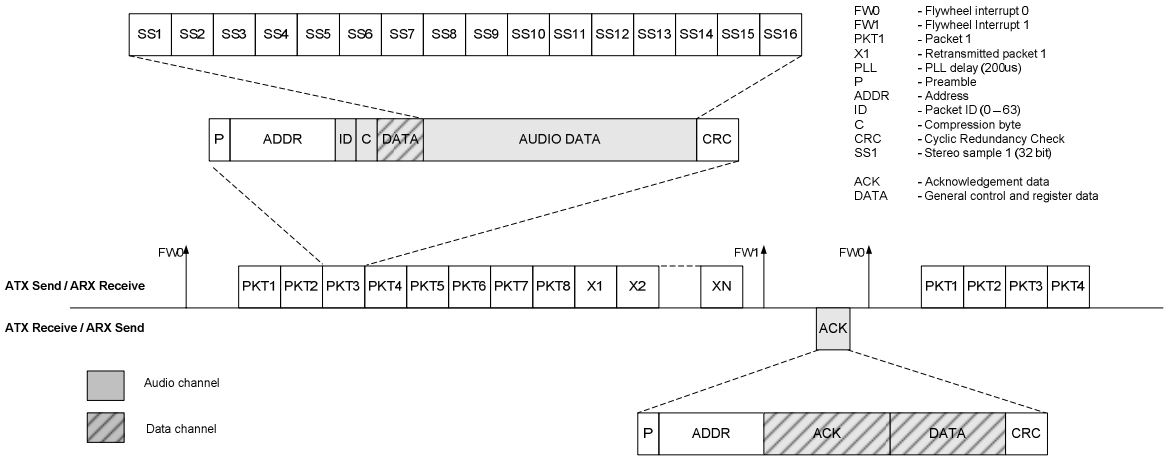


Figure 4-4 nRF24Z1 data frame and packet organization

4.3 Mode- and Interface alternatives

A number of interfaces are available for the nRF24Z1 device. The available interfaces depend on the nRF24Z1 mode of operation and the type of data to be transferred. Data is divided into two categories; audio data (audio channel) and configuration/status data (control channel). Figure 4-7 illustrates the available data interfaces for the various modes of operation.

Interface options are illustrated by grey bubbles, whilst functionality / operation modes are shown in white. Relevant configuration settings are shown in the links drawn between the bubbles.

Note that interface choice is done by a combination of pin and register settings. Refer to Chapter 7 Digital I/O for details.

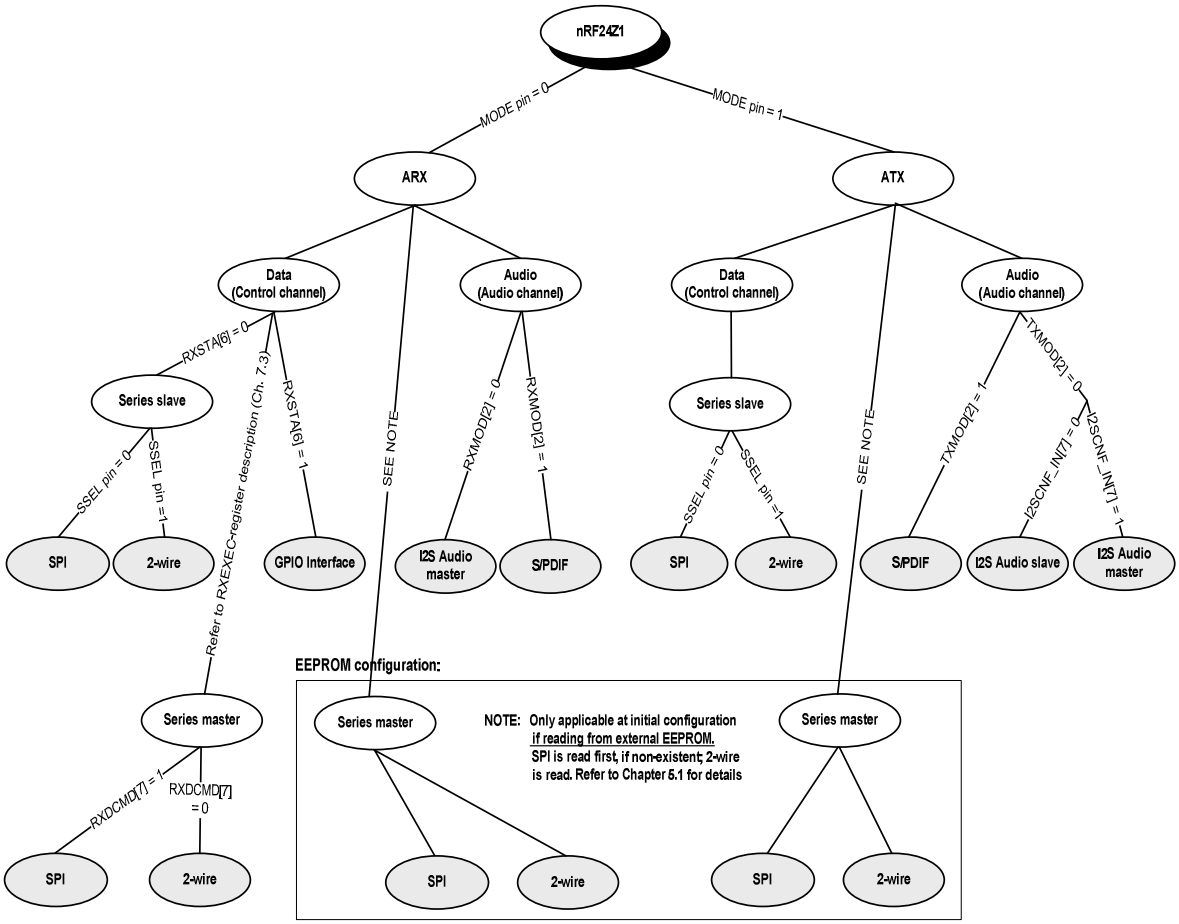


Figure 4-5 nRF24Z1 functional modes and interface alternatives

4.4 Audio transmitter (ATX)

When an nRF24Z1 is applied at the audio source side of the RF link, MODE must be high and nRF24Z1 becomes an audio transmitter (ATX). The block schematic of nRF24Z1 in ATX mode can be seen in Figure 4-6.

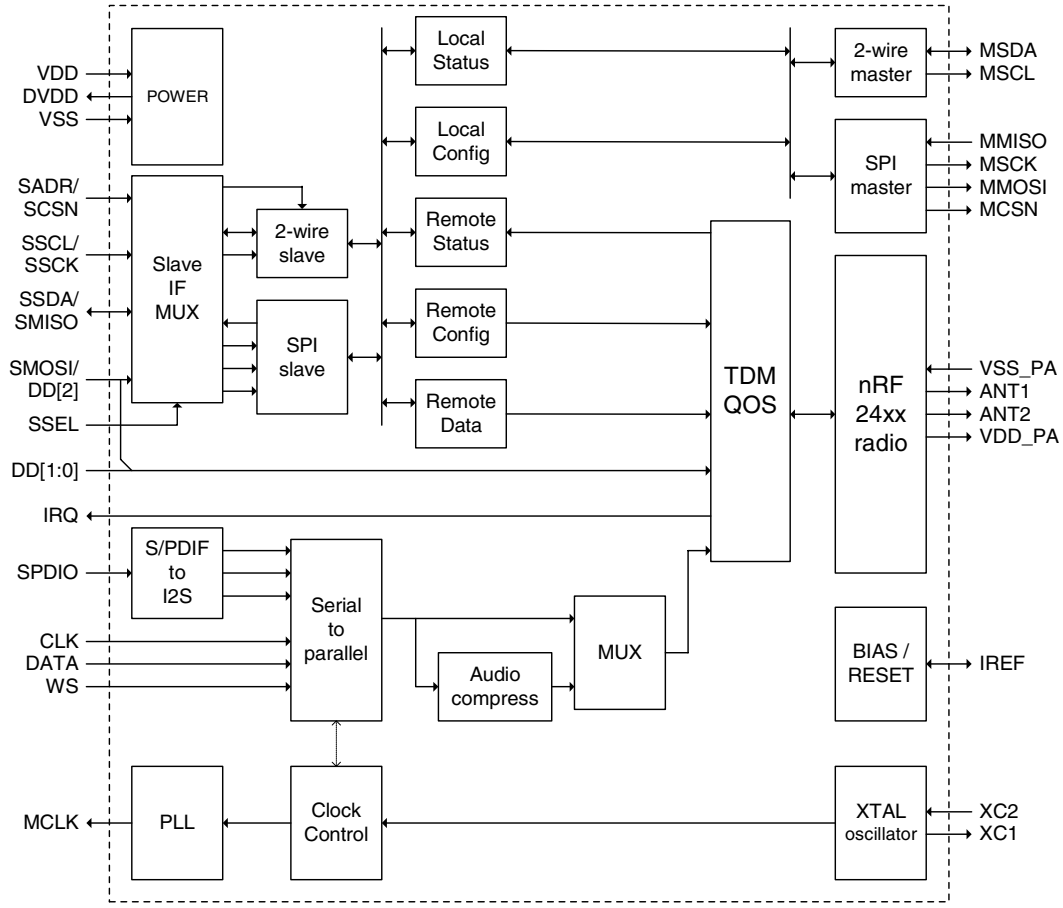


Figure 4-6 nRF24Z1 ATX mode block diagram

The I2S or S/PDIF interfaces can be used for audio data input, or alternatively.

4.4.1 I2S audio input

For seamless input from audio sources physically close to nRF24Z1, I2S is the preferred interface. The I2S interface consists of pins CLK, DATA and WS. This interface supports the 3 fundamental sampling rates 32, 44.1 and 48 kSPS plus these rates scaled by 0.5 or 0.25; yielding a total of 9 sample rates : 8, 11.025, 12, 16, 22.05, 24, 32, 44.1 and 48 kSPS. Data may be in 16 or 24 bit format.[1] The nRF24Z1 can be configured to automatically detect the applied data rate.

I2S may be used with an external stereo ADC for analog audio sources. The nRF24Z1 offers a sampling rate clock (f_S) of 256 times the audio fundamental sampling rate. The sample rate clock is available on the MCLK pin and may be used as system clock for the ADC.

4.4.2 S/PDIF audio input

The ATX also offers a (CMOS level) S/PDIF input on pin SPDIO. This interface supports 32, 44.1 or 48 kSPS sampling rates with resolution of 16, 20 or 24 bit, as well as linear and nonlinear audio according to IEC standards, see Ch. 7.2.2 for details.

4.4.3 Serial control (slave) interfaces

When ATX is controlled by an external MCU, configuration and control data for the audio transmitter and the linked audio receiver may be entered via a 2-wire or SPI slave serial interface. The same interface is used for reading back status information. The register map is identical for both interfaces, but only one of the interfaces (selected by SSEL pin) may be used in a given application.

The two interfaces are:

SSEL = 0; SPI (pins SCSN, SSCK, SMISO, SMOSI).
SSEL = 1; 2-wire (pins SADR, SSCL and SSDA)

Pin SADR is not part of a standard 2-wire interface but selects one of two possible bus addresses for the nRF24Z1.

[1] Only 16 bit format can be transferred uncompressed within the available 1.54 Mbit/s data rate.

4.4.4 Master interfaces

For standalone operation of nRF24Z1, a serial EEPROM or FLASH memory may be connected to an SPI or 2-wire master interface. If a memory is present at any of these interfaces during power up or reset, the device will read default configuration data from the memory.

The SPI master is found on pins MCSN, MMISO, MMOSI and MSCK and 2-wire master on pins MSDA and MSCL.

4.4.5 Direct data input pins

The ATX has 2 general purpose input pins, DD[1:0]. The status of these pins may be transmitted directly to the ARX without the use of an external MCU. When SSEL is set high (2-wire interface selected), an additional direct data pin (DD[2]) is available.
If the logic level on pins DD[2:0] are mirrored (copied) over the control channel, ARX pins DO[2:0] will output identical levels.
These pins may thus be used to switch on/off audio receiver peripherals without microprocessor activity.

4.4.6 Interrupt output

The nRF24Z1 can interrupt the external application through pin IRQ based on a number of sources (i.e. no audio input detected, loss of RF communication etc.).
Once IRQ has triggered external MCU, interrupt status can be read through the serial slave interface.

4.5 Audio Receiver (ARX)

When nRF24Z1 is put at the destination side of the RF link, MODE must be low and nRF24Z1 becomes the audio receiver (ARX). ARX can be configured with GPIO interface or slave interface, and the respective block schematics of nRF24Z1 in ARX mode can be seen in Figure 4-7 and Figure 4-8. I2S or S/PDIF are now used for audio or other real time data output.

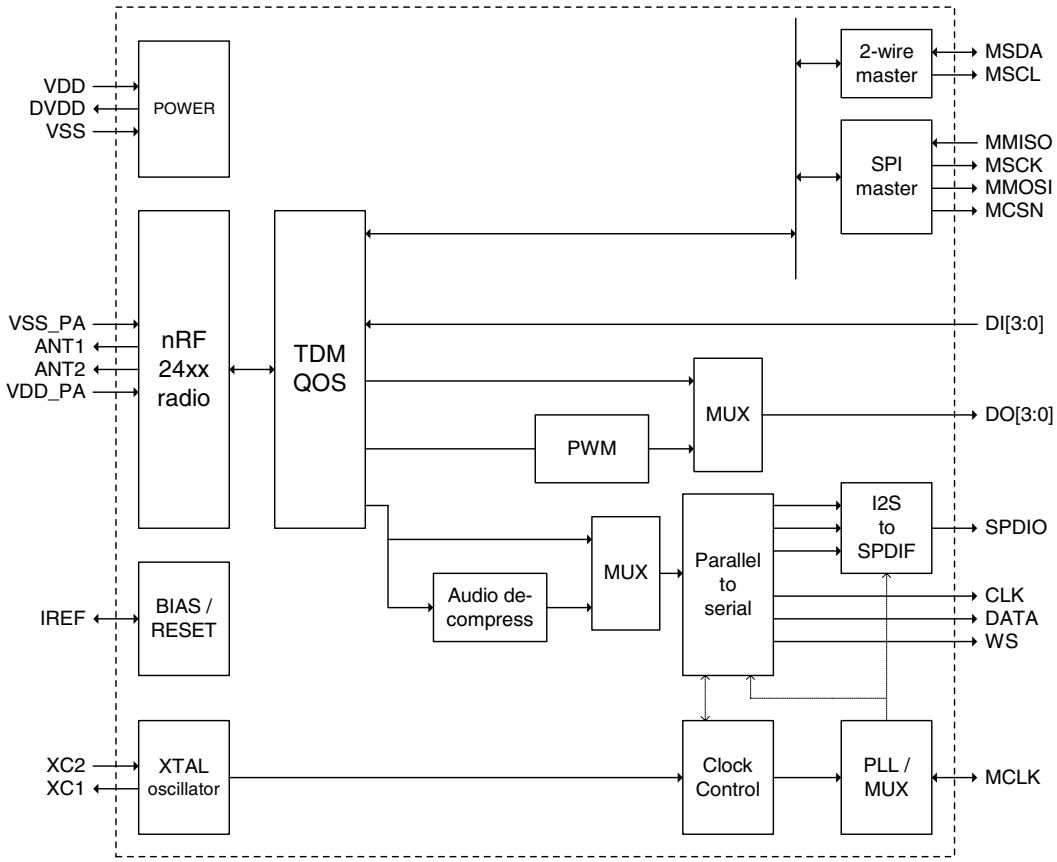


Figure 4-7 nRF24Z1 ARX mode with GPIO interface block diagram

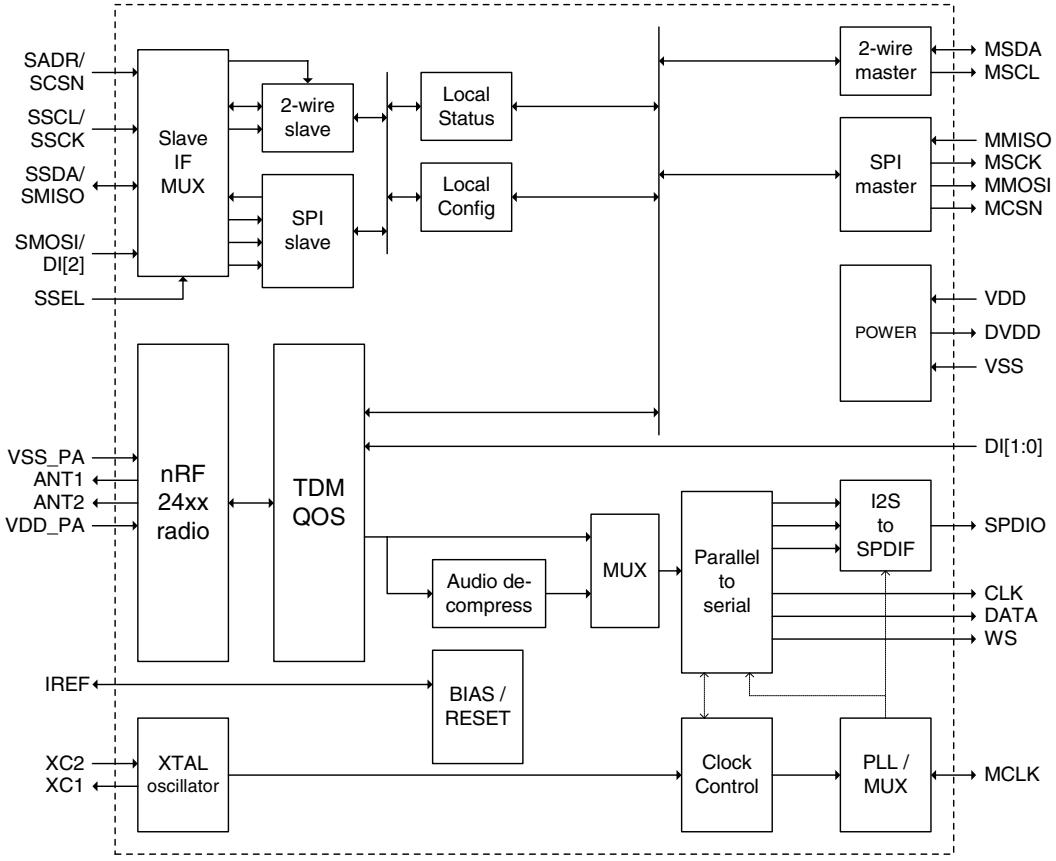


Figure 4-8 nRF24Z1 ARX mode with slave interface block diagram

After a link has been established, the user can control the SPI and 2-wire master on the ARX from the ATX. This feature enables the ATX to remotely control serial peripheral devices on the ARX (audio DACs, amplifiers etc.).

4.5.1 I2S audio output

Audio output to devices physically close to nRF24Z1 (typically a stereo DAC) are normally driven by the I2S output (pins CLK, DATA and WS). This interface supports the following sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1 and 48 kSPS. Audio rate on the ATX and ARX side must be identical. Data are in 16 bit format.

In audio receiver mode, the MCLK pin provides a sampling rate clock (f_S) of 256 times the audio fundamental sampling rate for an external DAC.

4.5.2 S/PDIF audio output

The ARX provides an S/PDIF (full swing CMOS) output on pin SPDIO. This interface supports 32, 44.1 and 48 kSPS, 16 or 24 bit data. Both linear and nonlinear audio may be received according to IEC standards, see Ch. 7.2.2 for details.

4.5.3 Master interfaces

A serial EEPROM or FLASH memory may be connected to a SPI or 2-wire master interface. If a memory is present at any of these interfaces during power up or reset, the device will read default configuration data from that memory. If not, hard coded default values will be used.

During audio receiver configuration, the SPI master (pins MMSCK, MMISO, MMOSI, MCSN) is operated at 1MHz with the SPI format set to CPOL=0,CPHA=0 for EEPROM/FLASH compatibility. After a link has been established, the user may control the SPI master from the audio transmitter. The available clock speed is up to 8 MHz over the full operational range of the device.

During start-up, the audio receiver operates the 2-wire master (MSDA, MSCL) interface at 100 kHz. After a link has been established, the user may control the 2-wire master from the audio transmitter to 100 kHz, 400 kHz or 1 MHz.

4.5.4 Serial control (slave) interfaces

When the ARX is controlled by an external MCU, configuration and control data for the audio receiver may be entered via a 2-wire or SPI slave serial interface. The same interface is used for reading back status information. The register map is identical for both interfaces, but only the interface selected by the SSEL pin may be used in a given application.

The two interfaces are:

SSEL = 0; SPI (pins SCSN, SSCK, SMISO, SMOSI).
SSEL = 1; 2-wire (pins SADR, SSCL and SSDA)

Pin SADR is not part of a standard 2-wire interface but selects one of two possible bus addresses for the nRF24Z1.

4.5.5 Parallel port and PWM

Alternatively to the serial slave interfaces, the ARX can be configured with an 8 bit parallel port, which can be controlled and read from the audio transmitter. The 4 input pins DI[3:0] are continuously monitored when a link is up. Changes on any of these inputs will be sent back to the audio transmitter where it can be accessed in a register (via the serial control interface). The audio receiver can also be programmed to wake up from power down mode upon a change of state on any of these pins.

There are 4 outputs DO[3:0] controlled from the audio transmitter. Pins DO[1] and DO[3] may be programmed for high current in order to drive application PCB LEDs or standard CMOS gates.

DO[3] may be programmed to provide a PWM signal, where the output duty cycle is programmable with 8-bit resolution from the audio transmitter. Note that this PWM cannot be used as an audio DAC.

The output pins DO[3:0] may also function as slave select signals if multiple slaves are present on the ARX SPI master bus.

4.6 Blocks and functionality common to the ATX and ARX

4.6.1 XTAL Oscillator

The crystal oscillator will provide a stable reference frequency with low phase noise for the radio and audio functions. See Ch. 17.2 for full crystal specification.

4.6.2 Radio Transceiver

The RF transceiver part of the circuit is a member of nRF24xx family of low power highly integrated 2.4GHz ShockBurst™ transceivers. The transceiver interface is optimized for high speed streaming of up to 4 Mbps. Output power and some radio protocol parameters can be controlled by the user via the Quality of Service (QoS) module.

4.6.3 Quality of Service (QoS) engine

The primary function of the QoS engine is to ensure robust communication between the ATX and the ARX in an audio streaming application.

Various data streams with different properties are handled. The available bandwidth is shared between audio data, service data and remote data.

Data integrity is ensured through a number of RF protocol features:

1. Packets of data are organized in frames with each packet consisting of an *RF address*, *payload* and *CRC*.

2. Packets that are lost or received with errors are handled by the error correction level of the quality of service engine; a two way, acknowledge protocol:
   When a packet is received by ARX, it is registered and CRC is verified. After ARX has received a frame, it sends a packet back to ATX acknowledging the packets successfully transferred. Packets lost or received with errors, are re-transmitted from ATX in the next frame.

3. The information (audio data) is dispersed over the 2.4 GHz band by use of an adaptive frequency hopping algorithm. This enables the nRF24Z1 link to cope with RF propagation challenges like reflections, multi-path fading and avoiding heavily trafficked areas of the 2.4 GHz band. Handling co-existence scenarios with contemporary RF systems such as Bluetooth, ZigBee, WLAN/WiFi as well as other nRF applications, is increasingly important.

The nRF24Z1 is constantly monitoring the quality of the RF link. Link quality information is available for external control devices in registers. nRF24Z1 can also be set to interrupt external controller devices upon poor link quality before the RF link is lost. An external controller device can hence take action in order to improve link quality or warn end user if RF link margins are poor.

The secondary function of the QoS module is to run a link initialization algorithm which manages initial connect and re-connect if link is lost (ex: out of range) between paired nRF24Z1's. Several schemes are available to enable nRF24Z1 connection without end user involvement.

4.6.4 Audio compression / decompression

An optional low latency compression option is available as an alternative to streaming of uncompressed audio.

The compression option enables 24-bit samples to be compressed to a 16-bit format by removing the least significant bits in the samples. All samples in a packet are scaled to the same exponent.

4.6.5 Power supply regulators

The power section of nRF24Z1 offers linear regulated supply to all internal parts of the device. This makes the device very robust towards external voltage supply noise and isolates (audio) devices in an application from any noise generated by the nRF24Z1.

4.6.6 Bias reference / RESET

The IREF pin sets up the bias reference for the nRF24Z1 by use of an external resistor. Shorting IREF to VDD will reset the device. When IREF pin is released, nRF24Z1 runs a full configuration procedure.

5 Operation overview

5.1 Power on / RESET sequence

When a power supply voltage is connected, nRF24Z1 performs a power-on-reset. Reset is held until the supply voltage has been above the minimum supply voltage for a few milliseconds. Pulling IREF to VDD will also put the device into reset.

When reset (power on or IREF high) is released, the device needs to be configured. There are 2 alternatives of nRF24Z1 configuration:

1. Upon reset release, nRF24Z1 will look for an external EEPROM/FLASH memory connected to the SPI master interface. If such a memory is present, configuration data is loaded, which implies that registers values are read from the external memory. If no memory is present on the SPI master interface, the procedure is repeated on the 2-wire master interface. If no SPI EEPROM is connected, MMISO must have an external pull down resistor to ground. Data in the external memory device will override any initial contents of nRF24Z1 registers.

2. If no external memory is present:
   An external micro processor must configure the nRF24Z1 ATX and ARX through the slave SPI or 2-wire serial interface, otherwise hard coded initial register contents are used.

   NOTE:
   A combination of the two power-up sequences may be used. One likely scenario is that the ATX is configured by an external MCU and that the ARX is configured from an external EEPROM/FLASH memory device.

nRF24Z1 will then start a link initialization procedure based on the link configuration data. The value of the MODE pin determines whether it will be in ATX or ARX mode.

In case an external EEPROM or Flash memory is present, please note that no access to the 2-wire slave interface should be started until configuration data from EEPROM/Flash is read in by the nRF24Z1.

5.2 RF Link initialization

The process of establishing a communication link between the ATX and the ARX is referred to as RF link initialization. This involves the ATX systematically probing the frequency band in search for an active ARX with the correct identity. Once found, the ATX/ARX are synchronized before audio transmission starts.

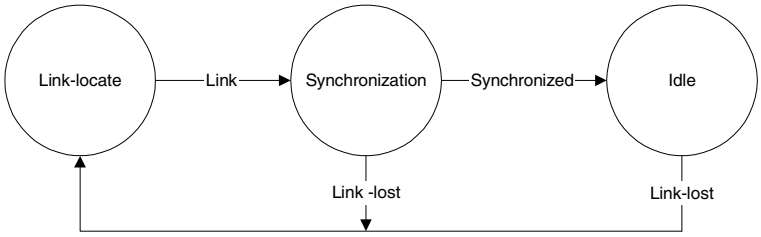


Figure 5-1 Link initialization algorithm

5.2.1 Idle state

The nRF24Z1 link initialization algorithm will be in idle state when a link is established. Once established, the frequency hopping engine is initiated and synchronized.

5.2.2 Link-locate state

If the link between ATX and ARX is broken, a special link-locate routine is initiated on both sides in order to re-establish the link, see Figure 5-1. During initialization, nRF24Z1 uses the NLCH first positions of the frequency hopping table (see Ch. 8.3).

5.2.2.1 Link-locate on ATX

The ATX tries to establish a link with ARX by iteratively sending short search packets on all available channels until an acknowledge signal is received from the ARX. The ATX will send one packet on each channel and wait for acknowledge for a time long enough to secure that the ARX has time to respond. The accumulated time used by the ATX while looping through all available channels, is defined as the ATX-loop-time. After receiving an acknowledge packet from the ARX, the ATX will enter the synchronization state as illustrated in Figure 5-1. The dwell time for linking (t_{DWELL_L}) is approx. 600µs. The dwell time is defined as *the time duration of which the ATX/ARX is active at a given frequency before changing frequency position.*

5.2.2.2 Link-locate on ARX

The ARX tries to establish a link with the ATX by listening for incoming search packets on all available channels. When a search packet is received, the ARX will proceed by sending one acknowledge packet to confirm a feasible link. The ARX will listen for incoming search packets on each channel for a fixed time longer than the ATX-loop-time. This guarantees at least one search packet to get through on each available channel used by the ARX, as long as this channel is not being occupied by another radio device. After sending the acknowledge packet, the ARX will enter the synchronization state. The dwell time is approx. (NLCH+1)·600µs (see Ch. 8.3).

5.2.3 Synchronization state

This state synchronizes the frequency hopping engine on ATX and ARX, ensuring that both units follows the same hopping sequence. The initial start frequency is found in link-locate mode.

5.3 Audio channel

The input audio data can be one of the following common digital audio formats:

I2S (audio serial) interface:

- Left justified, I2S and right justified.

S/PDIF interface:

- Consumer Linear PCM Audio as described in IEC 60958-3. As the nRF24Z1 has a single ended CMOS interface, external adaptation circuitry is needed in order to fulfil the electrical requirements.

- Non-Linear PCM Audio as described in IEC 61937-1 (General) and IEC 61937-2 (Burst-info). The nRF24Z1 communication channel is transparent and is thus compatible with the audio compression algorithm formats described in IEC 61937-3 to 61937-7.

In the ATX, the input audio stream format is converted to the nRF24Z1 RF protocol and transferred over the air.

Upon reception in the ARX, the received data are validated and converted to the specified audio output format and fed to the corresponding audio output interface.

5.3.1 Audio receiver clock rate recovery

Maintaining equal data rates on both sides of RF link is crucial in any RF system streaming true time data. This implies keeping the master clock frequency (MCLK) for the DAC on the receiving side, equal to the clock frequency used to feed data into the RF device on the transmitter side.

If these two clocks are not identical, the receiving end will either run out of samples for the DAC (ARX clock frequency > ATX clock frequency) or overflow (ARX clock frequency < ATX clock frequency), skipping samples.

This problem is solved in the nRF24Z1 device without the need for a tight tolerance crystal or extensive digital filtering.

As long as the nRF24Z1 QoS engine is able to maintain the RF link, the ARX locks its master clock output (MCLK) to the rate of the incoming audio stream. The MCLK signal on the ARX side is hence locked to the reference (crystal) of the device feeding audio data to the ATX, and *not* to the crystal of the nRF24Z1 ATX/ARX devices.

One exception; if the MCLK output option is used in the audio transmitter (i.e. clocking an external ADC), the nRF24Z1 ATX crystal is the reference for the audio speed on the entire nRF24Z1 link.

5.4 Control channel

A 2-way, low bit rate, control and signalling channel is running in parallel with the audio stream. This control channel is a part of the QoS overhead, i.e. difference between on the air data rate (4 Mbit/s) and the nominal audio data rate 1.5 Mbit/s. Data channel rate can hence not be traded for higher audio data rate. The functionality of the control channel is illustrated in Figure 5-2.

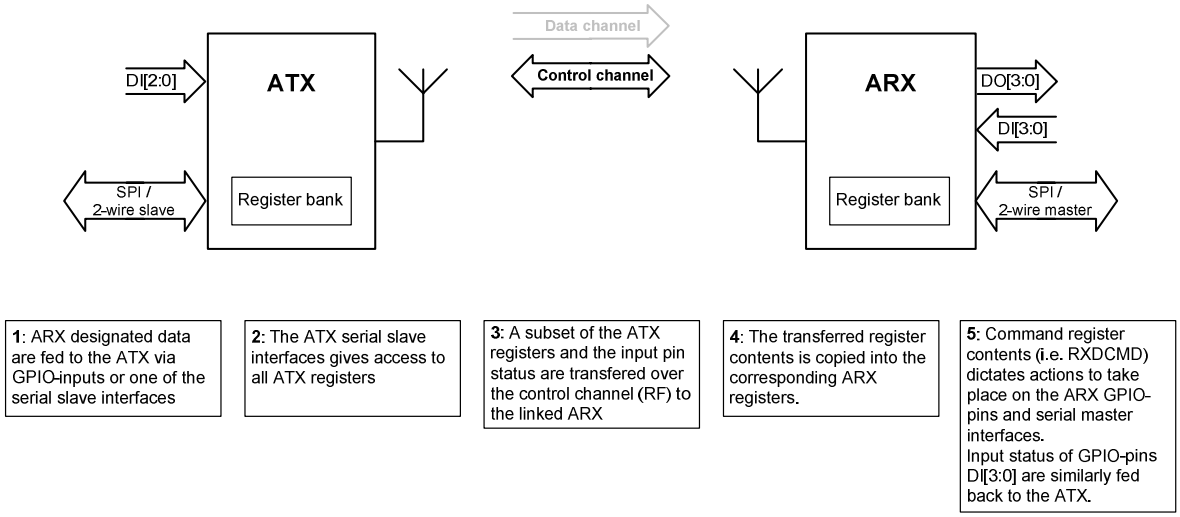


Figure 5-2 nRF24Z1 control channel transfer principle

Through the control channel the ATX has write access to a majority of registers which are related to ARX configuration. ATX can thereby access ARX GPIO (for LED's etc.) and the ARX 2-wire and SPI master interface for configuring of DAC's, volume control and other peripheral functions.

5.5 Power down mode

In Power down mode, the QoS engine is shut down, and only a low frequency oscillator and some timers are active. A timer time-out or an external pin event can be used to exit power down mode. Once power down mode is aborted, the link initialization routine is initiated as described in Ch. 5.2. The sleep and wake timers enable the nRF24Z1 to shut down on a cyclic basis if no transceiver counterpart is detected. The ARX may also be put out of power down mode by toggling a GPIO-pin.

6 nRF24Z1 register MAP

The nRF24Z1 control and status registers are listed in Table 6-1 and Table 6-2 below. The registers may be accessed by an external MCU via the slave interface (SPI or 2-wire). The registers are organized functionally into 7 groups; ATX, Link and ARX control and status, Data link and Test registers. All registers are present both in audio transmitter and audio receiver.
The initial value of all registers are read from EEPROM (if present) immediately after reset, otherwise the initial values in Table 6-1 and Table 6-2 apply.

6.1 Register access from the ATX side

If an MCU on the ATX side writes to a register, the corresponding ARX register is also updated if registers TXCSTATE, LNKCSTATE, RXCSTAT, RXEXEC are set. The ARX version of the register is updated via the control channel.

- Register TXCSTATE controls whether the ARX control registers are to be updated when writing to the *ATX control registers* (ref. Table 6-1)
- Register LNKCSTATE controls whether the ARX link control registers are to be updated when writing to the *Link control registers* (ref. Table 6-1)
- Register RXCSTATE controls whether the ARX control registers are to be updated when writing to the *ARX control registers* (ref. Table 6-1)

See Ch. 12 for details on control register updating by use of the control channel. Table 12-1 describes the above register update control registers.

An MCU on the audio transmitter side can read all registers in the ATX. In addition, the link status, ARX status and data link registers may be read from the audio receiver via the data link.

6.2 Register access from the ARX side

If an MCU on the audio receiver side writes to a register, only the audio receiver version of the register is written. This implies that the ATX MCU will not know about it, except that it can read back status register content via the data link.

An MCU on the audio receiver side can read all registers on its side, but it cannot read anything via the data link.

In brief, the ARX MCU only has local access, whilst the ATX MCU controls the data link.

Address Hex	Register	R/W	Initial Hex	Description
ATX registers				
0x01	TXSTA	R/W	0x80	Table 7-4, page 37
0x75	TXDD	R	0x00	Table 7-15, page 51
0x02	INTSTA	R/W	0x00	Table 9-1, page 67
0x5A	TXMOD	R/W	0x00	Table 7-6, page 38
0x51	TXFMT	R/W	0x00	Table 7-5, page 38
0x52	TXLAT	R/W	0x00	Table 8-6, page 65
0x53	INTCF	R/W	0x00	Table 9-1, page 67
0x54	I2SCNF_IN	R/W	0x00	Table 7-7, page 39
0x56	TXPWR	R/W	0x00	Table 8-7, page 66
0x57 - 0x58	TXSTI[0:1]	R/W	0x00	Table 11-2, page 73
0x59	TXWTI	R/W	0x00	Table 11-2, page 73
0x4D	TXLTI	R/W	0x00	Table 11-2, page 73
0x50	TXRESO	R/W	0x00	Table 10-1, page 69
0x5B	TXCSTATE	R/W	0x00	Table 12-1, page 76
LINK status registers				
0x03	LNKSTA	R/W	0x00	Table 8-5, page 65
0x04	LNKQ	R	0x00	Table 8-4, page 64
0x05	LNKERR	R	0x00	Table 8-4, page 64
LINK control registers				
0x0C- 0x31	CH[0:37]	R/W	0x00	Table 8-2, page 62
0x33	NBCH	R/W	0x00	Table 8-3, page 63
0x34	NACH	R/W	0x00	Table 8-3, page 63
0x35	NLCH	R/W	0x00	Table 8-3, page 63
0x36	LNKMOD	R/W	0x00	Table 8-5, page 65
0x37	LNKWTH	R/W	0x00	Table 8-4, page 64
0x38	LNKETH	R/W	0x00	Table 8-4, page 64
0x39 -0x3D	ADDR[0:4]	R/W	0x00	Table 8-1, page 60
0x3E	LNKCSTATE	R/W	0x00	Table 12-1, page 76
ARX status registers				
0x06	RXSTA	R	0x00	Table 7-16, page 54
0x07	RXPIN	R	0x00	Table 7-18, page 55
ARX control registers				
0x4A	RXMOD	R/W	0x00	Table 7-8, page 40
0x41	RXPIO	R/W	0x00	Table 7-20, page 56
0x42	RXPWME	R/W	0x00	Table 7-21, page 56
0x43	RXPWMD	R/W	0x00	Table 7-21, page 56
0x44	I2SCNF_OUT	R/W	0x00	Table 7-8, page 40
0x45	RXWAKE	R/W	0x00	Table 11-1, page 71
0x49	RXPWR	R/W	0x00	Table 8-7, page 66
0x46 - 0x47	RXSTI[0:1]	R/W	0x00	Table 11-2, page 73
0x48	RXWTI	R/W	0x00	Table 11-2, page 73
0x4C	RXLTI	R/W	0x00	Table 11-2, page 73
0x40	RXRESO	R/W	0x00	Table 10-1, page 69
0x4B	RXCSTATE	R/W	0x00	Table 12-1, page 76

Table 6-1 nRF24Z1 register listing

Address Hex	Register	R/W	Initial Hex	Description
Data link registers				
0x70	RXDCMD	R/W	0x00	Table 7-10, page 44
0x71	RXWCNT	R/W	0x00	Table 7-11, page 45
0x72	RXRCNT	R/W	0x00	
0x60-0x6f	RXBUF	R/W	0x00	
0x74	RXEXEC	R/W	0x00	
Test registers				
0x7E	TESTREG	R/W	0x00	Table 13-1, page 78
0x7F	TESTCH	R/W	0x00	
0x7D	REVBYT	R	0x20[1]	Revision byte

Table 6-2 nRF24Z1 register listing (continued)

6.3 Register map in external EEPROM

The table below shows the layout of the first few bytes of the EEPROM image.

Byte number	7	6	5	4	3	2	1	0
0	Reserved (must be 0000 0011)							
1	Reserved (must be 0000 0000)							
2	Reserved (must be 0000 0000)							
3	Value of register address 0x00							
4	Value of register address 0x01							
…	…							
127	Value of register address 0x7C							

Table 6-3 EEPROM layout

Bytes 3 to 127 are used to set initial values into all nRF24Z1 registers. The initial value of nRF24Z1 register address n, must be put in EEPROM byte n+3.

Registers 0x7D to 0x7F are *not* read from the EEPROM. The minimum EEPROM size is thus 128 bytes.

Designated EEPROM 2-wire slave address is 0xA0 for write and 0xA1 for read operations.

See ch. 4.5.3 for EEPROM interface description.

[1] REVBYT value is 0x20 for nRF24Z1 version B and C.

7 Digital I/O

This section describes the digital I/O pins, control registers and important interface timing of the nRF24Z1.

The digital I/O pins are divided into three groups:

1. Audio interfaces
2. Serial master interfaces
3. Control and GPIO interfaces

7.1 Digital I/O behaviour during RESET

During reset, all digital pins, except the master SPI interface output pins, are set as inputs to avoid driving conflicts with external devices. The master SPI pins; MCSN, MSCK and MMOSI are set to output high state. This sets the SPI interface to inactive state, ready to read the EEPROM configuration data clocked in immediately after reset. All pins will maintain their respective directions until any of the configuration read routines described in Ch. 5.1 is completed. The I/O pins are then set according to the new configuration data.

7.2 Audio interfaces

The audio interfaces consist of the I2S and S/PDIF interfaces plus the MCLK pin.

Pin name	Function
CLK	bit clock
WS	word sync clock
DATA	audio data
MCLK	256 · audio fundamental sample rate output, see Table 7-4 .
SPDIO	S/PDIF serial input or output, see Ch. 7.2.2.

Table 7-1 Serial audio port pins

7.2.1 I2S Audio Interface

The nRF24Z1 has a three-wire serial audio interface which can be configured to be compatible with various serial audio formats. In ATX mode, the audio interface is in slave or master input mode. In ARX mode, the audio interface is in master output mode. The audio interface consists of 6 pins in total, see Table 7-1.

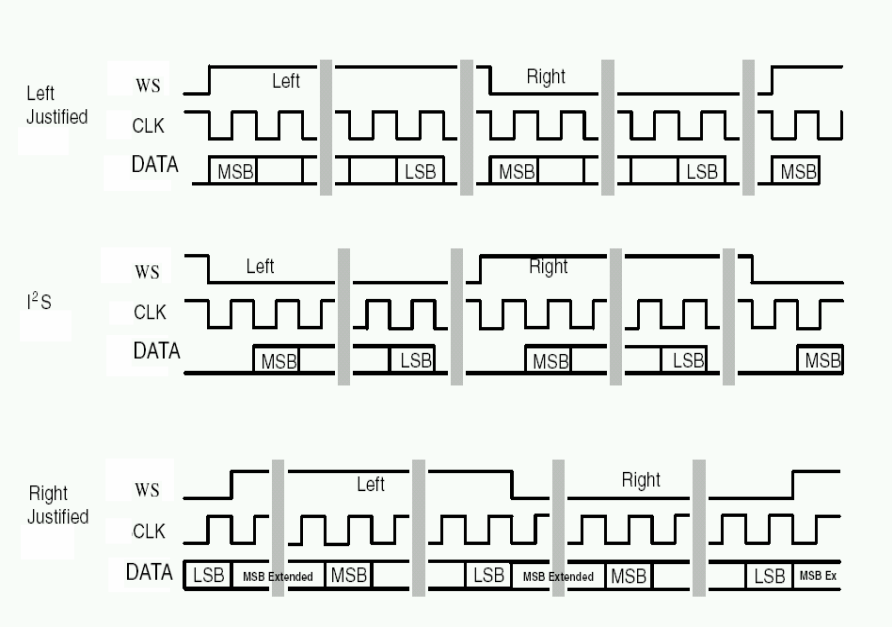


Figure 7-1 Serial audio formats I2S, left- and right justified

Audio format	I2SCNF[3:0] value
Left justified	0xA
I2S	0x0
Right Justified	0xB

Table 7-2 I2SCNF settings for three common serial audio formats (applies to I2SCNF_IN and I2SCNF_OUT registers).

See also Table 7-6 and Table 7-8.

7.2.2 S/PDIF Audio Interface

nRF24Z1 supports the following S/PDIF interface formats:

- Consumer Linear PCM Audio described in IEC 60958-3. Due to the single ended CMOS interface of the nRF24Z1, external adaptation circuitry is needed in order to fulfil the electrical requirements.

- Non-Linear PCM Audio, as described in IEC 61937-1 (General) and IEC 61937-2 (Burst-info). The nRF24Z1 is transparent to the specific audio compression algorithms used, transferring 16 bits of each audio sample from the ATX to the ARX. In addition, the 32 first bits of channel status information is transferred (but none of the other S/PDIF aux/data bits).

The S/PDIF valid bit is not transferred, and is always output as 0 (zero).

Only one of the audio interfaces can be active at any time. The active audio interface for ATX is set by bit 2 in register TXMOD (TXMOD[2] = 0; I2S, is the default value, see Table 7-6). ARX audio interface is set by bit 2 in register RXMOD.

7.2.3 Audio interface functionality

The functionality and direction of the pins in the audio interfaces are listed in Table 7-3.

		ARX (MODE=0)				**ATX** (MODE =1)				
		I2S (TXMOD[2]=0)		**S/PDIF** (TXMOD[2]=1)		**I2S** (TXMOD[2]=0)			**S/PDIF** (TXMOD[2]=1)	
Pin No.	**Pin name**	**Function**	**Direction**	**Function**	**Direction**	**Function**	**Audio slave**	**Audio master**	**Function**	**Direction**
							Direction			
10	CLK	CLK	OUT	X	IN	CLK	IN	OUT	X	IN
11	WS	WS	OUT	X	IN	WS	IN	OUT	X	IN
12	DATA	DATA	OUT	X	IN	DATA	IN	IN	X	IN
13	SPDIO	X	IN	SPDIO	OUT	X	IN	IN	SPDIO	IN
		RESET*	OUT			RESET*	OUT	OUT		
14	MCLK	MCLK	OUT	X	OUT	MCLK	OUT	OUT	X	OUT

Table 7-3 nRF24Z1 operational modes and audio interface pin functions

* If S/PDIF is not used for audio, the SPDIO pin can be used as RESET (output) to external devices. See chapter 10 for further details.

7.2.4 ATX audio interface control

In audio slave mode (see I2SCNF_IN bit 7), the ATX may be configured for automatic detection of the sampling rate of the input audio from an external master on the I2S interface (exception being 16 kSPS, see [1]), or the sampling rate can be set into register TXSTA.

In audio master mode the sampling rates must be set in register TXSTA, and 16kSPS is not allowed.

S/PDIF audio rate is always auto detected, but TXMOD bits 1:0 must be set.

Register TXSTA contains the detected data rate status for optional read back to an external MCU.

Address Hex	Register	R/W	Description	
0x01	TXSTA	R/W	ATX audio input rate register	
			Bit	Interpretation
			7	Reserved
			6:5	Audio rate scale factor (I2S only) if TXSTA bit 0 is set : audio rate is auto detected by hardware if TXSTA bit 0 is not set : audio rate must be set by user
			00	0.25
			01	0.5
			10	1
			11	Reserved
			4:3	Audio fundamental rate if TXSTA bit 0 is set : audio rate is auto detected by hardware if TXSTA bit 0 is not set : audio rate must be set by user
			00	48 kSPS
			01	44.1 kSPS
			10	32 kSPS
			11	Illegal or no input detected
			2:1	Reserved
			0	Value / Description
				1 – Audio input rate is auto detected by hardware
				0 – Audio input rate must be set by user

Table 7-4 Audio input status register

New values in TXSTA will take effect after the ATX and ARX have been reconfigured, this is done by setting LNKMOD[4] = 1.

[1] Auto detect of 16kSPS sampling rate is not supported in ATX audio slave mode, but can be used without auto detect enabled. Example : setting TXSTA=0x31 and I2SCNF_IN.7=0 is illegal, but TXSTA=0x30 and I2SCNF_IN.7=0 is allowed. And for ATX audio master mode, TXSTA=0x30 and I2SCNF_IN.7=1 is not allowed.

By default, nRF24Z1 transfers uncompressed audio, but may optionally transfer compressed audio data. Data compression enables transfer of 24 bit audio, which uncompressed would exceed the available radio bandwidth. Data rate reduction also reduces overall current consumption.
Data compression is based on removal of sample LSB's.

Example: 24 to 16 bit compression principle. If the sample values within a packet are within +/- 200000, the 3 LSB's are removed. If the sample values in the consecutive packet are within +/- 60000, only 1 LSB is removed. In effect, the number of LSBs truncated varies dynamically with maximum sample value for each packet, limiting the relative error.

Address Hex	Register	R/W	Description
0x51	TXFMT	R/W	Transmit data format Value: Interpretation 0: 16 bit linear PCM 1: 24 bit linear companded to 16 bit other: Reserved, MBZ

Table 7-5 TXFMT register

New values in TXFMT take effect after ATX and ARX are reconfigured, this is done by setting LNKMOD[4] = 1.

The Audio interfaces in ATX mode are controlled by the registers listed in Table 7-6 and Table 7-7.

Address Hex	Register	R/W	Description
0x5A	TXMOD	R/W	Audio transmitter modes of operation 7: RF transceiver enable 6: Audio transmitter power down 5: Enable wakeup on changing DD[1] 4: Reserved, MBZ 3: Enable direct data from pins DD[2:0]. DD[2] is only available if SSEL=1 2: S/PDIF enable (default input is I2S) [1] 1:0: MCLK output control [1] 00: MCLK off (logic 0) 01: Output 256 x 48 kSPS 10: Output 256 x 44.1 kSPS 11: Output 256 x 32 kSPS

Table 7-6 ATX audio input control register TXMOD

[1] IMPORTANT NOTICE: For S/PDIF audio input, the MCLK output is disabled. However the MCLK control value TXMOD[1:0] must generally be set to the expected sampling rate. This is mandatory if 32 kSPS sampling rate is expected, and recommended otherwise.

Address Hex	Register	R/W	Description
0x54	I2SCNF_IN	R/W	I2S interface configuration (on ATX side), see also Table 7-2

7	I2S audio in clock mode	
	0	Slave mode, WS,CLK,DATA are input
	1	Master mode, WS,CLK are output, DATA is input
6	Reserved, MBZ	
5:4	Sample length	
	00	16-bit samples
	10	24-bit samples
	other	Reserved
3	WS Polarity	
	0	WS=0: Left sample
	1	WS=1: Left sample
2	Data to Bit Clock relation (data valid at clock edge)	
	0	Rising Edge
	1	Reserved
1	WS to MSB delay	
	0	1 clock cycle
	1	0 clock cycles
0	Audio word justification	
	0	Left justified
	1	Right justified

Table 7-7 ATX audio input control register I2SCNF_IN

New values in TXMOD and I2SCNF_IN take effect after ATX and ARX are reconfigured. This is done by setting LNKMOD[4] = 1.

For analog audio sources, the nRF24Z1 offers a 256x clock output on pin MCLK. Clock frequency is set in register TXMOD[1:0]. This clock may be used as system clock in applications incorporating an external stereo ADC.

7.2.5 ARX audio interface control

In ARX mode the audio interfaces are controlled by registers 0x4A and 0x44 listed below.

<table>
<tr><th>Address Hex</th><th>Register</th><th>R/W</th><th>Description</th></tr>
<tr><td>0x4A</td><td>RXMOD</td><td>R/W</td><td>Audio receiver modes of operation
<table>
<tr><th>Bit</th><th>Interpretation</th></tr>
<tr><td>7</td><td>Audio receiver power down</td></tr>
<tr><td>6</td><td>Reserved, MBZ</td></tr>
<tr><td>5</td><td>RF transceiver enable</td></tr>
<tr><td>4</td><td>Reserved, MBZ</td></tr>
<tr><td>3</td><td>Reserved, MBZ</td></tr>
<tr><td>2</td><td>S/PDIF enable</td></tr>
<tr><td>1:0</td><td>Reserved, MBZ</td></tr>
</table></td></tr>
<tr><td>0x44</td><td>I2SCNF_OUT</td><td>R/W</td><td>I2S interface configuration for audio output (ARX side), see also Table 7-2
<table>
<tr><th>Bit</th><th>Interpretation</th></tr>
<tr><td>7</td><td>Reserved, MBZ</td></tr>
<tr><td>6</td><td>Mute sound output</td></tr>
<tr><td>5:4</td><td>Reserved MBZ</td></tr>
<tr><td>3</td><td>WS Polarity
0 WS=0: Left sample
1 WS=1: Left sample</td></tr>
<tr><td>2</td><td>Data to Bit Clock relation (data valid at clock edge)
0 Rising edge
1 Falling edge</td></tr>
<tr><td>1</td><td>WS to MSB delay
0 1 clock cycle
1 0 clock cycles</td></tr>
<tr><td>0</td><td>Audio word justification
0 Left justified
1 Right justified</td></tr>
</table></td></tr>
</table>

Table 7-8 ARX audio interface control registers

RXMOD is automatically sent from the ARX to the ATX during the link-locate procedure.

New values in I2SCNF_OUT take effect after ATX and ARX are reconfigured, this is done by setting LNKMOD[4] to “1”, except bit 6 MUTE which takes effect immediately after being received by the ARX. Note that MUTE forces the audio output sample values to zero instantly without any filtering.

Note that the ARX registers can be accessed by the audio transmitter through the control channel.

7.2.6 I2S Audio interface timing

7.2.6.1 I2S input (ATX) timing

The I2S input protocol may be configured in register I2SCNF_IN to handle various I2S formats The interface will automatically detect sample size and word length for the most common formats. This section describes the detailed bit-, clock- and word timing requirements for audio slave and audio master mode (as set by I2SCNF_IN.7).

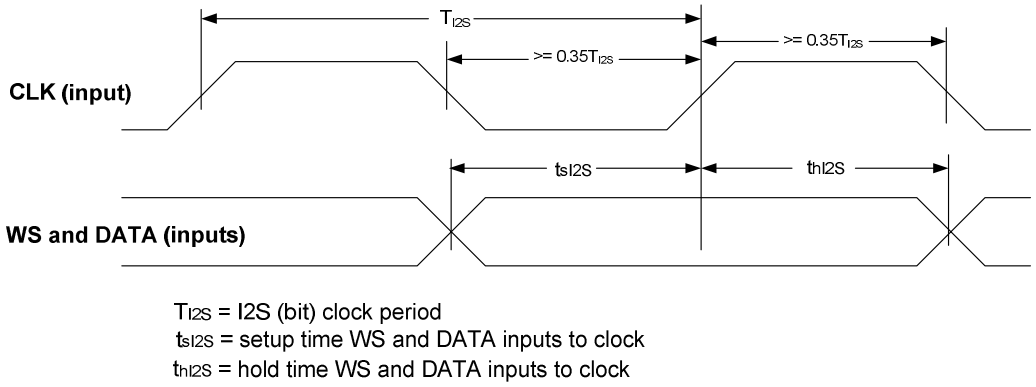


Figure 7-2. I2S input timing in audio slave mode (I2SCNF_IN[7]=0)

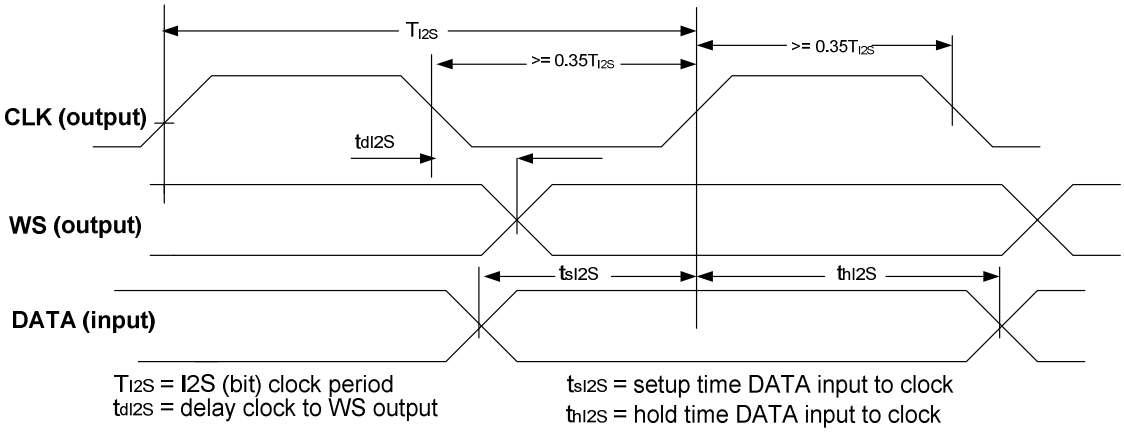


Figure 7-3. I2S input timing in audio master mode (I2SCNF_IN[7]=1)

Refer to Table 14-1 for values.

7.2.6.2 I2S output (ARX) timing

The I2S output protocol is configurable in register I2SCNF_OUT and is compatible with most I2S DACs and CODECs.

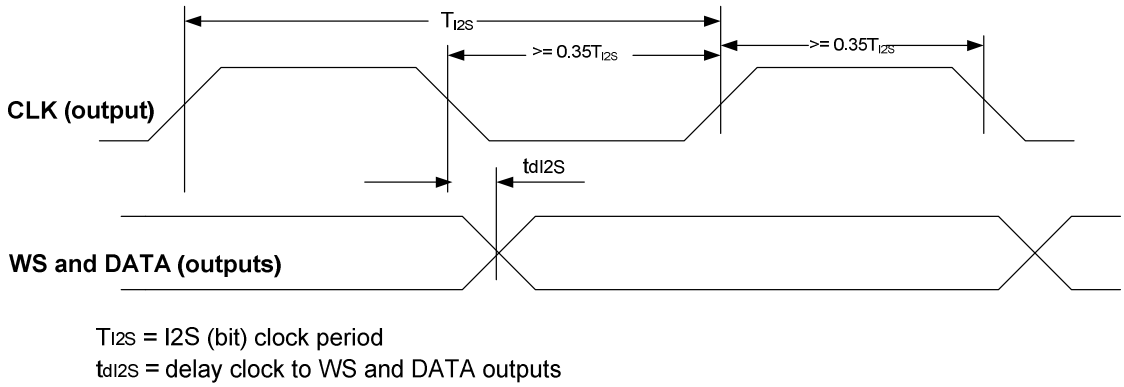


Figure 7-4. I2S output timing, for values see Table 14-1

7.3 Serial master interfaces

The nRF24Z1 serial master interface contains an SPI and a 2-wire master interface available at all times.

After RESET, the nRF24Z1 will search for a serial memory on the SPI master interface. If no memory is present, the process is repeated on the 2-wire interface. If no external memories are found, it is assumed that an external microcontroller is used to configure the device. The nRF24Z1 will then be idle until MCU based configuration is initiated over one of the slave control interfaces. Link initialization will start as soon as the necessary control register bits are set.

During configuration, the SPI master is operated at 1MHz. SPI format is CPOL=0, CPHA=0 as used by industry standard EEPROM/FLASH memories.
The nRF24Z1 is protocol compatible with SPI memory with sizes ranging from 1 Kbyte to 64 Kbytes with 16-bit sub-address used.

The connected slave(s) determines the protocol on the 2-wire master interface. During configuration, nRF24Z1 is protocol compatible with industry standard 2-wire memories. Memory size may range from 128 bytes to 4 Kbytes (with 3 address pins and one byte sub-address used). Designated slave address is 0xA0 for write and 0xA1 for read operations. During configuration this interface is operated at 100 kHz , compatible with most serial 2-wire memories.

The pin out and functionality of the serial master I/O pins are shown in Table 7-9.

		ARX (MODE=0)				**ATX** (MODE =1)			
		2-wire interface RXDCMD[7] = 0		**SPI** RXDCMD[7] = 1		**2-wire interface** 2-wire EEPROM		**SPI** SPI EEPROM	
Pin	**Name**	**Function**	**Direction**	**Function**	**Direction**	**Function**	**Direction**	**Function**	**Direction**
27	MSDA	MSDA	IN/OUT	X	IN	MSDA	IN/OUT	X	IN
				RESET[1]	OUT			RESET[1]	OUT
28	MSCL	MSCL	IN/OUT	X	IN	MSCL	IN/OUT	X	IN
29	MSCN	MSCN	OUT	MSCN	OUT	MSCN	OUT	MSCN	OUT
30	MMISO	X	IN	MMISO	IN	X	IN	MMISO	IN
31	MMOSI	X	IN	MMOSI	OUT	X	IN	MMOSI	OUT
		RESET[1]	OUT			RESET[1]	OUT		
35	MSCK	X	IN	MSCK	OUT	X	IN	MSCK	OUT

Table 7-9 Serial masters functionality

The ATX master interfaces may only be used for initial configuration. The ARX interfaces become an extension of the ATX interface through the control channel.

The serial master interface setup of the ARX is controlled by ATX via the link, by register RXDCMD (0x70) as shown in Table 7-10.

[1] A pin in the serial interface NOT being used for external memory and/or controlling external circuitry can be configured to act as reset for external devices (i.e. ADC/DAC). Refer to Chapter 10 for further details.

<table>
<tr><th>Address Hex</th><th>Register</th><th>R/W</th><th>Description</th></tr>
<tr><td>0x70</td><td>RXDCMD</td><td>R/W</td><td>
Data command. Specifies master interface and speed
<table>
<tr><th>Bit</th><th>Interpretation</th></tr>
<tr><td>7</td><td>Interface select
<table>
<tr><td>0</td><td>ARX 2-wire interface</td></tr>
<tr><td>1</td><td>ARX SPI interface</td></tr>
</table></td></tr>
<tr><td>6:4</td><td>For SPI:
Slave select control. Definition of slave select signals and associated polarity. If 2-wire configuration EEPROM is used, the DO-pin used as slave select signal, must have external pull up/down resistor to the defined inactive state of the external device.
For 2-wire interface:
Access type.
<table>
<tr><th>Value</th><th>SPI interpretation</th></tr>
<tr><td>000</td><td>CSN, active low [2]</td></tr>
<tr><td>001</td><td>DO[0], active low [1]</td></tr>
<tr><td>010</td><td>DO[1], active low [1]</td></tr>
<tr><td>011</td><td>DO[2], active low [1]</td></tr>
<tr><td>100</td><td>CSN, active low [2]</td></tr>
<tr><td>101</td><td>DO[0], active high [1]</td></tr>
<tr><td>110</td><td>DO[1], active high [1]</td></tr>
<tr><td>111</td><td>DO[2], active high [1]</td></tr>
<tr><th>Value</th><th>2-wire interpretation</th></tr>
<tr><td>000</td><td>start stop access [3]</td></tr>
<tr><td>001</td><td>Start only access [4]</td></tr>
</table>
Notes:
1. In order to use any of DO[2:0] as SPI slave select signals, the corresponding bit in the RXPIO-register should be set to the SPI slave select inactive state (i.e. if DO[0] is to be used as active low slave select, RXPIO[0] must be set to 1).
2. MCSN is always active low
3. Example of a 2-wire start stop access is shown in Figure 7-8.
4. A start only access is used to form a 2-wire repeated start access, shown in Figure 7-9. A repeated start access consists of a start only access command, followed by a start stop access command.</td></tr>
<tr><td>3:1</td><td>Interface data rate select
<table>
<tr><th>Value</th><th>SPI Interpretation</th><th>2-wire Interpretation</th></tr>
<tr><td>000</td><td>8 Mbit/s</td><td>Illegal</td></tr>
<tr><td>001</td><td>8 Mbit/s</td><td>100 kbit/s</td></tr>
<tr><td>010</td><td>4 Mbit/s</td><td>400 kbit/s</td></tr>
<tr><td>011</td><td>2 Mbit/s</td><td>1 Mbit/s</td></tr>
<tr><td>100</td><td>1 Mbit/s</td><td>Illegal</td></tr>
<tr><td>101</td><td>500 kbit/s</td><td>Illegal</td></tr>
<tr><td>110</td><td>250 kbit/s</td><td>Illegal</td></tr>
<tr><td>111</td><td colspan="2">No master interface access</td></tr>
</table></td></tr>
<tr><td>0</td><td>Reserved, MBZ</td></tr>
</table>
</td></tr>
</table>

Table 7-10 RXDCMD register

Values in RXDCMD are used when 0x01 is written to RXEXEC.

The number of bytes data to read from (or write to) the master interface, is set in the 'write and read count' registers RXWCNT (0x71) and RXRCNT (0x72). The actual data are transferred via the data buffers RXBUF.

Once the RXWCNT and RXRCNT registers are set, writing to RXEXEC will initiate a SPI or 2-wire operation on the ARX serial master interfaces. Completion of this operation is also reported in the RXEXEC register and can be mapped to an interrupt in the ATX. See also Figure 5-2 nRF24Z1 control channel. Values in registers RXWCNT, RXRCNT, and RXBUF are used when 0x01 is written to RXEXEC. If no data is to be exchanged on the master interface, the "Speed select" setting in register RXDCMD should be set to "No master interface access".

Address Hex	Register	R/W	Description
0x71	RXWCNT	R/W	Number of bytes to write (max 16) to master interface
0x72	RXRCNT	R/W	Number of bytes to read (max 16) from master interface
0x60 - 0x6F	RXBUF	R/W	Data to be written to the interface specified by RXDCMD, or Data read from audio receiver on the interface specified by RXDCMD
0x74	RXEXEC	R/W	Writing to this register will execute a command on the audio receiver. The interface and speed are specified by RXDCMD. The audio receiver will first write RXWCNT bytes from RXBUF to the selected interface. Afterwards RXRCNT bytes are read and transmitted back to be stored in RXBUF. An interrupt may be delivered upon successful completion of the command. Returned values are : 0 : idle, last transfer was successful 1 : busy with a write or read command 2 : idle, last transfer was unsuccessful MCU must set RXEXEC=1 to perform a command, and can thereafter poll RXEXEC to see if the command is finished (idle)

Table 7-11 ARX master data registers

7.3.1 Timing serial master interfaces

7.3.1.1 2-wire master timing

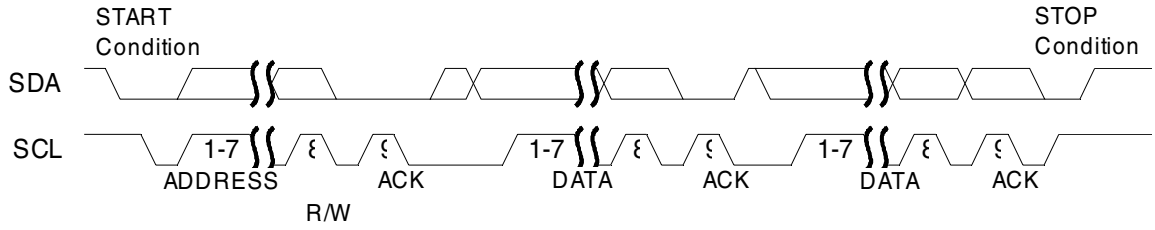


Figure 7-5 2-wire data transfer

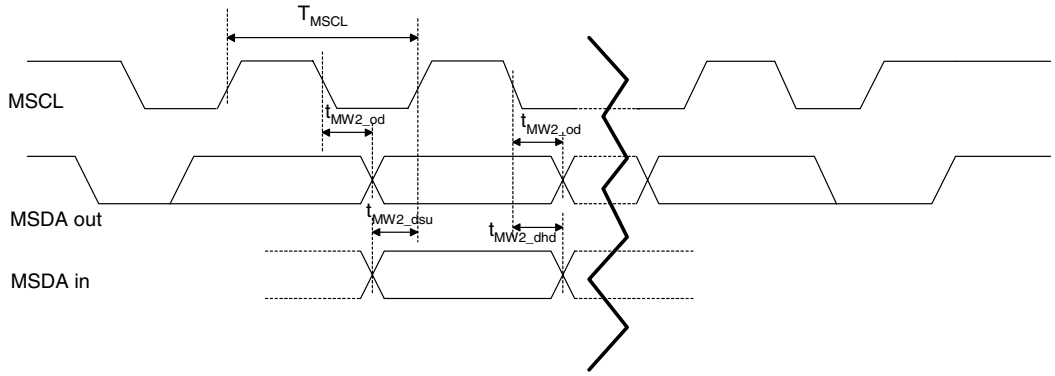


Figure 7-6 2-wire master timing (for values see Table 14-1)

7.3.1.2 SPI master timing

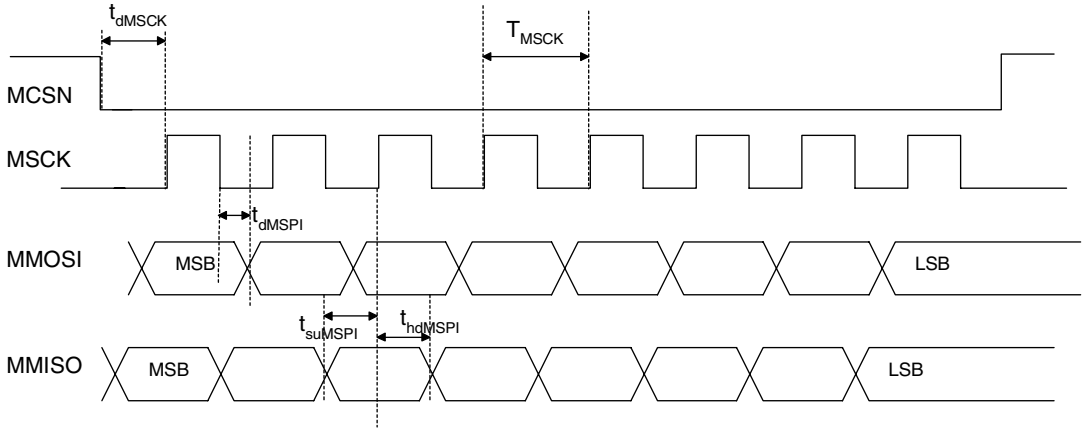


Figure 7-7 SPI master interface timing (one byte transaction shown).

T_{MSCK} : MSCK cycle time, as defined by RXDCMD register.
t_{dMSCK} : time from MCSN active to first SCK pulse, $t_{dSCK} = T_{MSCK} / 2$
t_{dMSPI} : delay from the negative edge of MSCK to new MMOSI output data
t_{suMSPI} : MMISO setup time to the positive edge of MSCK.
t_{hdMSPI} : MMISO hold time to the positive edge of MSCK.

Refer to Table 14-1 for values.

7.4 Control and GPIO interfaces

The following control and GPIO interfaces are available:

- ATX: SPI or 2-wire slave interfaces and general purpose inputs (DD [2:0])
- ARX: SPI or 2-wire slave interfaces as for ATX, or GPIO pins DI[3:0] and DO[3:0]. DO[3:0] pins have alternative functionality: PWM or master SPI chip select signal

External applications / devices control the nRF24Z1 by means of the ATX serial slave interfaces. If an external MCU is not present at the ATX side, configuration can only be done immediately after RESET (Ch. 7.3). All audio and RF link configuration is then fixed and the control channel can only carry simple push button/interrupt signals.

7.4.1 ATX interface and pin configuration

One of two interfaces can be chosen (set by input pin SSEL):

SSEL = 0; SPI (pins SCSN, SSCK, SMISO, SMOSI).
SSEL = 1; 2-wire (pins SADR, SSCL and SSDA)

The functionality and signal direction of the pins in ATX mode is listed in Table below.

nRF24Z1 GPIO and serial slave interface pins		**ATX mode**			
		Device control: SPI mode (SSEL = 10)		**Device control: 2-wire mode** (SSEL =11)	
Pin	**Name**	**Function**	**Direction**	**Function**	**Direction**
1	SSEL	SSEL	IN	SSEL	IN
2	SMISO/SSDA	SMISO	OUT	SSDA	IN/OUT
3	SSCK/SSCL	SSCK	IN	SSCL	IN/OUT
4	SCSN/SADR	SCSN	IN	SADR	IN
6	SMOSI/DD[2]	SMOSI	IN	DD[2]	IN
7	DD[1]	DD[1]	IN	DD[1]	IN
8	DD[0]	DD[0]	IN	DD[0]	IN
26	MODE	MODE	IN	MODE	IN
36	IRQ	IRQ	OUT	IRQ	OUT

Table 7-12 ATX Control and GPIO pins functionality

7.4.2 SPI slave interface

The first byte of the SPI transaction specifies the register address and whether it is a read or a write access. The seven least significant bits in the first byte is the nRF24Z1 register address, while the most significant bit is the read/write indicator (read=1, write=0), see Table 7-13

B7	B6	B5	B4	B3	B2	B1	B0
R/W	Register address						

Table 7-13 SPI command byte encoding

Write transaction: The next byte on SMOSI will be put into the register with the address specified in the first byte. Writing additional bytes will increment the register address automatically.

Read transaction: The next byte on SMISO will be the contents of the register with address as specified in the first byte. Reading more bytes will increment the register address automatically.

SCSN is active low. Consecutive accesses with SCSN low will auto-increment the address.

7.4.3 2-wire slave interface

This interface is similar to what is found on serial memories and data converter devices. The 7-bit device address of nRF24Z1 is 'a101001', where 'a' is the logic level of the **SADR** input pin (read during power-up and reset only).

Each 2-wire transaction is started with the "Start condition" followed by the first byte containing the 7 bit long device address and one read/write bit. This byte is hereafter referred to as the "address/read command byte" or the "address/write command byte" depending on the state of the read/write bit (read=1, write=0).
The second byte contains the register address, specifying the register to be accessed. This address will be written into the ATX chip, and it is therefore necessary that the first byte after the first start condition is an address/write command. Further actions on the 2-wire interface depend on whether the access is a read or write access. The 2-wire command byte is illustrated in Table 7-14.

B7	B6	B5	B4	B3	B2	B1	B0
a	1	0	1	0	0	1	R/W

Table 7-14 2-wire command byte encoding

7.4.3.1 2-Wire write access.

Figure 7-8 illustrates a simple write operation, where one byte is written to the ATX chip.

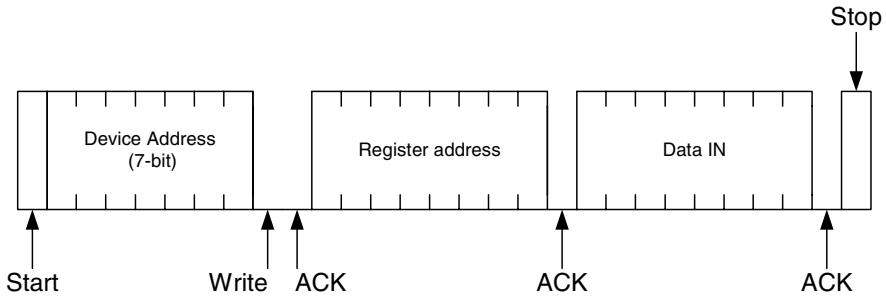


Figure 7-8 2-wire write operation example

A write access is composed by a start condition, an address/write command byte, a register address byte and the corresponding data byte. Each byte will be acknowledged by the 2-wire slave by pulling the data line (SDA) low. To stop the write access, a stop condition is applied on the 2-wire interface. See Figure 7-10 for an example. Consecutive write access is performed by postponing the stop condition.

7.4.3.2 2-Wire read access

Figure 7-9 illustrates a simple read operation, where one byte is read back from the ATX chip.

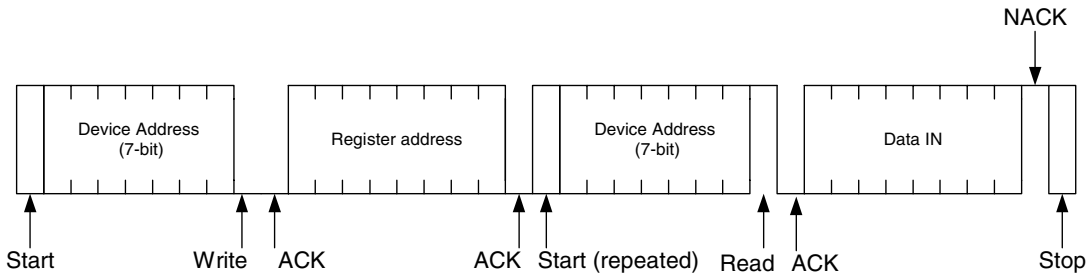


Figure 7-9 2-wire read operation example

A read access is composed by a start condition, an address/write command byte and a register address byte. These two bytes are acknowledged by the 2-wire slave. This scenario is followed by a repeated start condition and an address/read control byte. This byte is also acknowledged by the 2-wire slave. After the acknowledge bit has been sent from the 2-wire slave, the register value corresponding to the register address byte is supplied by the 2-wire slave. This byte must be acknowledged by the 2-wire master if consecutive register read operations are intended. The read access is stopped by not acknowledging the last byte read, followed by a stop condition. See Figure 7-10 for an example.

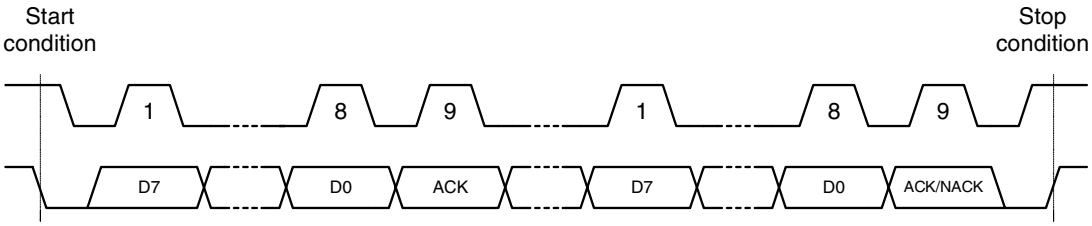


Figure 7-10 2-wire waveform example

7.4.4 General purpose input pins D[2:0]

Three (2 in the case of SPI slave being used, SSEL=0) general purpose inputs are available. The status on these pins can be read in register 0x20.

Address Hex	Register	R/W	Description
0x75	TXDD	R	Value of ATX DD input pins Bit: Interpretation 7:3: Reserved, do not use 2: Value of DD2 (only if SSEL=1) 1: Value of DD1 0: Value of DD0

Table 7-15 ATX DD[2:0] status

If bit TXMOD[3] is set, the levels of pins DD[2:0] are mirrored on ARX pins DO[2:0] directly. See Table 7-6

The IRQ pin can act as an interrupt signal to external application circuitry. There are a number of interrupt sources available, Chapter 9 for details.

7.4.5 ATX Control interface timing

7.4.5.1 2-wire slave timing

The interface supports data transfer rates of 100 kHz, 400 kHz and 1MHz.

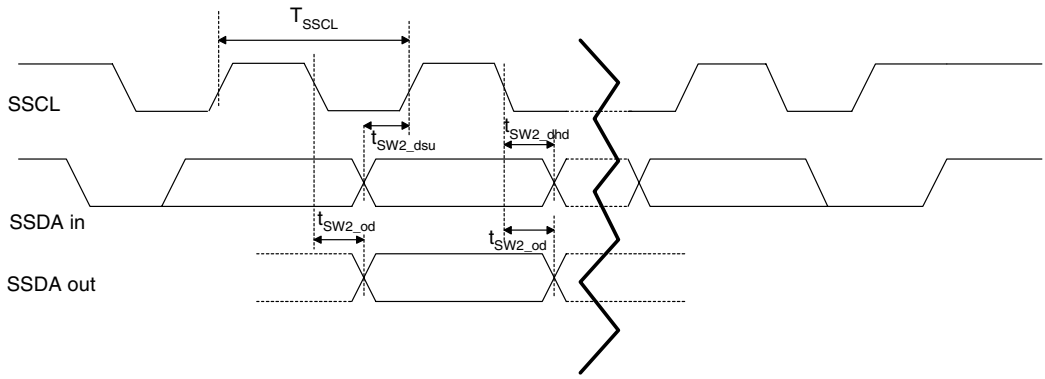


Figure 7-11 2-wire slave timing diagram

Refer to Table 14-1 for values.

7.4.5.2 SPI slave timing

Normal SPI slave clock frequency is up to 8 MHz. However, at 3V (or higher) power supply, the maximum clock frequency may be increased to 16MHz. Note the minimum pause interval t_{SRD} between writing / reading of a byte.

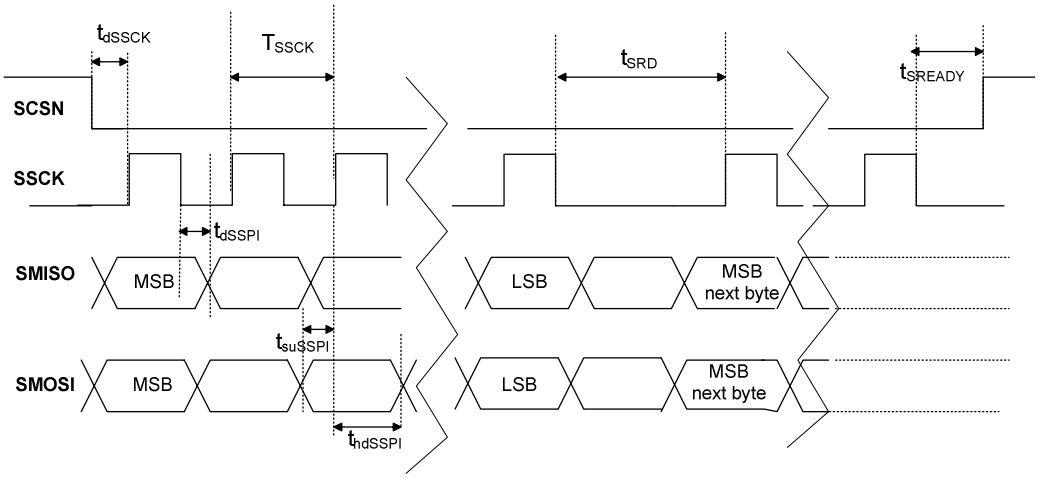


Figure 7-12 SPI slave timing diagram

T_{SSCK} : SSCK cycle time.
t_{dSSCK} : time from SCSN active to first SSCK pulse
t_{dSSPI} : delay from negedge SSCK to new SMISO output data
t_{suSSPI} : SMOSI setup time to posedge SSCK
t_{hdSSPI} : SMOSI hold time to posedge SSCK
t_{SRD} : minimum pause between each byte read from or written to slave SPI
t_{SREADY} : time from SSCK negative edge to SCSN rising edge

Refer to Table 14-1 for values.

7.4.6 ARX control interface options

The ARX is by default configured with a serial slave interface, identical to the ATX serial slave interface. The interface type (SPI or 2-wire) is selected by pin SSEL. The serial slave interface gives local access to all registers in the ARX, but no access to any registers on the ATX side. Only exception is RXPIN[3:0] and RXBUF (indirectly).

Alternatively, if RXSTA[6] is set in the configuration EEPROM, the ARX will be configured with GPIO pins instead of a serial slave interface. The pin-out and functionality of the slave interface or GPIO pins are shown in Table 7-17

Address Hex	Register	R/W	Description
0x06	RXSTA	R	ARX status register. Bit: Interpretation 7: RXEXEC status, 1 is OK, 0 is error 6: 0 : ARX w. serial slave interface 1 : ARX w. GPIO interface, which implies no serial slave interface 5:0: Reserved, do not use

Table 7-16 ARX status register

RXSTA[6] cannot be updated from the ATX, but must be set by the EEPROM or by MCU at ARX side.

	ARX with SPI slave interface (RXSTA[6] = 0, SSEL=0)		**ARX with 2-wire slave interface** (RXSTA[6] = 0, SSEL=1)		**ARX with GPIO interface** (RXSTA[6] =1)	
Pin	**Function**	**Direction**	**Function**	**Direction**	**Function**	**Direction**
1	SSEL	IN	SSEL	IN	DO[2]	OUT
2	SMISO	OUT	SSDA	IN/OUT	DO[1]	OUT
3	SSCK	IN	SSCL	IN/OUT	DO[0]	OUT
4	SCSN	IN	SADR	IN	DI[3]	IN
6	SMOSI	IN	DI[2]	IN	DI[2]	IN
36	IRQ[1]	OUT	IRQ	OUT	DO[3]/PWM[2]	OUT

Table 7-17 ARX serial slave interface / GPIO configuration settings.

Note that the GPIO functions described for registers RXPIO, RXPWME, RXPWMD, RXPIN bits 3:2, RXWAKE bits 3:2, are only available if the ARX is configured with GPIO interface (RXSTA[6]=1). However, these registers may always be read or written to, but if ARX is configured with slave interface, the registers will be disconnected from their corresponding GPIO-pins.

Note that if ARX is configured with a slave interface, multiple ARX registers can be accessed both by the control channel from the ATX, and locally by the MCU via the slave interface. Care should be taken in order to avoid setting conflicting values to a register.

[1] The ATX and ARX have their own local instance of the INTSTA register.
[2] General purpose output (DO[3]) or PWM functionality is set by register RXPWME (0x42)

7.4.7 ARX GPIO pins

General purpose inputs DI[3:0] and outputs DO[3:0] are available in ARX-mode as shown in Table 7-17.

7.4.7.1 INPUTS

DI[3:0] are general purpose inputs while in ARX-mode. Status on these pins is monitored in ATX register RXPIN (0x07). If the ARX is configured with a slave interface, a connected MCU may emulate general purpose inputs by performing a local write to the RXPIN register.

Address Hex	Register	R/W	Description
0x07	RXPIN	R	Current state of audio receiver GPIO inputs Bit: Interpretation 7:4: Reserved, do not use. 3: DI[3] value 2: DI[2] value 1: DI[1] value 0: DI[0] value

Table 7-18 Register RXPIN (0x07)

7.4.7.2 OUTPUTS

Configuration alternatives of general purpose pins DO[3:0] are shown below:

Pins	Functionality	Controlling register	Description
DO[3:0]	General purpose output	RXPIO (0x41)	See below
DO[2:0]	Mirror of DD[2:0]	TXMOD (0x1A)	Ch. 7.4.1
DO[2:0]	ARX SPI master bus enable	RXDCMD (0x70)	Table 7-10, Ch. 7.3
DO[3]	PWM output	RXPWME (0x42) RXPWMD (0x43)	See below

Table 7-19 DO[3:0] configuration alternatives

When used as general purpose outputs, DO[3:0] pin characteristics are controlled by register RXPIO (0x41). On some ARX general purpose output pins, high current drive capabilities can be enabled (e.g. LED output driver). The register contents of RXPIO is listed in Table 7-20.

.

Address Hex	Register	R/W	Description
0x41	RXPIO	R/W	Receiver GPIO output and drive strength Bit | Logic 1 Interpretation 7 | High drive high enable for DO[3] 6 | Reserved, MBZ [1] 5 | High drive high enable for DO[1] 4 | Reserved, MBZ [2] 3 | Data for DO[3] 2 | Data for DO[2] 1 | Data for DO[1] 0 | Data for DO[0] NOTES: 1: nRF24Z1 Version B : High drive low enable for DO[2] 2: nRF24Z1 Version B : High drive low enable for DO[0] High drive sink current (IOL_HD) for DO[0] and DO[2] @ VOL= 0.4V is typ. 10mA (only valid for nRF24Z1 Ver. B)

Table 7-20 Register 0x41 RXPIO

Values in RXPIO are sent to the ARX when (0x01) is written to RXCSTATE.

Note that RXPIO values do not become effective until link is established. Example : initial values set in configuration EEPROM will not show on DO-outputs until link is established.

Pin DO[3] can also be used as a PWM output. PWM-enable and PWM-frequency is controlled by register RXPWME (0x42). PWM- duty cycle is controlled by register RXPWMD (0x43) as shown in Table 7-21.

Address Hex	Register	R/W	Description
0x42	RXPWME	R/W	Enables audio receiver PWM on pin DO[3] and sets PWM frequency Bit | Interpretation 7:6 | 00 : PWM not enabled 11 : Enable PWM on DO[3] 01,10 : reserved, do not use 5:0 | PWM frequency (repetition rate) fPWM=16MHz/(255·(1+RXPWME[5:0]))
0x43	RXPWMD	R/W	Set audio receiver PWM duty cycle

Table 7-21 Registers RXPWME (0x42) and RXPWMD (0x43)

Values in RXPWME and RXPWMD are sent to the ARX when (0x01) is written to RXCSTATE.

7.5 Data Channel Timing

7.5.1 Forward data channel; data transfer from ATX to ARX

Data communication from ATX to ARX is performed through a dedicated data channel which is superimposed on the audio stream. Maximum data rate on this channel can be calculated by using Formula 1 and Formula 2.

$$BRR = AFR/(8 \cdot 16) \quad \text{frame/sec} \quad (1)$$

$$DR = BRR \cdot NPB \cdot NBP \cdot 8\text{bits} \quad \text{bits/sec} \quad (2)$$

BRR: Frame Repetition Rate, time interval between data frame starting points.
AFR: Audio Fundamental Rate (sampling frequency).
DR: Average Data Rate on data channel.
NPB: Number of Packets per Frame.
NBP: Number of data Bytes per Packet.

nRF24Z1 has the following parameters alternatives for the ATX to ARX data channel:
AFR: 48 kSPS, 44.1 kSPS or 32 kSPS
NPB: 4
NBP: 1

Table 7-22 lists the resulting data rates.

Fundamental rate of audio signal	Maximum data rate on data channel
48kSPS	12000 bits/sec
44.1kSPS	11025 bits/sec
32 kSPS	8000 bits/sec

Table 7-22 Forward data channel bandwidth

7.5.1.1 Limitations in forward data channel, effective data rate.

The data channel bandwidth listed in Table 7-22 is shared by the different inputs. Data from all interfaces are fed into a FIFO queue for transmission via the forward data channel.

Note that high activity on one source will increase the link delay for other sources sharing the same forward data channel.
The resulting effective data rate on the forward data channel depends mainly on link quality. A poor link will result in reduced data rate compared to ideal- or low noise conditions.

7.5.2 Return data channel; data transfer from ARX to ATX

Data communication from ARX to ATX is performed through a dedicated data channel which is integrated in the acknowledge data stream. Maximum data rate on this data channel can be calculated with Formula 1 and Formula 2 with NPB = 1 and NBP = 5 (see Table 7-23).

Fundamental rate of audio signal	Maximum data rate on return data channel
48kSPS	15000 bits/sec
44.1kSPS	13781 bits/sec
32 kSPS	10000 bits/sec

Table 7-23 Return data channel rate

7.5.2.1 Limitations in return data channel

Data transfer from ARX to ATX can be divided into three categories:

1. Link error monitoring.
2. Parallel port monitoring.
3. ARX master interface communication.

These three data transfer categories share the bandwidth of the return channel listed in Table 7-23.

7.5.2.2 Link error monitoring

The refresh rate of the link error register, LNKERR, depends on the data rate shown in Table 7-24.

Fundamental rate of audio signal	LNKERR data rate on return data channel
48kSPS	3000 bits/sec
44.1kSPS	2756 bits/sec
32 kSPS	2000 bits/sec

Table 7-24 LNKERR data rate

7.5.2.3 Parallel port monitoring

The parallel port is updated according to the data rate shown in Table 7-25.

Fundamental rate of audio signal	Parallel port data rate on return data channel
48kSPS	1500 bits/sec
44.1kSPS	1378 bits/sec
32 kSPS	1000 bits/sec

Table 7-25 Parallel port data rate

7.5.2.4 Master interface communication

The effective data rate of the ARX to ATX master interface is listed in Table 7-26.

Fundamental rate of audio signal	Master interface data rate on return data channel
48kSPS	3000 bits/sec
44.1kSPS	2756 bits/sec
32 kSPS	2000 bits/sec

Table 7-26 Serial master interface data rate

8 Quality of Service (QoS) and RF-protocol

The purpose of the QoS-engine is to maintain satisfactory audio quality over time during normal operation.

This involves:

- Ensuring that corrupt or lost information sent from the ATX is automatically detected and retransmitted to the ARX
- Monitoring and avoiding channels used by other 2.4GHz equipment or which have poor radio propagation properties (e.g. fading effects)
- Reducing the audible effect of corrupt data when retransmission fails within the latency timeframe
- Establish a new link in the case of communication break down

The control channel is used for monitoring radio link status information.

It should be noted that at some point, the QoS-engine is unable to maintain a flawless audio link. This may be the result of stretched range, excessive interferer noise or both.

The RF-protocol is an integral part of the QoS-engine and is therefore not subject for user modification.

8.1 Link establishment

The link establishment procedure is fully managed on-chip.

8.2 RF protocol

The RF-protocol is controlled on-chip. The only parameter configurable by the application is the address. This enables separate nRF24Z1 devices to be identified and accessed independently in the same physical area. The RF protocol address length is 5 bytes and the address bytes are set in registers ADDR[0:4], listed in Table 8-1.

Address Hex	Register	R/W	Description
0x39	ADDR[0]	R/W	Address byte #0 (LSB)
0x3A	ADDR[1]	R/W	Address byte #1
0x3B	ADDR[2]	R/W	Address byte #2
0x3C	ADDR[3]	R/W	Address byte #3
0x3D	ADDR[4]	R/W	Address byte #4

Table 8-1 RF protocol address

The contents of ADDR[0-4] is sent to the ARX when (0x01) is written to LINKCSTATE.

8.3 Adaptive Frequency Hopping (AFH)

Adaptive Frequency Hopping is an integral part of the QoS-engine functionality. The audio data is split in segments which are transmitted at different frequencies known by the transmitter and receiver. The frequencies used by the ATX/ARX are changing over time as active noise sources in the frequency band appear and disappear.
AFH also enables the nRF24Z1 link to handle challenges such as signal cancellation due to multi-path fading effects.

The frequencies used by the AFH-algorithm are specified in 38 frequency position registers shown in Table 8-2. The hopping sequence follows the register positions in consecutive order (i.e. CH0, CH1, CH02.... CH36, CH37, CH0, CH1 etc.). The contents of CH0-37 may not be sent from the ATX to the ARX. Register values of CH0-37 must be configured locally by EEPROM or MCU.

Address Hex	Register	R/W	Description
0x0C	CH0	R/W	Frequency positions for the hopping sequence. The frequency position frequency is equal to the position number multiplied by 1 MHz relative to 2400MHz. Example: To define a frequency hopping scheme starting at f=2420MHz, and then hopping to f=2440MHz , the following values must be set : CH0=0x14, CH1=0x28...
0x0D	CH1	R/W	
0x0E	CH2	R/W	
0x0F	CH3	R/W	
0x10	CH4	R/W	
0x11	CH5	R/W	
0x12	CH6	R/W	
0x13	CH7	R/W	
0x14	CH8	R/W	
0x15	CH9	R/W	
0x16	CH10	R/W	
0x17	CH11	R/W	
0x18	CH12	R/W	
0x19	CH13	R/W	
0x1A	CH14	R/W	
0x1B	CH15	R/W	
0x1C	CH16	R/W	
0x1D	CH17	R/W	
0x1E	CH18	R/W	
0x1F	CH19	R/W	
0x20	CH20	R/W	
0x21	CH21	R/W	
0x22	CH22	R/W	
0x23	CH23	R/W	
0x24	CH24	R/W	
0x25	CH25	R/W	
0x26	CH26	R/W	
0x27	CH27	R/W	
0x28	CH28	R/W	
0x29	CH29	R/W	
0x2A	CH30	R/W	
0x2B	CH31	R/W	
0x2C	CH32	R/W	
0x2D	CH33	R/W	
0x2E	CH34	R/W	
0x2F	CH35	R/W	
0x30	CH36	R/W	
0x31	CH37	R/W	

Table 8-2 Frequency hopping table registers.

8.3.1 Adapting to the RF environment

In an environment without other 2.4GHz applications or noise sources, the nRF24Z1 will use all the frequency positions listed in Table 8-2. In the presence of an active RF system, occasional packet collisions are likely, resulting in RF packets being lost.

When an operating frequency resulting in unacceptable packet loss is detected, the ATX may remove it from the list of frequency positions used by AFH algorithm. The corresponding list in the ARX is synchronized by use of the control channel.

Frequency positions removed from the frequency hopping sequence are added to a FIFO list of frequencies *temporarily banned* for use by the AFH-algorithm.
The length of the list of banned frequencies are configurable (see Table 8-3). The maximum number of banned channels is 18. A banned channel will remain in the list of banned frequencies until it will be pushed out by a new candidate.

The frequency bandwidth occupied by a nRF24Z1 device is approx. 4MHz, whereas the frequency resolution of the available frequencies (frequency positions) is 1MHz. Thus, the frequency position spacing in Table 8-2 must be at least 4 in order to achieve non-overlapping channels.

Note that the list of hopping positions does not need to contain solely non-overlapping channels in order to achieve optimal effect. Generally, the frequency positions should be distributed over the available frequency band.

Address Hex	Register	R/W	Description
0x33	NBCH	R/W	Number of Banned CHannels. The number of frequency positions subject to ban at any time. Maximum register value is 18.
0x34	NACH	R/W	The number of frequency positions used in normal audio streaming mode. The frequency locations used are the first NACH-locations of Table 8-2.
0x35	NLCH	R/W	Number of frequency positions used in link mode. This is the number of frequency positions used in linking mode. The frequency locations used are the first NLCH-locations of Table 8-2.

Table 8-3 Frequency hopping configuration registers.

Values in NBCH, NACK, and NLCH are transmitted to the ARX when 0x01 is written to RXCSTATE

To minimise linking time, the same basic frequency hopping scheme must be set on the ATX and ARX side.

8.4 Link registers

The nRF24Z1 has a number of link registers whose primary function is to monitor the overall quality on the link and enable actions to be taken based on it. The link monitoring registers are listed in Table 8-4.

<table>
<tr><th>Address Hex</th><th>Register</th><th>R/W</th><th>Description</th></tr>
<tr><td>0x04</td><td>LNKQ</td><td>R</td><td>LiNK Quality register. A measure of the number of packets lost in the last 14 frame window (of a consecutive series of 14 frame windows).
Calculations :
- Number of packets lost in the 14 frame window is 255-LNKQ.
- LNKQ=255 means no packets lost
- Total number of packets in the 14 frame window is (14*NPPF)+(255-LNKQ) where NPPF is Number of Packets Per Frame which varies with audio rate as shown below :
<table><tr><td>Audio sampling rate</td><td>48-32kHz</td><td>24-16kHz</td><td>12-8kHz</td></tr><tr><td>NPPF</td><td>8</td><td>4</td><td>2</td></tr></table></td></tr>
<tr><td>0x05</td><td>LNKERR</td><td>R</td><td>LiNK ERRor register. Returns the number of packets permanently lost[1] in the last 32 frame window (of a consecutive series of 32 frame windows).
0 = no packets lost
255 = all packets lost</td></tr>
<tr><td>0x37</td><td>LNKWTH</td><td>R/W</td><td>LiNK Warning THreshold limit. A LNKQ value ≤ LNKWTH will cause an IRQ to be activated (if enabled by INTCF[5])</td></tr>
<tr><td>0x38</td><td>LNKETH</td><td>R/W</td><td>LiNK Error THreshold limit. A LNKERR value ≥ LNKETH will cause an IRQ to be activated (if enabled by INTCF[2])</td></tr>
</table>

Table 8-4 Link quality monitoring registers

LNKQ and LNKERR are status registers directly available in the ATX. Note that only LNKERR is available in the ARX.

The register value of LNKQ indicates the current level of strain on the QoS-engine. The LNKERR register reports the number of unrecoverable packets in the last 14 frame window. LNKWTH and LNKETH registers enable system interrupts if one of the quality indicators drops below an acceptable level.

The link functional status is reported in register LNKSTA.

Actions to be taken upon the quality requirements set in LNKWTH and LNKETH, can be set in register LNKMOD. Registers LNKSTA and LNKMOD are listed in Table 8-5.

[1] A packet is permanently lost if it is not successfully received at the time it is required for audio output, i.e. it can not be retransmitted any longer.

<table>
<tr><th>Address Hex</th><th>Register</th><th>R/W</th><th>Description</th></tr>
<tr><td>0x03</td><td>LNKSTA</td><td>R/W</td><td>Link status register
Bit | Interpretation
7:1 | Reserved, do not use
0 | Link established</td></tr>
<tr><td>0x36</td><td>LNKMOD</td><td>R/W</td><td>Link mode register.
Bit | Interpretation
7 | Reserved, MBZ
6 | ATX and ARX reset to initial EEPROM register contents if no counterpart is found on the next link initialization.
5 | Reserved, MBZ
4 | Force reconfiguration with new configuration data
3 | Mute when LNKERR > LNKETH
2 | Disable adaptive frequency hopping
1:0 | Reserved, MBZ</td></tr>
</table>

Table 8-5 Link status/mode registers

8.4.1 RF link latency

Link robustness may be traded with link latency. In systems where latency is not critical (i.e. CD player headsets), the high latency option should be used. Latency is set in the TXLAT register as shown below. Note that the resulting latency (e.g. audio delay) also depends on the audio sampling rate f_s.

<table>
<tr><th>Address Hex</th><th>Register</th><th>R/W</th><th>Description</th></tr>
<tr><td>0x52</td><td>TXLAT</td><td>R/W</td><td>ATX to ARX Latency
<table>
<tr><th>Value</th><th>Interpretation</th><th>f_s = 48kSPS</th><th>f_s= 44.1kSPS</th><th>f_s= 32kSPS</th></tr>
<tr><td>0</td><td>Short</td><td>6 ms</td><td>6.6 ms</td><td>9 ms</td></tr>
<tr><td>2</td><td>Nominal</td><td>11.4ms</td><td>12.4 ms</td><td>17 ms</td></tr>
<tr><td>4</td><td>High</td><td>16.7 ms</td><td>18.2 ms</td><td>25.1ms</td></tr>
</table>
Note: Latency values listed are without ADC/DAC delay (digital in/out)</td></tr>
</table>

Table 8-6 TXLAT register

8.5 RF output power

The only configurable parameter in the RF subsystem is the RF transmitter output power. ATX output power is set in register TXPWR. ARX output power is set in register RXPWR.

Address Hex	Register	R/W	Description
0x56	TXPWR	R/W	ATX output power Value: Interpretation 0: -20 dBm 1: -10 dBm 2: -5 dBm 3: 0 dBm
0x49	RXPWR	R/W	ARX output power Value: Interpretation 0: -20 dBm 1: -10 dBm 2: -5 dBm 3: 0 dBm

Table 8-7 TXPWR and RXPWR registers

Both output power registers are accessible from the ATX. The output power on the ATX/ARX may thus be set based on the result of the RF link quality registers described in Table 8-4. Reducing the output power will result in extended battery lifetime and reduced strain on other coexisting RF systems.

9 Interrupts

An nRF24Z1 with serial slave interface can be configured to deliver interrupts to any external system connected to pin IRQ. Interrupt sources are defined by register INTCF (0x13). Interrupt status flags are available in register INTSTA (0x02). After interrupt initiation, the IRQ will stay active ("0" with INTCF[7]=0, "1" with INTCF[7]="1") until a "1" is written to the corresponding interrupt flag in the INTSTA register. All interrupt flags may be cleared by writing 0x7F to INTSTA.

<table>
<tr><th>Address Hex</th><th>Register</th><th>R/W</th><th>Description</th></tr>
<tr><td>0x02</td><td>INTSTA</td><td>R/W</td><td>Interrupt status register. Register contents and interrupt are cleared upon reading.
<table><tr><th>Bit</th><th>Interpretation</th></tr><tr><td>7</td><td>Reserved, do not use</td></tr><tr><td>6</td><td>link broken status flag</td></tr><tr><td>5</td><td>poor link quality status flag (LNKQ<=LNKWTH)</td></tr><tr><td>4</td><td>remote transfer done status flag , set upon completion of a RXEXEC, TXCSTATE, LNKCSTATE or RXCSTATE command.</td></tr><tr><td>3</td><td>ATX : remote input (RXPIN) changed status flag
ARX with slave interface : RXPIO[3:0] register value changed status flag</td></tr><tr><td>2</td><td>Link error flag (LNKERR >= LNKETH)</td></tr><tr><td>1</td><td>Wakeup from power down status flag (see Ch.11.2.4)</td></tr><tr><td>0</td><td>Reserved, do not use</td></tr></table>See register INTCF for interrupt enabling</td></tr>
<tr><td>0x53</td><td>INTCF</td><td>R/W</td><td>Interrupt configuration. Select events that can generate interrupt on the IRQ pin.
<table><tr><th>Bit</th><th>Interpretation</th></tr><tr><td>7</td><td>Interrupt polarity, 1 is active high, 0 is active low</td></tr><tr><td>6</td><td>Enable link broken interrupt</td></tr><tr><td>5</td><td>Enable poor link quality interrupt</td></tr><tr><td>4</td><td>Enable remote transfer done interrupt</td></tr><tr><td>3</td><td>Enable GPIO changed interrupt [1]</td></tr><tr><td>2</td><td>Enable link error interrupt</td></tr><tr><td>1</td><td>Enable wakeup from power down interrupt</td></tr><tr><td>0</td><td>Reserved, MBZ</td></tr></table></td></tr>
</table>

Table 9-1 Registers INTCF and INTSTA

[1] ATX: interrupt generated by change of logic level on ARX DI[3:0]-pin(s)
ARX: interrupt generated by change of logic level on ARX DO[3:0]-pin(s)

An interrupt pin is always available in ATX mode. While in ARX mode, an interrupt pin is only available when the device is configured with a serial slave interface. In this case the interrupt registers are local to ATX and ARX respectively (i.e. an interrupt on the ARX will only trigger the ARX, likewise an interrupt on the ATX will only trigger the ATX).
If the nRF24Z1 is configured to give interrupt on “Wakeup from power down”, no other detected interrupts will trigger the IRQ pin. With this configuration, the IRQ pin will constantly be set active in power up and inactive in power down. This feature can be utilized by an external MCU to monitor the power down state of the nRF24Z1.
“Poor link quality interrupt” and “Remote transfer done interrupt” are only available to the ATX.

INTSTA- and INTCF register content is set locally in the ATX and the ARX devices. All interrupts must be cleared after power-on-reset.

10 RESET outputs

Designated pins not used for other functionality can provide reset pulses to external peripherals.
External RESET is required when the nRF24Z1 device is operated standalone and no autonomous devices (i.e. MCU) are available to provide RESET to peripherals such as an ADC or DAC.
External RESET is executed as a part of the configuration routine performed immediately after power-on-reset and after device reconfiguration.

The I/O pin of choice and its signal polarity is dictated by register TXRESO (0x10) for the ATX and register RXRESO (0x40) for ARX peripherals.

Address Hex	Register	R/W	Description
0x50	TXRESO	R/W	Enabling of optional RESET pulse output from ATX. Bit: Interpretation 7:3: Reserved, MBZ 2:1: 0 : no RESET output 1 : RESET output on MSDA pin 2 : RESET output on MOSI pin 3 : RESET output on SPDIO pin 0: ATX RESET output polarity 0 : active low 1 : active high Reset pulse duration is approx. 285us
0x40	RXRESO	R/W	Enabling of optional RESET pulse output from ARX. Bit: Interpretation 7:3: Reserved, MBZ 2:1: 0 : no RESET output 1 : RESET output on MSDA pin 2 : RESET output on MOSI pin 3 : RESET output on SPDIO pin 0: ARX RESET output polarity 0 : active low 1 : active high Reset pulse duration is approx. 285us

Table 10-1 TXRESO and RXRESO registers

Values in the TXRESO and RXRESO registers should be stored in a configuration EEPROM.

11 Power down control

11.1 Activation of power down mode

Two power down mode initiation alternatives exist; initiation by an external MCU or induced by detection of communication link breakdown/loss.

Normally, ATX/ARX power down is initiated by an external MCU connected to the ATX. The ARX power down mode is initiated first (register RXMOD[7]=1) followed by the ATX (register TXMOD[6]=1). Register TXMOD is described in Table 7-6 and register RXMOD is described in Table 7-8.

Note that *the nRF24Z1s will not enter power down mode unless a wake time is specified*. In order to enable ARX power down mode, the RXWTI register must contain a value > 0x00. Similarly, the ATX TXWTI register value must be > 0x00. Refer to Chapter 11.2.2 for timer control register description.
The ARX will enter power down as soon as the appropriate register settings have been successfully transferred. The transfer is initiated by writing 0x01 to register RXCSTATE.

11.1.1 Automatic power down

An automatic power down mechanism will be activated as soon as the nRF24Z1 looses its radio link. This mechanism will cause the nRF24Z1 to enter power down automatically if no new link is established after a specific timeout interval. This feature is enabled in the ATX by writing a value ≠ 0x00 into TXWTI and in the ARX by writing a value ≠ 0x00 into RXWTI. The time that the devices will spend looking for a link before going to automatic power down is specified by (TXSTI1 · 256 + TXSTI0) · 10ms in the ATX and (RXSTI1 · 256 + RXSTI0) · 10ms in the ARX.

11.2 Wake up from power down

Two events may trigger a wake up from power down mode; status change on external pin (wake-on-interrupt) and timer controlled wake up (wake-on-timer).
To deactivate power down mode, an external MCU is required to reset the power down bits in the ATX and ARX.

11.2.1 Wake-on-interrupt

An nRF24Z1 device can be put in power down mode until the level on an external pin is changed. A change of logic level will initiate wake up and new link initialisation.

In ATX mode, the DD[1] pin may be used to enable a wake up. This feature is enabled in register TXMOD[5].

In ARX mode, wake up can be initiated by a level change on any of the input pins DI[3:0]. Wake up enable is controlled by register RXWAKE, described in Table 11-1. Register TXMOD is described in Table 7-6.
Wake-on-timer has priority in this register. RXWAKE[4] must thus be cleared in order to enable external pin change wakeup. Any combination of the RXWAKE[0:3] bits can be set.

Upon wake up, the nRF24Z1 device will attempt to re-link during the specified wake time. *If the power down bit is not reset during this interval the device will return to power down mode*. Power down timing is described in Chapter 11.2.2 and 11.3 (example). For external pin wakeup, the resulting wakeup time is TXWTI·(TXLTI+1)·10 ms for ATX and RXWTI·(RXLTI+1)·10 ms for ARX respectively.

The shortest pulse width (on an input pin) for wakeup is 1 ms.

<table>
<tr><th>Address Hex</th><th>Register</th><th>R/W</th><th>Description</th></tr>
<tr><td>0x45</td><td>RXWAKE</td><td>R/W</td><td>Wakeup sources for audio receiver
<table>
<tr><th>Bit</th><th>Interpretation</th></tr>
<tr><td>7:6</td><td>Reserved, MBZ</td></tr>
<tr><td>5</td><td>Reserved</td></tr>
<tr><td>4</td><td>Wakeup on sleep timer</td></tr>
<tr><td>3</td><td>Wakeup on DI[3] change</td></tr>
<tr><td>2</td><td>Wakeup on DI[2] change</td></tr>
<tr><td>1</td><td>Wakeup on DI[1] change</td></tr>
<tr><td>0</td><td>Wakeup on DI[0] change</td></tr>
</table></td></tr>
</table>

Table 11-1 External wake-up control registers

11.2.2 Wake-on-timer

The nRF24Z1 can also be operated in a power saving mode where timers controls a cyclic power down / wake up sequence. In this mode the nRF24Z1 will be able to re-initialise the RF link without any user interaction. If no matching nRF24Z1 devices are located within the specified time interval after wake-up, power down mode is resumed.

The internal timer that puts the device into the power down part of the cycle has priority over link re-initialisation attempts. In order to re-initialise the link, the power down bits in TXMOD and RXMOD must be cleared during the wake up part of the cycle, and the ATX and ARX must both be in the wake up part of the cycle at the same time. Power down is resumed if RXMOD and TXMOD power down bits remain set, or if ATX and ARX are not in the wake up part of the cycle at the same time.

In power down mode, the ATX and ARX timing is no longer synchronised. A separate set of timers are hence implemented in the ATX and ARX.

The wake-on-timer sequence is controlled by a 16 bit sleep interval timer (ATX: TXSTI, ARX: RXSTI) and an 8 bit wake up interval timer (ATX: TXWTI, ARX: RXWTI). The contents of the sleep timer control registers decide the number of consecutive 10ms intervals the nRF24Z1 device will sleep before waking up. The wake up interval timers correspondingly sets the number of consecutive 10ms intervals in which the nRF24Z1 should attempt to re-link before returning to power down mode.

If the two paired nRF24Z1 devices are active at the same time, and the power down bits in TXMOD and RXMOD are cleared, a link is re-established. The controlling device (e.g. MCU) on the ATX side should then reset TXWTI and RXWTI in order to prevent return to power down mode caused by the automatic power down mechanism. With a controlling MCU on the ATX side, it is important to put the ARX to sleep before the ATX, and to wake up the ATX before waking up the ARX.

The sleep and wake up timers are controlled by the registers described in Table 11-2.

Address Hex	Register	R/W	Description
0x57	TXSTI[0]	R/W	ATX sleep timer byte #0 TXSTI is a 16-bit number specifying the number of consecutive 10ms periods in which the ATX is to sleep between attempts to establish a new link.
0x58	TXSTI[1]	R/W	ATX sleep timer byte #1
0x59	TXWTI	R/W	ATX wake up timer. With TXWTI set to 0, the ATX will not return to power down mode. A setting > 0 will specify the number of consecutive 10ms periods in which the ATX is trying to establish a link before re-entering power down mode.
0x4D	TXLTI	R/W	ATX wake up time extension register, used to extend ATX wake up time when woken by a pin status change or while in link mode. Total wake up time is then (TXLTI+1)·TXWTI·10ms
0x46	RXSTI[0]	R/W	ARX sleep timer byte #0 RXSTI is a 16-bit number specifying the number of consecutive 10ms periods in which the ARX is to sleep between attempts to establish a new link. Only used if the sleep timer is enabled, see bit 4 of RWAKE register.
0x47	RXSTI[1]	R/W	ARX sleep timer byte #1
0x48	RXWTI	R/W	ARX wake up timer. With RXWTI set to 0, the ATX will not return to power down mode. A setting > 0 will specify the number of consecutive 10ms periods in which the ARX is trying to establish a link before re-entering power down mode.
0x4C	RXLTI	R/W	ARX wake up time extension register, used to extend ARX wake time when woken by a pin change or while in link mode. Total wake time is then (RXLTI+1)·RXWTI·10ms

Table 11-2 Sleep and wake up timer registers

11.2.3 Wakeup from automatic power down

When automatic power down is enabled, and after having lost its link for the specified time, the devices will enter the sleep modes set by TXMOD, RXMOD and RXWAKE. This means that a device set to Wake-on-Interrupt has to be interrupted (i.e. button pushed) before it may start trying to re-establish a link after automatic power down. However, if both ATX and ARX are set to Wake-on-timer, they are able to wakeup from automatic power down without user intervention.

11.2.4 Interrupting an MCU while waking up

The nRF24Z1 has several ways of interrupting an external MCU or other external devices. The wakeup from power down interrupt (INTSTA[1]) is the only interrupt whose interrupt flag does not have to be cleared in register INTSTA. Enabling the wakeup from power down interrupt on the ATX makes the IRQ output pin track the sleep modes of the nRF24Z1. An active low IRQ pin will be low when the ATX is streaming audio or trying to establish a link. It will be high when the ATX is idle between attempts at establishing a link.

This means that if the ATX is Wake-on-Timer, the external MCU does not have to be in charge of system timing while in sleep mode. Instead it is interrupted by the nRF24Z1 whenever it wakes up and becomes ready to receive commands.

11.3 nRF24Z1 power saving example

A combination of the two power down control alternatives is possible.
Figure 11-1 shows an example of ATX timer controlled power down combined with power down with wake up on external pin event in the ARX. In this example the ARX is shut down completely until a user activates the ARX (i.e. headphone or speaker).

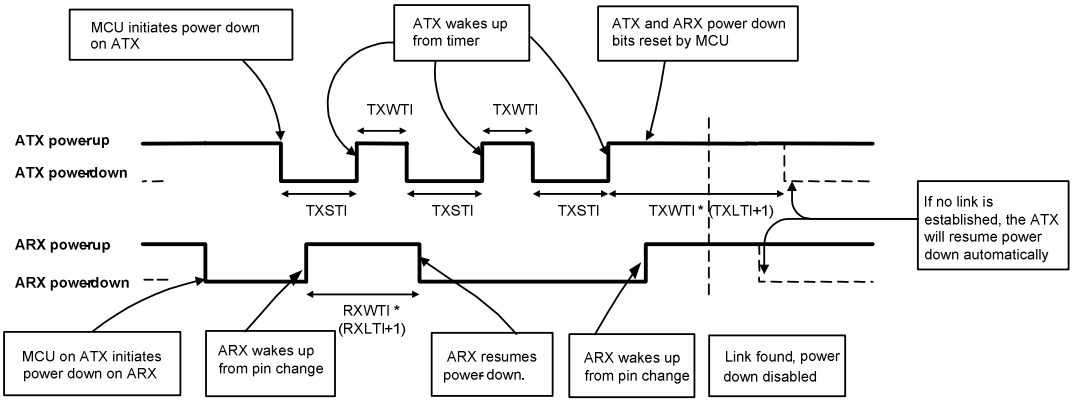


Figure 11-1 nRF24Z1 power saving example

In this example, the ARX will wake up upon a logic level shift on one of the DI[3:0] GPIO pins. The ARX will then be active for the designated time interval, attempting to establish link with the ATX. The ARX will return to power down if the register bit RXMOD[7] is not cleared.

The ATX will wake up from power down on a cyclic basis. In order to (cancel cyclic behaviours) the ATX, the register bit TXMOD[6] must be cleared within the ATX wake time.

If the ARX wakes up and a link is established, the ARX and ATX will remain awake upon ATX clearing of the ARX power down bit.

ATX will resume power down if no link is found after the extended wake time interval is over; even when the power down bit was cleared.

12 Register update over the control channel

The registers TXCSTATE, LNKCSTATE, RXCSTATE can be used by an ATX MCU to update audio receiver control registers via the control channel. Writing to these registers from an ARX MCU is illegal. When the ATX MCU is to initiate a register contents change in one or more of the ARX registers, the register value(s) are first buffered in the ATX. The registers contents are then transferred to the ARX and employed there when the corresponding *update register* is written to by the ATX MCU. Prior to any transfer to the ARX, the transfer register should be polled to check if the ATX is ready to transfer new register values to the ARX.
Setting an update register to 0x01, triggers the ATX to send the corresponding register values to the ARX. The update register is then automatically reset to 0x00 after the register values have been successfully transferred. When an update register reads 0x01, the ATX is busy sending the register values to the ARX. When an update register reads 0x02, the last transfer was unsuccessful. A value of 0x02 may indicate a radio link problem.

Address Hex	Register	R/W	Description
0x5B	TXCSTATE	R/W	Controls when to send ATX registers TXFMT, TXLAT, I2SCNF_IN over the data link to the ARX. Status values are : 0 : idle, last transfer successful 1 : busy, registers may not be accessed. 2 : idle, last transfer unsuccessful When idle, data may be written to the ATX registers. Setting TXCSTATE=1 triggers the ATX to send register values to the ARX. TXCSTATE is automatically reset to 0 by the ATX upon successful transfer to the ARX. An external MCU should poll this register before accessing the ATX registers.
0x3E	LNKCSTATE	R/W	Controls when to send ATX side link control registers over the data link to the ARX. Status values are : 0 : idle, last transfer was successful 1 : busy, registers may not be accessed. 2 : idle, last transfer was unsuccessful When idle, data may be written to the link control registers. Setting LNKCSTATE=1 triggers the ATX to send link control register values to the ARX. LNKCSTATE will be reset to 0 by the ATX upon successful transfer to the ARX. An external MCU should poll this register before accessing any link control registers.
0x4B	RXCSTATE	R/W	Controls when to send ARX control register data from the ATX over the data link to the ARX. Status values are[1] : 0 : idle, and last transfer was successful 1 : busy, the registers may not be accessed. 2 : idle, but last transfer was unsuccessful When idle, data may be written to the ARX control registers. Setting RXCSTATE=1 triggers the ATX to send ARX control register values to the ARX. RXCSTATE will be reset to 0 by the ATX upon successful transfer to the ARX. An external MCU should poll this register before accessing any of the ARX control registers.

Table 12-1 Register update registers

[1] Status applies to all ARX control registers except RXMOD

12.1 Register update and device relink

Some register updates require ARX and ATX reconfiguration.
The ATX and ARX will always be reconfigured after a link has been established. The ATX and ARX may thus be reconfigured by forcing a re-link. This can be done by setting the "Force reconfiguration" bit; LNKMOD[4] = 1.

Register category	Register name
ATX registers	TXSTA[6:3] TXFMT TXMOD[2:0] I2SCNF_IN TXLAT
ARX registers	RXMOD[2] I2SCNF_OUT[5:0]
LINK registers	ADDR0, ADDR1, ADDR2, ADDR3, ADDR4 NBCH NACH
TEST_MODE registers	TESTREG TESTCH

Table 12-2 Registers requiring device re-configuration

Some related registers and bits which have special functionality are listed below:

Register name	Register function
RXSTA[6]	The ARX serial slave interface may only be disabled by setting RXSTA[6] from an external configuration EEPROM. A serial slave interface will be enabled by default if no EEPROM is present on the ARX.
CH0-37	The frequency hopping table registers is not transferred from the ATX to ARX. These registers must therefore be configured in EEPROM or local MCU.
TXSTA	Sampling rates are automatically transmitted to the ARX from the ATX during link-locate mode.
RXMOD	ARX operation mode is automatically transmitted to the ARX from ATX during link-locate mode.
RXPIN	Information about ARX general-purpose input pins is automatically transmitted from the ARX to the ATX during link-locate mode. This information is also being continuously transferred from the ARX to the ATX during normal audio streaming mode.
TXCSTATE	Transfer register used by the ATX to send data to ARX.
RXCSTATE	Transfer register used by the ATX to send data to ARX.
LNKCSTATE	Transfer register used by the ATX to send data to ARX.
RXEXEC	Transfer register used by the ATX to send and receive data to/from the SPI and 2-wire master interfaces of the ARX.

Table 12-3 Registers with special functionality

13 Test mode

nRF24Z1 test mode is initiated by writing to test registers TESTREG and TESTCH, followed by setting bit 4 of the LNKMOD register. This will force the device to restart in test mode according to the TESTREG and TESTCH register settings.
nRF24Z1 will remain in test mode until reset. Test mode can only be aborted by use of reset. Test mode changes can only be performed upon device reset. This applies for both the ATX and ARX.

The ATX test registers can be accessed via the (SPI or 2-wire) slave interface (also valid for an ARX configured with slave interface; RXSTA[6]=0).

For an ARX configured from an external EEPROM with GPIO interface (EEPROM/RXSTA[6]=1), the slave interface does not exist, blocking access to the test registers. EEPROM configuration may be avoided by forcing the EEPROM data output line low, aborting the read process from the EEPROM. As a result, RXSTA[6] will not be set, and the ARX is configured with a slave interface.

<table>
<tr><th>Address Hex</th><th>Register</th><th>R/W</th><th colspan="2">Description</th></tr>
<tr><td>0x7E</td><td>TESTREG</td><td>W</td><td colspan="2">Test mode register:
Code 1: 0110 0011 – Single channel test.
Code 2: 0111 0011 – Channel sweep test. Sweeps all channels from frequencies from 2400 MHz to 2480 MHz in steps of 1MHz.</td></tr>
<tr><td>0x7F</td><td>TESTCH</td><td>W</td><td>Bit</td><td>Interpretation</td></tr>
<tr><td></td><td></td><td></td><td>7</td><td>1: TX, 0: RX
Initiates the mode described in TESTREG in RX / TX mode.</td></tr>
<tr><td></td><td></td><td></td><td>6:0</td><td>Channel number when TESTREG is set to Code 1 (single channel), number is in 1MHz step relative to 2400MHz</td></tr>
</table>

Table 13-1 Test mode registers.

Note : Output power in test mode is always 0dBm, and any other setting in TXPWR and RXPWR registers is ignored in test mode.

14 Electrical Specifications

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	Operating conditions					
VDD	Supply voltage		2.0	3.0	3.6	V
TEMP	Operating temperature		-20	27	80	ºC
	Digital input pins					
V_{IH}	HIGH level input voltage		0.7·VDD		VDD	V
V_{IL}	LOW level input voltage		VSS		0.3·VDD	V
	Digital output pins					
V_{OH}	HIGH level output voltage (I_{OH}=-0.5mA)		VDD-0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.5mA)		VSS		0.3	V
I_{OH_HD}	High drive source current for DO[1] and DO[3] @ V_{OH}= VDD-0.4V	1		10		mA
	General electrical specification					
I_{PD}	Supply current in power down mode			5		µA
	General RF conditions					
f_{OP}	Operating frequency	2	2400		2521	MHz
Δf	Frequency deviation			+/-640		kHz
R_{GFSK}	GFSK data rate			4000		kbps
BW_{MOD}	Modulation bandwidth				4	MHz
f_{XTAL}	Crystal frequency	3		16		MHz
C_{load}	Crystal load capacitance	3	8	12	16	pF
Δ f_{XTAL}	X-tal frequency tolerance + temperature drift	3			+/-30	ppm
	RF Transmit mode					
P_{RF_0dBm}	Maximum output power (TXPWR=3)	4		0	3	dBm
P_{RF_-5dBm}	Maximum output power (TXPWR=2)	4		-5	0	dBm
P_{RF_-10dBm}	Maximum output power (TXPWR=1)	4		-10	-5	dBm
P_{RF_-20dBm}	Maximum output power (TXPWR=0)	4		-20	-12	dBm
P_{RFC}	RF power control range		16	20		dB
P_{RFCR}	RF power range control resolution				+/-3	dB
P_{BW}	20dB bandwidth for modulated carrier			2500	4000	kHz
	RF Receive mode					
RX_{SENS}	Sensitivity at 0.1% BER			-80		dBm
RX_{MAX}	Maximum received signal		0			dBm
	ATX current consumption					
I_{ATX_0dBm}	Mean supply current in audio streaming mode @ 0dBm output power Sample rate: 32kSPS 44.1kSPS 48kSPS	5		14 17 18		mA mA mA
I_{ATXmax}	Peak supply current in audio streaming mode for all sample rates and output power	5		33.5		mA

[1] Output pin programmed for high current (register RXPIO)

[2] Device operates in the 2400 MHz ISM band (2400-2483 MHz).

[3] For further details on crystal specification, see Ch. 17.2

[4] Antenna load impedance = 100Ω+j175Ω, see chapter 17; application information

[5] $C_{load\_MCLK} \approx 8pF$

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
I_{ATX_-5dBm}	Mean supply current @ -5dBm output power	1,2		16		mA
I_{ATX_-10dBm}	Mean supply current @ -10dBm output power			15.3		mA
$I_{ATX-20dBm}$	Mean supply current @ -20dBm output power			15		mA
	ARX current consumption					
I_{ARX_lnk}	Mean supply current in link mode			32		mA
I_{ARX_au}	Mean supply current in audio streaming mode Sample rate: 32kSPS 44.1kSPS 48kSPS	3, 4		 19.5 23 24		 mA mA mA
	I2S interface timing	(refer to Figure 7-2, Figure 7-3 and Figure 7-4)				
T_{I2S}	I2S clock period		150			ns
t_{sI2S}	DATA and WS (input) setup time to CLK		20			ns
t_{hI2S}	DATA and WS (input) hold time from CLK		20			ns
t_{dI2S}	DATA and WS (output) delay from CLK				40	ns
	MCLK (256 f_S) output clock					
Δf_{MCLK}	Locking range vs nominal MCLK frequency	5	-500		+500	ppm
J_{RMS}	RMS jitter 0-25kHz			250	310	ps
	Slave SPI interface timing	(refer to Figure 7-12)				
T_{SSCK}	SSCK clock period	6	62			ns
t_{suSSPI}	SMOSI setup time to SSCK		10			ns
t_{hdSSPI}	SMOSI hold time from SSCK		10			ns
t_{dSSPI}	SMISO delay from SSCK				55	ns
t_{dSSCK}	SCSN setup time to SSCK		500			µs
t_{SRD}	SPI slave ready		500			µs
t_{SREADY}	SCSN hold time to SSCK		500			µs
	Master SPI interface timing	(refer to Figure 7-7)				
T_{MSCK}	MSCK clock period		125			ns
t_{suMSPI}	MMISO setup time to MSCK		55			ns
t_{hdMSPI}	MMISO hold time from MSCK		10			ns
t_{dMSPI}	MMOSI delay from MSCK				20	ns
t_{dMSCK}	MCSN setup to MSCK		30	500		ns
	Slave 2-wire interface timing	(refer to Figure 7-11)				
T_{SSCL}	2-wire clock period		1000			ns
t_{SW2_dsu}	SSDA setup time to SSCL		50			ns
t_{SW2_dhd}	SSDA hold time from SSCL		65			ns
t_{SW2_od}	SSDA 1->0 delay from SSCL				170	ns
	Master 2-wire interface timing	(refer to Figure 7-6)				
T_{MSCL}	2-wire clock period		1000			ns
t_{MW2_dsu}	MSDA setup time to MSCL		60			ns
t_{MW2_dhd}	MSDA hold time from MSCL		50			ns
t_{MW2_od}	MSDA 1->0 delay from MSCL				50	ns

Table 14-1 nRF24Z1 Electrical specifications.

[1] Sample rate = 44.1 kSPS

[2] $C_{load\_MCLK} \approx 8pF$

[3] $C_{CLK} = C_{WS} = C_{DATA} = C_{MCLK} \approx 10pF$

[4] Peak current in ARX-mode is approx. 34mA

[5] Nominal MCLK frequency is 256 times f_S for f_S in [32kHz, 44.1kHz, 48kHz] programmable

[6] For VDD ≥ 3.0V +/-10%, otherwise minimum T_{SSCK} is 124ns (8MHz)

15 Absolute maximum ratings

Supply Voltages
VDD ..... - 0.3V to + 3.6V
VSS 0V

Input Voltage
V_I.....- 0.3V to VDD + 0.3V

Output Voltage
V_O.....- 0.3V to VDD + 0.3V

Total Power Dissipation
P_D (T_A=80°C) 140mW

Temperatures
Operating temperature ..... - 20°C to + 80°C
Storage temperature .....- 40°C to + 125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!
Electrostatic sensitive device.
Observe precaution for handling.

16 Package outline

nRF24Z1 is packaged in a 36 pin 6 by 6 QFN (all dimensions in mm) matt tin plating.

Package		A	A_1	A2	b	D/E	D1/E1	e	J	K	L	R
Green	**Min**	0.8	0.0	0.65	0.18				4.47	4.47	0.3	1.735
QFN36	**typ.**		0.02		0.23	6 BSC	5.75 BSC	0.5 BSC	4.57	4.57	0.4	1.835
(6x6 mm)	**Max**	0.9	0.05	0.69	0.3				4.67	4.67	0.5	1.935

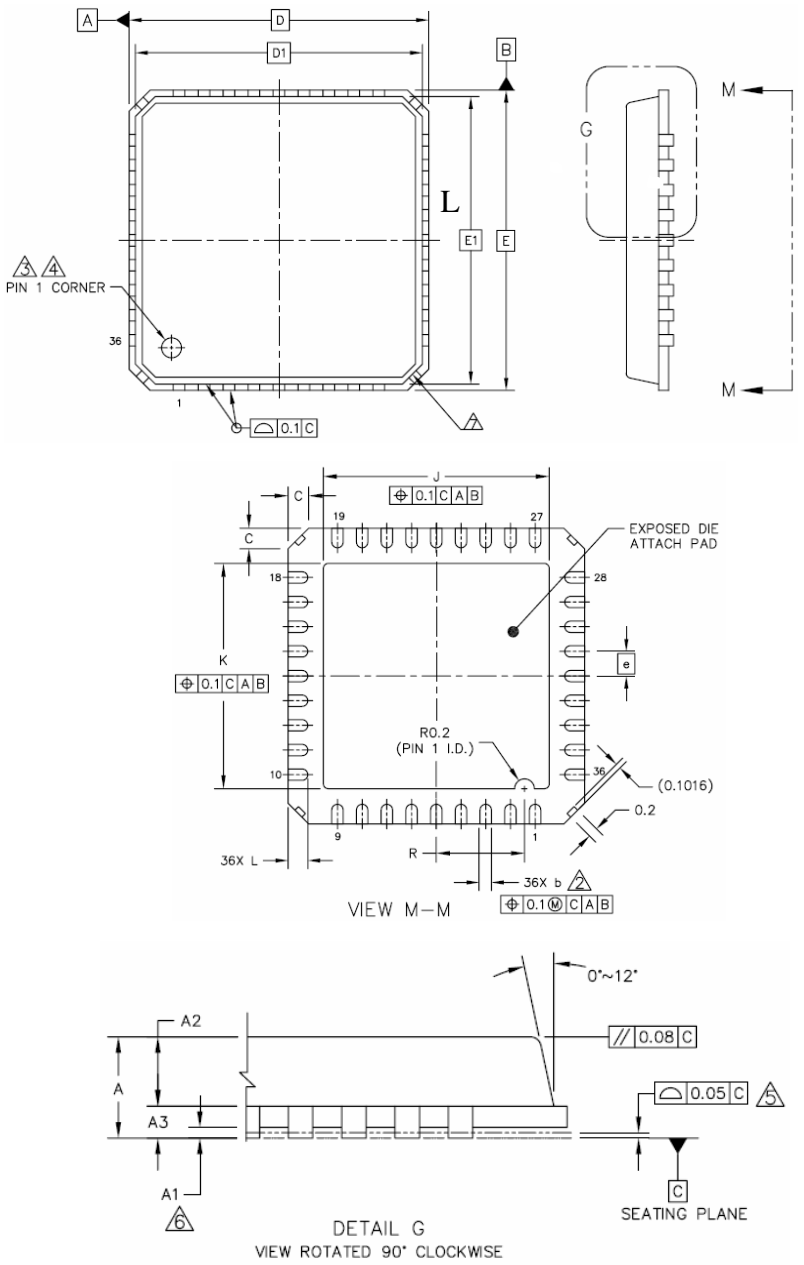


Figure 16-1 nRF24Z1 package outline.

16.1 Package marking

n	R	F		*B*	*X*
D	D	D	D	D	D
Y	*Y*	*W*	*W*	*L*	*L*

Figure 16-2 nRF24Z1 package marking layout

Abbreviations:

DDDDDD – Product number, e.g. 24Z1
B – Build Code, i.e. unique code for silicon revision, production site, package type and test platform
X – "X" grade, i.e. Engineering Samples (optional)
YY – 2 digit Year number
WW – 2 digit Week number
LL – 2 letter wafer lot number code

17 Application Information

17.1 Antenna I/O

The ANT1 & ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD_PA, either via a RF choke or via the center point in a balanced antenna. Differential load impedance between the ANT1 and ANT2 pins, 100Ω+j175Ω, is recommended for maximum output power. Antennas with lower load impedance (for example 50 Ω) can be matched to nRF24Z1 by using a simple matching network.

17.2 Crystal Specification

Tolerance includes initial accuracy and tolerance over temperature and aging.

Frequency	C_L	ESR	C_{0max}	Tolerance
16MHz	8pF – 16pF	100Ω	7.0pF	±30ppm

Table 17-1 Crystal specification of nRF24Z1

In order to obtain a crystal setup with low power consumption and fast start-up time, a crystal with low crystal load capacitance is recommended.

The crystal load capacitance, C_L, is given by:

$$C_L = \frac{C_1' \cdot C_2'}{C_1' + C_2'}, \quad where\ C_1' = C_1 + C_{PCB1} + C_{I1}\ and\ C_2' = C_2 + C_{PCB2} + C_{I2}$$

C_1 and C_2 are SMD capacitors as shown in the application schematics. C_{PCB1} and C_{PCB2} are the layout parasitics on the circuit board. C_{I1} and C_{I2} are the capacitance seen into the XC1 and XC2 pin respectively; the value is typical 1pF.

17.3 Bias reference resistor

A resistor between pin IREF (pin24) and ground sets up the bias reference for the nRF24Z1. A 22 kΩ (1%) resistor is to be fitted. Changing the value of this resistor will degrade nRF24Z1 performance.

17.4 Internal digital supply de-coupling

Pin DVDD (pin15) is a regulated output of the internal digital power supply of nRF24Z1. The pin is purely for de-coupling purposes and only a 33nF (X7R) capacitor is to be connected. The pin must not be connected to external VDD and can not be used as power supply for external devices.

17.5 PCB layout and de-coupling guidelines

A well-designed PCB is necessary especially to achieve good RF performance. Keep in mind that a poor layout may lead to loss of performance, or even functionality if due care is not taken. A fully qualified RF-layout for the nRF24Z1 and its surrounding components, including antenna matching network, can be downloaded from **www.nordicsemi.no**.

A PCB with a minimum of two layers with ground planes is recommended for optimum performance. The nRF24Z1 DC supply voltage must be de-coupled as close as possible to the VDD pins, see Ch.18. A large value surface mount tantalum capacitor (e.g. 10µF) should be placed in parallel with the smaller value capacitors. The nRF24Z1 supply voltage must be filtered and routed separately from the supply voltages of other circuitry. When the nRF24Z1 is used in combination with A/D and D/A converters, it is very important to avoid power supply noise generated by the nRF24Z1 from reaching the analogue supply pins of the A/D and D/A converters. Hence, star-routing directly from a low-noise supply source (e.g. a linear voltage regulator) is highly recommended, and where the nRF24Z1 has its own power supply line from the supply source and also the A/D and D/A converters have their own separate digital and analogue supply lines.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF24Z1 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to place via holes as close as possible to the VSS pins. A minimum of one via hole should be used for each VSS pin.

Full swing digital data or control signals should not be routed close to the reference crystal or the power supply lines.

18 Application example

The following example show nRF24Z1 schematics and layouts where the ATX is controlled over SPI by an external MCU and the ARX has a SPI EEPROM attached for stand alone operation.

Interfaces routed out from the nRF24Z1 are:

- Audio: I2S
- ATX control: SPI slave
- ATX GPIO: DD[1:0]
- ATX external interrupt pin (IRQ)
- ARX GPIO: DI[3:0], DO[3:0]

18.1 nRF24Z1 schematics

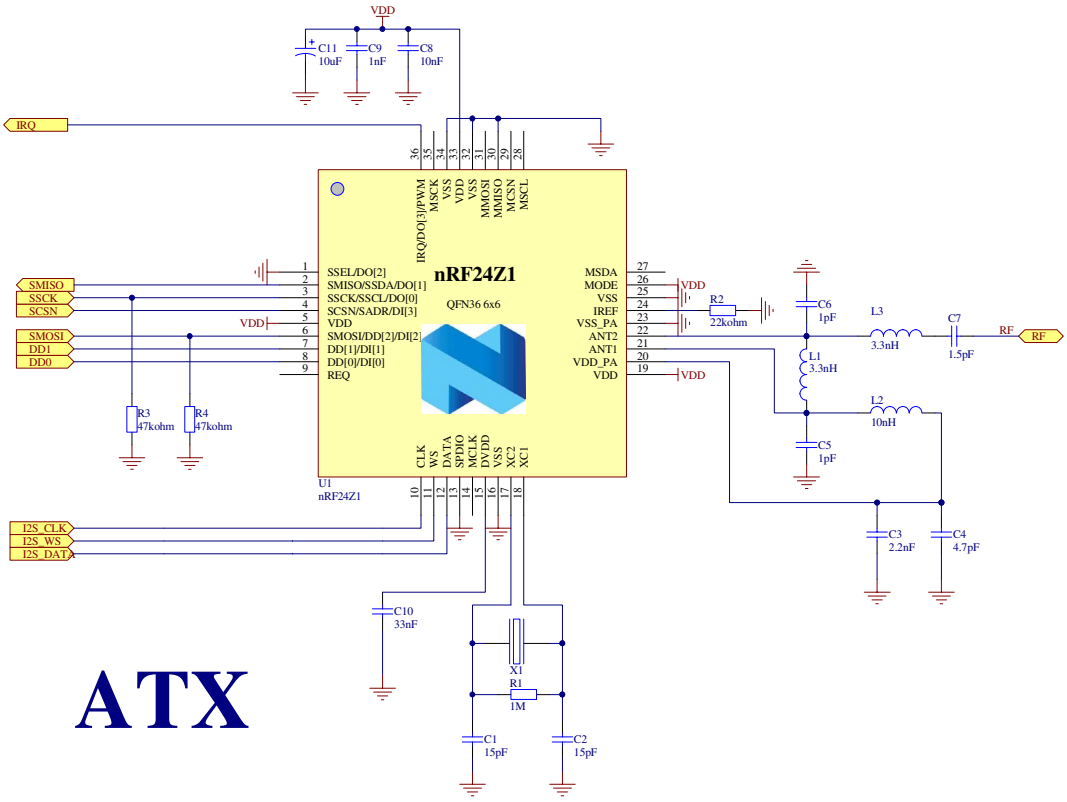


Figure 18-1 nRF24Z1 MCU controlled ATX schematic

Resistors R3 and R4 are not necessary for device functionality. R3 is added to guarantee that no nRF24Z1 registers are changed if the external MCU is resetting. R4 is used to terminate the nRF24Z1 SPI input. This avoids any floating signals if the SPI bus is disabled (power down). Only one resistor on the bus is needed. If the MCU MOSI output has internal pull up/down, it can be omitted.

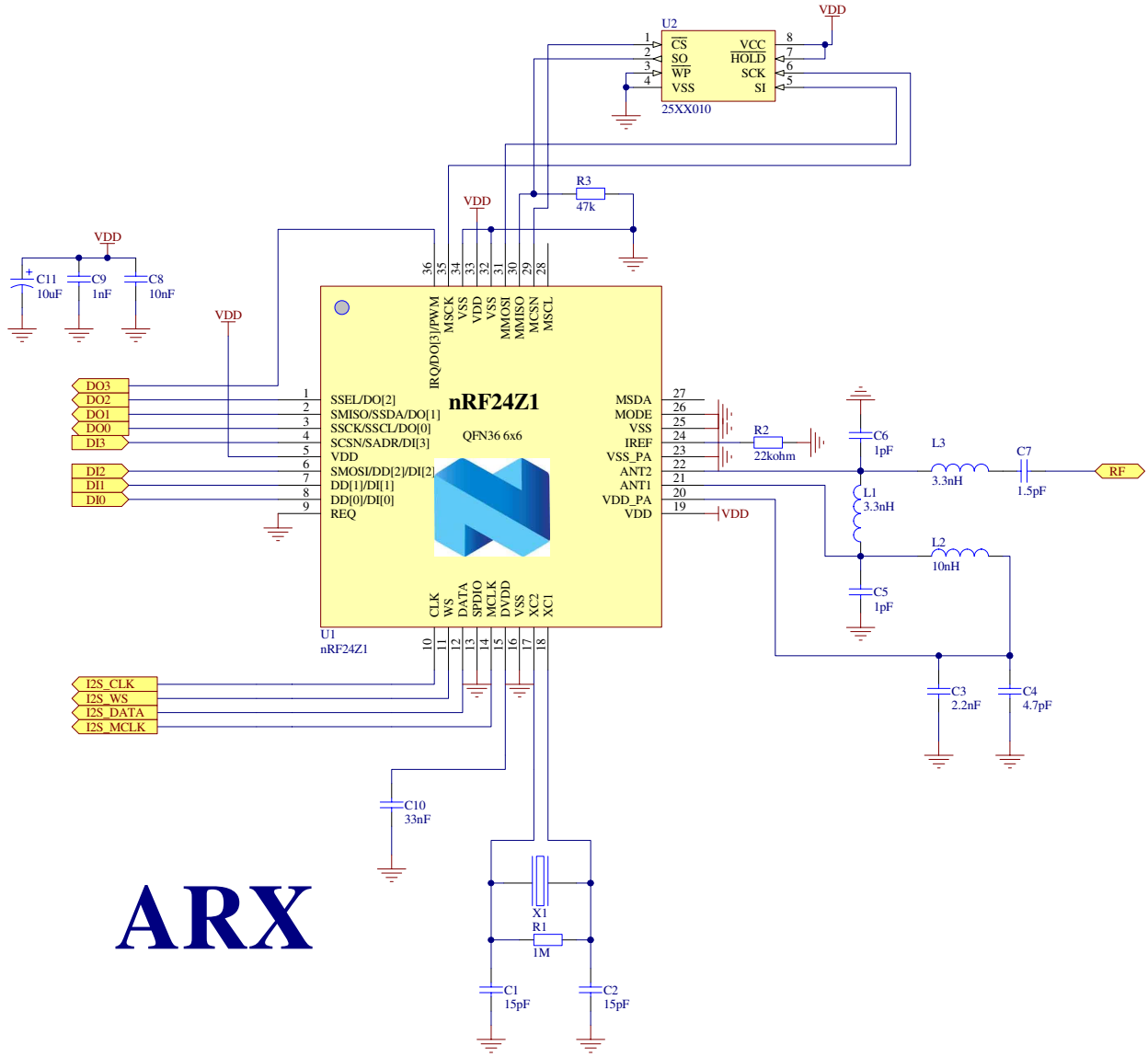
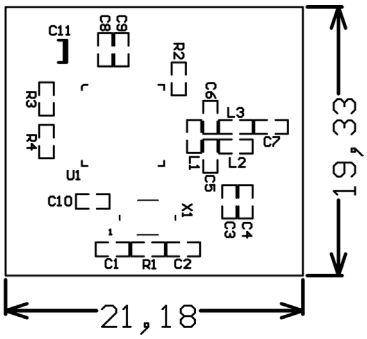


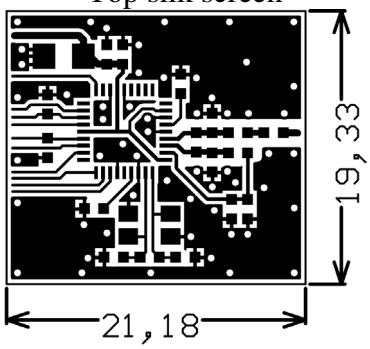
Figure 18-2 nRF24Z1 ARX with SPI EEPROM schematic

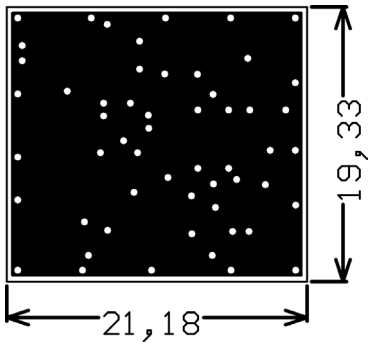
18.2 nRF24Z1 layout



No components on bottom layer

Top silk screen

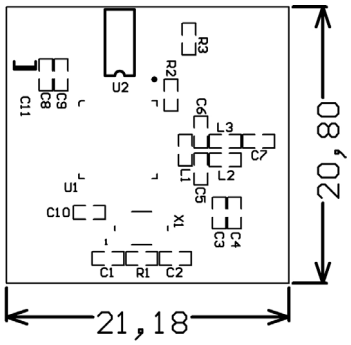




Top layer

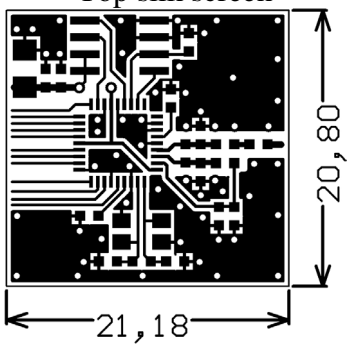
Bottom layer

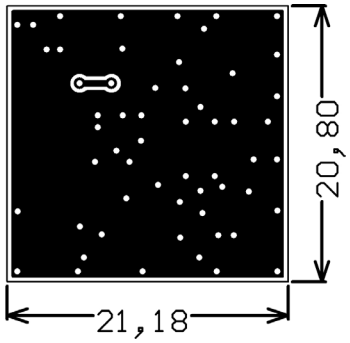
Figure 18-3 nRF24Z1 ATX PCB layout



No components on bottom layer

Top silk screen





Top layer

Bottom layer

Figure 18-4 nRF24Z1 ARX PCB layout

18.3 nRF24Z1 Bill of Materials

18.3.1 ATX BoM

Designator	Value	Description	Footprint
C1	15pF	Capacitor, NP0, +/- 5%	0603
C2	15pF	Capacitor, NP0, +/- 5%	0603
C3	2.2nF	Capacitor, X7R, +/- 10%	0603
C4	4.7pF	Capacitor, NP0, +/- 5%	0603
C5	1pF	Capacitor, NP0, +/- 0.1 pF	0603
C6	1pF	Capacitor, NP0, +/- 0.1 pF	0603
C7	1.5pF	Capacitor, NP0, +/- 0.25pF	0603
C8	10nF	Capacitor, X7R, +/- 10%	0603
C9	1nF	Capacitor, X7R, +/- 10%	0603
C10	33nF	Capacitor, X7R, +/- 10%	0603
C11	10µF	Capacitor, Tantalum, +/- 20%	1206
L1	3.3nH	TOKO LL1608-FS chip inductor series[1]	0603
L2	10nH	Chip Inductor, +/- 5%	0603
L3	3.3nH	TOKO LL1608-FS chip inductor series[1]	0603
R1	1MΩ	Resistor, 10%	0603
R2	22kΩ	Resistor, 1 %	0603
R3	47kΩ	Resistor, 5%	0603
R4	47kΩ	Resistor, 5%	0603
U1	nRF24Z1	2.4 GHz audio streamer	QFN36L/6x6
X1	16MHz	Crystal (Ch.17.2), C_L=9pF, ESR < 100Ω, +/- 30ppm	

Table 18-1 nRF24Z1 ATX BoM

[1] Inductance vs. frequency may differ significantly in inductors with the same value but different part numbers and/or vendors! Inductor value is usually characterized at 100-250 MHz, but the actual value at 2.4 GHz may vary significantly even though the given inductance at 250 MHz is the same.
Inductors from other TOKO series and other vendors may well be used, but antenna matching network performance MUST be verified as the inductor value may need to be changed.

18.3.2 ARX BoM

Designator	Value	Description	Footprint
C1	15pF	Capacitor, NP0, +/- 5%	0603
C2	15pF	Capacitor, NP0, +/- 5%	0603
C3	2.2nF	Capacitor, X7R, +/- 10%	0603
C4	4.7pF	Capacitor, NP0, +/- 5%	0603
C5	1pF	Capacitor, NP0, +/- 0.1 pF	0603
C6	1pF	Capacitor, NP0, +/- 0.1 pF	0603
C7	1.5pF	Capacitor, NP0, +/- 0.25pF	0603
C8	10nF	Capacitor, X7R, +/- 10%	0603
C9	1nF	Capacitor, X7R, +/- 10%	0603
C10	33nF	Capacitor, X7R, +/- 10%	0603
C11	10µF	Capacitor, Tantalum, +/- 20%	1206
L1	3.3nH	TOKO LL1608-FS chip inductor series[1]	0603
L2	10nH	Chip Inductor, +/- 5%	0603
L3	3.3nH	TOKO LL1608-FS chip inductor series*	0603
R1	1MΩ	Resistor, 10%	0603
R2	22kΩ	Resistor, 1 %	0603
R3	47kΩ	Resistor, 5%	0603
U1	nRF24Z1	2.4 GHz audio streamer	QFN36L/6x6
U2	25XX640	EEPROM	SO-8
X1	16MHz	Crystal (see Ch 17.2), C_L=9pF, ESR < 100Ω, +/- 30ppm	

Table 18-2 nRF24Z1 ARX BoM

[1] Inductance vs. frequency may differ significantly in inductors with the same value but different part numbers and/or vendors! Inductor value is usually characterized at 100-250 MHz, but the actual value at 2.4 GHz may vary significantly even though the given inductance at 250 MHz is the same.
Inductors from other TOKO series and other vendors may well be used, but antenna matching network performance MUST be verified as the inductor value may need to be changed.

19 References

For latest version of documents, please visit http://www.nordicsemi.no

20 Definitions

Product Specification Status	
Objective Product Specification	Planned or Under Development. This specification contains the design objectives for product development. Specifications may change in any manner without notice.
Preliminary Product Specification	Engineering Samples and Pre Production series. This specification contains preliminary data. Nordic Semiconductor reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	The product is qualified for production. Changes will be notified according to industry standard criteria for Product/Process Change Notifications.
Obsolete Product Specification	Not In Production. This specification contains specifications on a product that has been discontinued by Nordic Semiconductor. The specification is printed for reference information only.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 20-1 Product status information.

Nordic Semiconductor ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic Semiconductor does not assume any liability arising out of the application or use of any product or circuits described herein.

LIFE SUPPORT APPLICATIONS

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21 Your notes

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