MAX2551

Band II and V WCDMA Femtocell Transceiver with GSM Monitoring

General Description

The MAX2551 is a complete single-chip RF-to-bits and bits-to-RF radio transceiver. This device is in compliance with the 3GPP TS25.104 femtocell standard for Band II and V. It's equipped with multiple receive inputs and transmit outputs for low band, high band, and macro-cell monitoring (Table 1).

This fully integrated transceiver facilitates compact radio designs for dongle and standalone femtocell products by minimizing external component count. Maxim's MAX-PHY serial interface is used to drastically reduce IC pin count, while worldwide field-proven architecture accelerates time to product deployment.

The device features unparalleled receive blocker performance and the industry's lowest noise figure for higher data rates and range. Low-power operational modes are available to minimize power consumption. The transmitter is designed to deliver EVM far exceeding the standard requirement at 0dBm.

The MAX2550–MAX2553 is a family of pin-compatible transceivers to cover all major WCDMA and cdma2000® bands. All parts are controlled by a 4-wire interface.

The MAX2551 is packaged in a compact 7mm x 7mm TQFN and specified over the -40°C to +85°C extended temperature range. A complete radio reference design is available to facilitate custom designs.

Applications

WCDMA Band II and V Femtocells

***Simplified Block Diagram** appears at end of data sheet.*

***Ordering Information** appears at end of data sheet.*

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX2551.related**.*

Benefits and Features

- **Single-Chip Femtocell Radio Transceiver**
- **WCDMA/HSPA+ Band II and V Operation**
- **TS25.104 Standard Compliant**
- **Multiple LNA Inputs for WCDMA, PCS, and GSM Macrocell Monitoring**
- **High Level of Integration**
  - **On-Chip Fractional-N Frequency Synthesizers for LO Generation**
  - **No Tx SAW Filters Required**
  - **Integrated PA Drivers for Lower-Cost Power Amplifier Designs**
  - **12-Bit AFC DAC to Control TCXO**
  - **On-Chip Temperature Sensor**
  - **Three General-Purpose Outputs**
  - **Reference Clock with Selectable CMOS and Low Swing Output**
  - **PLL Lock-Detect Output Through GPO3**
- **Optimized Receiver Performance**
  - **Exceptional Receive Sensitivity**
  - **High Dynamic Range Sigma-Delta ADCs Allow Simple AGC Implementation with Switched Gain States**
- **Optimized Transmitter Performance**
  - **Factory Calibrated for Gain, Carrier Leakage, and Sideband Suppression**
  - **10-Bit Gain Control Resolution for Better Power Accuracy**
  - **60dB Gain Control Range**
- **Loopback Operating Mode from Tx Baseband Input to Rx Baseband Output**
- **MAX-PHY Serial Digital Interface**
- **SPI Read/Write Functionality**
- **Operation Controlled by 4-Wire Serial Interface**
- **Low-Cost 7mm x 7mm TQFN Package**

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ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to GND_ ....-0.3V to +3.9V
RXIN_, MIXIN_, LNAOUT_, to GND_....................-0.3V to +1.2V
All Pins Except $V_{CC\_}$ to GND_................-0.3V to ($V_{CC\_}$ + 0.3V)
AC Input Signals ....1.0V Peak
Digital Input Current... ±10mA
Maximum VSWR Without Damage.. 8:1
Continuous Power Dissipation (T_A = +70°C)
TQFN Multilayer Board
(derate 40mW/°C above +70°C)....................................3.2W

Junction Temperature ....+150°C
Operating Temperature Range.......................... -40°C to +85°C
Storage Temperature Range............................ -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....25°C/W
Junction-to-Case Thermal Resistance (θ_{JC})....................1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = 3.0V to 3.6V, T_A = -40 to +85°C, 50Ω system, f_{REFIN} = 19.2MHz, typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C, unless otherwise noted. Register settings as defined in tables following the specification tables.) (Note 2)

SPEC NO.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC1a	Supply Voltage	$V_{CC\_}$		3.0	3.3	3.6	V
DC19	Operating Supply Current WCDMA	$I_{CC\_}$	Full-duplex high band		312	410	mA
DC20			Full-duplex low band		290	400	
DC21			RXIN4 monitor		75	100	
DC22			RXIN5 monitor		88	120	
DC23			Tx only high band		227	315	
DC24			Tx only low band		218	315	
DC25			Idle Rx		48		
DC26			Idle Tx		48		
DC3	Operating Supply Current AFC-Only Mode	$I_{CC\_}$	AFC DAC and SPI only		175	1000	μA
DC5	Operating Supply Current Reference Buffer Mode	$I_{CC\_}$	REFOUT = 500Ω ll 22pF, all else = off		5.3	7.5	mA
DC6	Operating Supply Current Sleep Mode	$I_{CC\_}$	All functions off		14	1000	μA
DC11	Digital Input Logic-High			1.3			V
DC12	Digital Input Logic-Low					0.4	V
DC13	Input Current for Digital Control Pins					10	|μA|
DC16	GPO Sink Current		V_{OUT} = 0.35V, DOUT_DRV = 01	1.0	1.8		mA
DC17	GPO Source Current		V_{OUT} = $V_{CC\_}$ - 0.3V, DOUT_DRV = 01	1.0	1.9		mA

AC ELECTRICAL CHARACTERISTICS

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred. Typical values are at T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band II Duplexer Specifications

(Diplexer between antenna and duplexer loss: 0.3dB (applies to all Rx modes).)

Antenna—Uplink Port (Applies to Uplink WCDMA Rx Mode on RXIN1)

BAND (MHz)	Uplink 1850 to 1910	1 to 1800	1930 to 1995	1980 to 2020	2020 to 2200	2300 to 2500	2500 to 4500	4500 to 12750
ATTENUATION (dB)	Attenuation	Minimum Attenuation						
	2	35	30	35	37	27	25	15
Rx SAW FILTER RESPONSE								
BAND (MHz)	Out of Band							
ATTENUATION (dB)	Required minimum attenuation relative to in-band							
	25							

Band II Uplink WCDMA Rx Mode on RXIN1 (Full Duplex)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb2fu-0	Frequency Band	WCDMA FDD Band II uplink (lowest to highest channel center frequency)	1852.4		1912.6	MHz
Wb2fu-1	Sensitivity 3GPP TS25.104 Section 7.2.1	Tx on at -27dBm, LNA gain mid gain, PGA gain register set to 9, assumed SNDR > -17.5dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT, LNA linearity set to 0dBm (Note 3)		-118	-107	dBm
Wb2fu-1a	Sensitivity with LNA in High-Gain Mode	Tx on at -27dBm, LNA gain high, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT, LNA linearity set to high		-121	-107	dBm
Wb2fu-3	High-Level EVM WCDMA	P_{IN} = -20dBm, LNA gain low, PGA gain register set to 1		4.5		%

AC ELECTRICAL CHARACTERISTICS

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred. Typical values are at T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band II Uplink WCDMA Rx Mode on RXIN1 (Full Duplex) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb2fu-4	Sensitivity with Adjacent Channel Interference 3GPP TS25.104 Section 7.4.1	Tx on at -27dBm; LNA gain high; PGA gain register set to 3; assumed SNDR > -17.5dB at sensitivity; interfering signals at front-end input -28dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP; using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104; tested by measurement of SNDR at output on CW input signal at -90dBm; SNDR at MAX-PHY filter output established with FFT (Note 3)		-107	-91	dBm
Wb2fu-5	Sensitivity with In-Band Blocking Interference 3GPP TS25.104 Section 7.5	Tx on at -27dBm; LNA gain high; PGA gain register set to 6; assumed SNDR > -17.5dB at sensitivity; interfering signal at front-end input -30dBm at 1900MHz to 2000MHz min, 10MHz offset modulated as in 3GPP; using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104; tested by measurement of SNDR at output on CW input signal at -90dBm; (test only worst case in production); SNDR at MAX-PHY filter output established with FFT (Note 3)		-120	-101	dBm
Wb2fu-6	Sensitivity with Out-of-Band Blocking Interference 3GPP TS25.104 Section 7.5.1	Front-end assumed response as above, Tx on at -27dBm, LNA high gain, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity, interfering signal at front-end input -15dBm CW, 1MHz to 1830MHz and 1930MHz to 2750MHz with 1 MHz steps, no exceptions allowed, (test only worst case in production), using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT (Note 3)		-116	-101	dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred. Typical values are at T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band II Uplink WCDMA Rx Mode on RXIN1 (Full Duplex) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb2fu-8	Sensitivity with Intermodulation Interference 3GPP TS25.104 Section 7.6.1	Tx on at -27dBm; LNA gain high; PGA gain register set to 6; assumed SNDR > -17.5dB at sensitivity; interfering signals at front-end input -38dBm, at 10MHz offset (CW) and 20MHz offset (modulated) as in 3GPP; using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104; tested by measurement of SNDR at output on CW input signal at -90dBm; SNDR at MAX-PHY filter output established with FFT (Note 3)		-118	-101	dBm
Wb2fu-10	Spurious Emissions Out-of-Band 3GPP TS25.104 Section 7.7.1	30MHz to 1GHz, measured in 100kHz BW		-100	-60	dBm
		1GHz to 12.75GHz, measured in 1MHz BW, with the exception of frequencies between 12.5MHz below the first carrier frequency and 12.5MHz above the last carrier frequency used by the BS (Note 3)		-100	-50	
Wb2fu-11	Spurious Emissions in Receive Bands 3GPP TS25.104 Section 7.9.2	Front-end assumed response as above, 1850MHz to 1910MHz (Note 3)		-95	-80	dBm
Wb2fu-12	Conversion Gain High LNA Gain	LNA high gain; PGA gain register set to 6; tested on CW input signal at -90dBm; calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	23	32	39	dB
Wb2fu-13	Conversion Gain Mid LNA Gain	LNA mid gain; PGA gain register set to 9; tested on CW input signal at -90dBm; calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	22	30.5	37	dB
Wb2fu-14	Conversion Gain Low LNA Gain	LNA gain low; PGA gain register set to 1; tested on CW input signal at -20dBm; calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	-13.5	-6.5	-3	dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred. Typical values are at T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Antenna—Downlink Port (Applies to Downlink WCDMA Rx Mode on RXIN5)

BAND (MHz)	Downlink 1930 to 1990	1 to 1910	1850 to 1910	2050 to 3000	2255 to 12750
ATTENTUATION (dB)	Attenuation:	Minimum Attenuation (dB)			
	3.5	15	52	25	15

Band II Downlink WCDMA Rx MODE on RXIN5 (Monitor)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb2fd-0	Frequency Band		1932.4		1992.6	MHz
Wb2fd-1	Sensitivity 3GPP TS25.101 Section 7.3.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, using UL reference measurement channel, (12.2kbps) as specified in C.3.1 3GPP 25.101, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT, LNA linearity set to 0dBm, specified data is for a manual built fcLGA using 2.7pF filter caps		-110		dBm
Wb2fd-8	Spurious Emissions Out-of-Band 3GPP TS25.101 Section 7.9.1	30MHz to 1000MHz in 100kHz bandwidth (Note 3)		-100	-60	dBm
		1000MHz to 12750MHz in 1MHz bandwidth (Note 3)		-96	-50	
Wb2fd-9	Spurious Emissions in Receive Bands 3GPP TS25.101 section 7.9.2	Front-end assumed response as above, 1850MHz to 1910MHz and 1930MHz to 1990MHz (Note 3)		-97	-80	dBm
Wb2fd-10	Conversion Gain High LNA Gain	LNA gain high; PGA gain register set to 11; tested on CW input signal at -90dBm; calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	37	44.5	49	dB
Wb2fd-11	Conversion Gain Low LNA Gain	LNA gain low; PGA gain register set to 0; tested on CW input signal at -20dBm; calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	-18	-12.7	-7.5	dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred. Typical values are at T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

PCS Band GMSK Rx Mode

The signal shares the same path as WCDMA Band II downlink. Losses applied are:

1) Diplexer: 0.3dB
2) Band II duplexer, antenna to downlink port (same as WCDMA table)
3) SPDT: 0.3dB

PCS Band Rx Mode on RXIN5

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
pcs-0	RF Frequency		1930.2		1994.8	MHz
pcs-1	Sensitivity 3GPP TS100.910 Section 6.2	LNA gain high, PGA gain register set to 12, assumed SNDR > 7dB at sensitivity, using static E-TCH/F as specified in 3GPP TS 100.910, tested by measurement of SNDR at ADC output on CW input signal at -102dBm, SNDR at MAX-PHY filter output established with FFT		-108		dBm

Band V Duplexer Specifications

Antenna—Uplink Port (Applies to Uplink WCDMA Rx Mode on RXIN3)

BAND (MHz)	Uplink 824 to 849	1 to 804	869 to 894	894 to 2500	2500 to 3000	3000 to 6000
ATTENUATION (dB)	Attenuation			Minimum Attenuation (dB)		
	2	32	43	32	22	15
Rx SAW FILTER RESPONSE						
BAND (MHz)	Out-of-Band					
ATTENUATION (dB)	Required minimum attenuation relative to in-band					
	25					

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred. Typical values are at T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band V Uplink WCDMA Rx Mode on RXIN3 (Full Duplex)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb5fu-0	Frequency Band	WCDMA FDD Band V uplink (lowest to highest channel center frequency)	821.4		846.6	MHz
Wb5fu-1	Sensitivity 3GPP TS25.104 Section 7.2.1	Tx on at -27dBm, LNA gain mid gain, PGA gain register set to 9, assumed SNDR > -17.5dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT, LNA linearity set to 0dBm (Note 3)		-118	-107	dBm
Wb5fu-2	Sensitivity with LNA in High-Gain Mode	Tx on at -27dBm, LNA gain high, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT, LNA linearity set to high		-121	-107	dBm
Wb5fu-3	High-Level EVM WCDMA	P_{IN} = -20 dBm, LNA gain low, PGA gain register set to 1		4.0		%
Wb5fu-4	Sensitivity with Adjacent Channel Interference 3GPP TS25.104 Section 7.4.1	Tx on at -27dBm; LNA gain high; PGA gain register set to 3; assumed SNDR > -17.5dB at sensitivity; interfering signals at front-end input -28dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP; using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104; tested by measurement of SNDR at output on CW input signal at -90dBm; SNDR at MAX-PHY filter output established with FFT (Note 3)		-104	-91	dBm
Wb5fu-5	Sensitivity with In-Band Blocking Interference 3GPP TS25.104 Section 7.5.1	Tx on at -27dBm; LNA gain high; PGA gain register set to 6; assumed SNDR > -17.5dB at sensitivity; interfering signal at front-end input -30dBm at 1900MHz to 2000MHz min, 10MHz offset modulated as in 3GPP; using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104; tested by measurement of SNDR at output on CW input signal at -90dBm; (test only worst case in production); SNDR at MAX-PHY filter output established with FFT (Note 3)		-120	-101	dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred. Typical values are at T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band V Uplink WCDMA Rx Mode on RXIN3 (Full Duplex) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb5fu-6	Sensitivity with Out-of-Band Blocking Interference 3GPP TS25.104 Section 7.5.1	Front-end assumed response as above; Tx on at -27dBm; LNA gain high; PGA gain register set to 6; assumed SNDR > -17.5dB at sensitivity; interfering signal at Front-end input -15dBm CW; 1MHz to 804MHz and 869MHz to 12750MHz with 1 MHz steps; no exceptions allowed; (test only worst case in production); using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104; tested by measurement of SNDR at output on CW input signal at -90dBm; SNDR at MAX-PHY filter output established with FFT (Note 3)		-118	-101	dBm
Wb5fu-7	Sensitivity with Intermodulation Interference 3GPP TS25.104 Section 7.6.1	Tx on at -27dBm; LNA gain high; PGA gain register set to 6; assumed SNDR > -17.5dB at sensitivity; interfering signals at front-end input -38dBm, at 10MHz offset (CW) and 20MHz offset (modulated) as in 3GPP; using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104; tested by measurement of SNDR at output on CW input signal at -90dBm; SNDR at MAX-PHY filter output established with FFT (Note 3)		-117	-101	dBm
Wb5fu-8	Spurious Emissions Out-of-Band 3GPP TS25.104 Section 7.7.1	30MHz to 1GHz, measured in 100kHz BW		-100	-60	dBm
		1GHz to 12.75GHz, measured in 1MHz BW, with the exception of frequencies between 12.5MHz below the first carrier frequency and 12.5MHz above the last carrier frequency used by the BS (Note 3)		-84	-50	
Wb5fu-10	Conversion Gain High LNA Gain	LNA high gain; PGA gain register set to 6; tested on CW input signal at -90dBm; calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	25	32.5	37	dB
Wb5fu-11	Conversion Gain Mid LNA Gain	LNA mid gain; PGA gain register set to 9; tested on CW input signal at -90dBm; calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	23.5	30	35	dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred. Typical values are at T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band V Uplink WCDMA Rx Mode on RXIN3 (Full Duplex) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb5fu-12	Conversion Gain Low LNA Gain	LNA gain low; PGA gain register set to 1; tested on CW input signal at -20dBm; calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	-14.5	-8	-4	dB

Antenna—Downlink Port (Applies to Downlink WCDMA Rx Mode on RXIN4)

BAND (MHz)	Downlink 869 to 894	1 to 804	824 to 849	914 to 3000	3000 to 6000
ATTENUATION (dB)	Attenuation:	Minimum Attenuation (dB)			
	3	37	51	35	20

Band V Downlink WCDMA Rx Mode on RXIN4 (Monitor)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb5fd-0	Frequency Band		867.4		891.6	MHz
Wb5fd-1	Sensitivity 3GPP TS25.101 Section 7.3.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT, LNA linearity set to 0dBm, specified data is for a manual built fcLGA using 2.7pF filter caps		-111.5	-104.7	dBm
Wb5fd-4	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1	LNA gain high; PGA gain register set to 11; assumed SNDR > -7dB at sensitivity; interfering signals at front-end input -52dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP; using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101; tested by measurement of SNDR at output on CW input signal at -90dBm; SNDR at MAX-PHY filter output established with FFT		-111		dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred. Typical values are at T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band V Downlink WCDMA Rx Mode on RXIN4 (Monitor) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb5fd-9	Spurious Emissions Out-of-Band 3GPP TS25.101 Section 7.9.1 (Note 3)	30MHz to 1000MHz, 100kHz bandwidth		-100	-60	dBm
		1000MHz to 12750MHz, 1MHz bandwidth		-98	-50	
Wb5fd-10	Spurious Emissions in Receive Bands 3GPP TS25.101 Section 7.9.2	Front-end assumed response as above, 824MHz to 849MHz and 869MHz to 894MHz (Note 3)		-95	-80	dBm
Wb5fd-11	Conversion Gain High LNA Gain	LNA gain high; PGA gain register set to 11; tested on CW input signal at -90dBm; calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	40	45	48	dB
Wb5fd-12	Conversion Gain Low LNA Gain	LNA gain low; PGA gain register set to 0; tested on CW input signal at -20dBm; calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the16-bit output	-17.5	-13.5	-8.5	dB

GSM850 Band Rx Mode

The signal shares the same path as WCDMA Band V downlink. Losses applied are:

1) Diplexer: 0.3dB
2) Band V duplexer, antenna to downlink port (same as WCDMA table)
3) SPDT: 0.3dB

GSM850 Band GMSK Monitor on RXIN4

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
G850-0	RF Frequency		865.2		893.8	MHz
G850-1	Sensitivity 3GPP TS100.910 Section 6.2	LNA gain high, PGA gain register set to 12, assumed SNDR > 7dB at sensitivity (GSM), using static E-TCH/F as specified in 3GPP TS 100.910, tested by measurement of SNDR at output on CW input signal at -102dBm, SNDR at MAX-PHY filter output established with FFT		-110	-104	dBm

Tx MODE AC ELECTRICAL CHARACTERISTICS

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, WCDMA downlink TM1 16 channels with -14dBFs peak level into sigma-delta modulator inside baseband chip (see the *Baseband Input Level* section), registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, typical values are at T_A = +25°C, $V_{CC\_}$ = 3.3V, and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
W1	RF Frequency Range	Center of the WCDMA signal, Band II output (TXOUTH)	1932.4		1992.6	MHz
W1a		Band V output (TXOUTL)	867.4		891.6	MHz
W2	Linear Output Power	TX_GAIN = 1023	0			dBm
W3	Adjacent Channel Power Ratio	Offset frequency = ±5MHz in 3.84MHz BW, P_{OUT} = 0dBm (Note 3)		-55	-50	dBc
W4	Alternate Channel Power Ratio	Offset frequency = ±10MHz in 3.84MHz BW, P_{OUT} = 0dBm (Note 3)		-70	-60	dBc
W5	Rx Band Noise Power, $P_{OUT} \leq$ 0dBm	Noise measured at -80MHz offset in 3.84MHz BW, then convert to per Hz, Band II output		-153	-142	dBm/Hz
W5a		Noise measured at -45MHz offset in 3.84MHz BW, then convert to per Hz, Band V output		-152	-142	dBm/Hz
W6	EVM	P_{OUT} = 0dBm		3.3		%
W6a	RCDE	TM6, 8 channels at 0dBm		-28		dB
W7	Minimum Output Power	TX_GAIN = 0		-61	-50	dBm
W8	Output Power Deviation from T_A = +25°C to -40°C	TX_GAIN = 1023, high band	-0.5	+2	+3.5	dB
		Low band	-1	+0.5	+2.5	
W9	Output Power Deviation from T_A = +25°C to +85°C	TX_GAIN = 1023, high band	-4	-2	-1	dB
		Low band	-2.5	-1	0	
W10	Power Control Step Size Accuracy	Five calibration points over the power control range to create four linear regions, any linearly interpolated 1dB TX_GAIN step over the specified power range (W2 and W7) will produce 1dB output power step within this error range.		±0.25		dB
W11	Power Control Step Size Accuracy	Five calibration points over the power control range to create four linear regions, any linearly interpolated 10dB TX_GAIN step over the specified power range (W2 and W7) will produce 10dB output power step within this error range.		±0.75		dB

AC ELECTRICAL CHARACTERISTICS: General

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE FREQUENCY INPUT						
R1	Input Level	Test condition	125		600	mV_{P-P}
R2	Input Frequency	Reference divider set to divide-by-2 for frequencies higher than 26MHz	13	19.2	40	MHz
REFERENCE FREQUENCY OUTPUT						
RO1a	REFOUT Output Level, AC	500Ω ll 22pF load, REFOUT_LV_CMOS_SEL = 1	110	320	500	mV_{P-P}
RO1b	REFOUT Output Level, DC			0.8		V
RO2	REFOUT Output Amplitude	500Ω ll 22pF load, REFOUT_LV_CMOS_SEL = 0	2.4	2.7		V_{P-P}
RO4	REFOUT Output Frequency	Matches REFIN frequency (FREF)	13	19.2	40	MHz
Rx DIGITAL LOW-VOLTAGE DIFFERENTIAL SIGNALING OUTPUT INTERFACE						
LV0	Output Bit Rate on Each I and Q	Test condition		153.6		Mbps
LV1	Output Common Mode			1.2		V
LV3	Output Differential Swing on Load	120Ω differential output load (Note 3)	100	140	220	mV_{PEAK}
LV4	Differential Output Resistance			670		Ω
Tx BASEBAND INTERFACE						
Bb1	Input Bit Rate, on Each I and Q	Test condition		153.6		Mbps
Bb8	Common Mode Input Voltage			1.25		V
Bb9	Differential Input Swing		112	140	500	mV_{P-P}
bb10	Differential Input Resistance (Note 3)	Bit TXINDACZI = 1	55	100	140	Ω
bb11		Bit TXINDACZI = 0	140	220	340	
Rx RF PLL						
RS1	Valid RF Main Division Ratio Range		62		147	
RS3	Valid Main Fractional Divider Programming Value	20-bit resolution	00000		FFFFF	hex
RS5	Charge-Pump Current Gain	Using 800µA setting	0.5	0.82	1.0	mA
RS6a	VCO Tuning Gain	RXVCO, high band	21	65	111	MHz/V
RS6b		RXVCO, low band	38	127	216	
RS9	PLL Settling Time	50kHz loop bandwidth		200		µs

AC ELECTRICAL CHARACTERISTICS: General (continued)

(MAX2551 MAX-PHY FPGA evaluation platform, T_A = -40°C to +85°C, registers set as described in Tables 20–51, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Tx RF PLL						
TS2	Valid RF Main Division Ratio Range		66		153	
TS3	Valid Reference Division Ratios	Division ratios are 1 or 2	1		2	
TS4	Valid Main Fractional Divider Programming Value	20-bit resolution	00000		FFFFF	hex
TS5	Charge-Pump Current CP	800µA	0.5	0.82	1.0	mA
TS9	PLL Settling Time	50kHz loop bandwidth		200		µs
DAC1	Resolution	Monotonicity is production tested		12		Bits
AFC DAC						
DAC3	Output-Voltage High	Load > 200kΩ to GND, AFCDAC = all 1	2.55	2.68		V
DAC4	Output-Voltage Low	Load > 200kΩ to $V_{CC\_}$, AFCDAC = all 0		0.37	0.45	V
DAC5	Output Noise	Any code within 0.5V to 2.5V output level, 100Hz to 20kHz		6		µV/rtHz
DAC6	Settling Time	Step from 0.6V to 2V, settling to ±10mV				µs
DIGITAL TEMPERATURE SENSOR						
T1	Output Code vs. Temperature	T_A = -40°C		5		°/code
T2		T_A = +25°C		17		
T3		T_A = +85°C		27		
T5	Code Slope	T_A = -20°C to +70°C		5		
ISOLATION						
M1	RXIN_ Pin-to-Pin Isolation	Between any RXIN_ pins, with one of the two ports disabled		30		dB
M2	TXOUT_ to RXIN_ Isolation	Between any TXOUT and RXIN_, with both ports on		60		dB

Note 2: Production tested at T_A = +25°C. Cold and hot are guaranteed by design and characterization.
Note 3: Guaranteed by design and characterization.

General Comments

MAX-PHY

MAX-PHY is Maxim's solution for the digital interface system between the radio IC and the baseband/DSP. It is a multimode, software programmable, digital signal post-processing engine that processes the data out of the radio IC and produces the digital filtered outputs for use in the DSP. It enables multimode operation of the radio through software control. Maxim offers an evaluation kit for the MAX2551 along with an FPGA-based MAX-PHY evaluation platform. The FPGA includes the recommended digital channel-selection filters. The Verilog code for these filters is also available for integration into the DSP. Contact Maxim for further information.

Additional Information

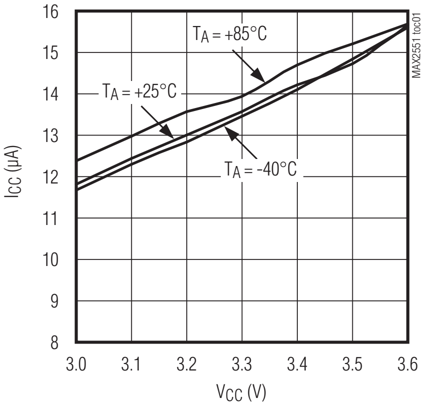
The specifications in the following pages calculate sensitivity with a specified front-end loss from a measured signal-to-noise and distortion ratio (SNDR) and an assumed minimum output $SNDR_{SENS}$ needed for demodulation at sensitivity. The sensitivity values can be related to noise figure by the formula:

Noise Figure of MAX2551 (dB) = Sensitivity (dBm) - Front-End Loss (dB) - $SNDR_{SENS}$ (dB) + 174dBm/Hz - 10 x LOG(bandwidth in Hz)

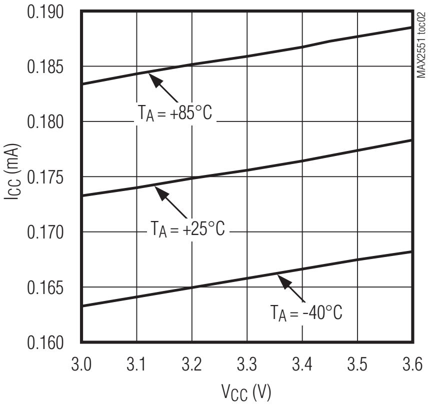
Low-noise amplifier (LNA) and programmable-gain amplifier (PGA) gain are set according to the Conditions column in the *Electrical Characteristics* table. The output SNDR is measured using MAX-PHY and the bandwidth of the measurement is defined by the digital filters in MAX-PHY. DC at the output is excluded from the SNDR measurement. SNDR is calculated using an FFT of the output bytes with a typical FFT length of 2^{14} output samples.

Typical Operating Characteristics

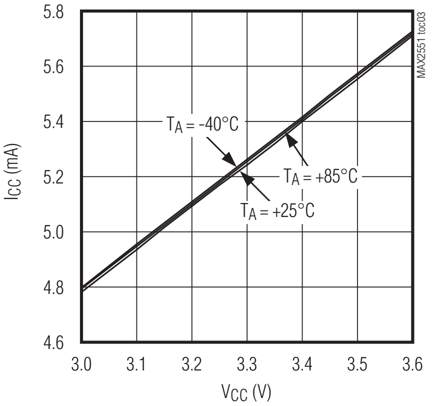
(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)



SLEEP MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE



AFC-ONLY MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE

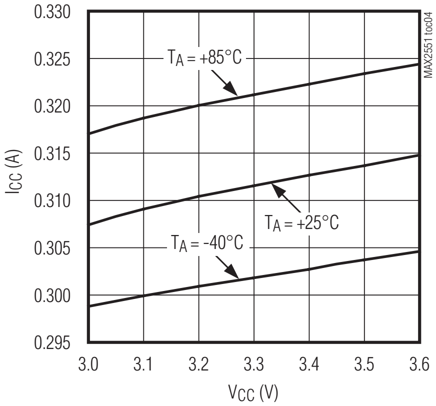


REFERENCE BUFFER MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE

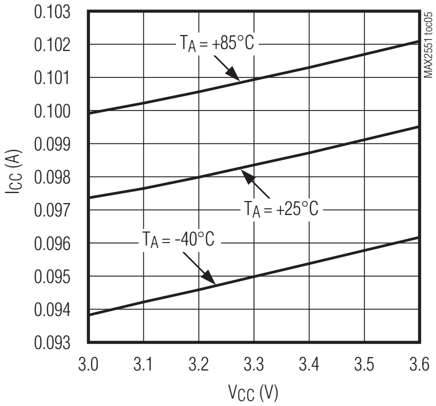
Typical Operating Characteristics (continued)

(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

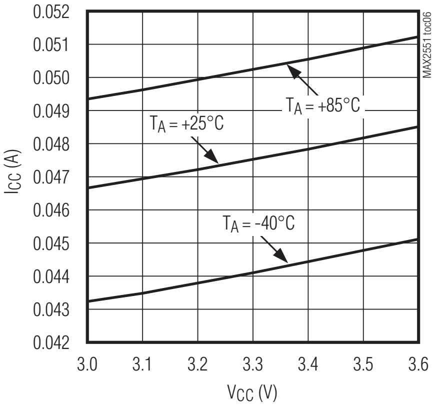
FULL-DUPLEX MODE (HIGH BAND)
SUPPLY CURRENT vs. SUPPLY VOLTAGE



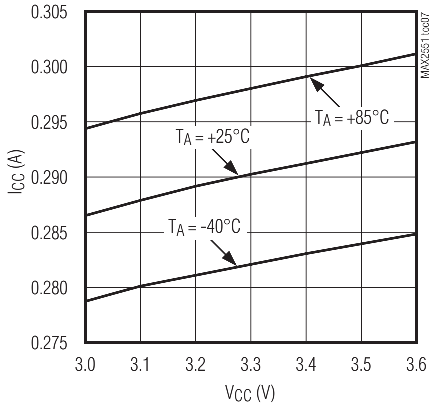
RX1-ONLY MODE
SUPPLY CURRENT vs. SUPPLY VOLTAGE



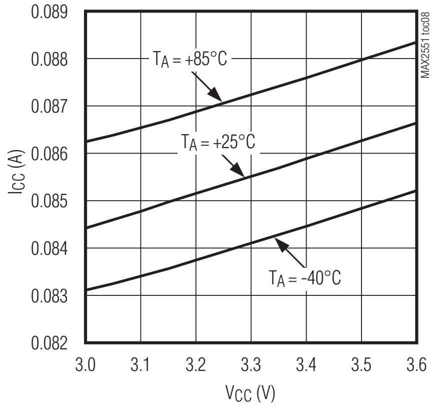
Rx IDLE MODE (HIGH BAND)
SUPPLY CURRENT vs. SUPPLY VOLTAGE



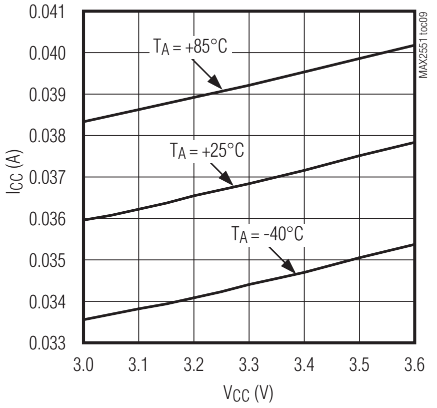
FULL-DUPLEX MODE (LOW BAND)
SUPPLY CURRENT vs. SUPPLY VOLTAGE



RXIN3-ONLY MODE (LOW BAND)
SUPPLY CURRENT vs. SUPPLY VOLTAGE

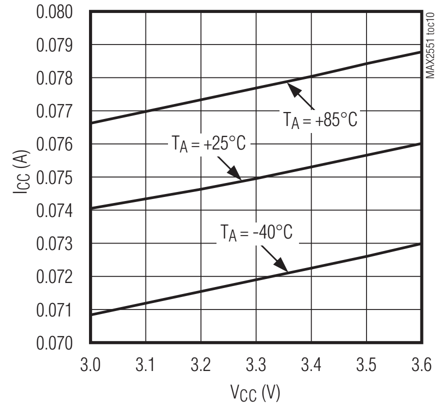


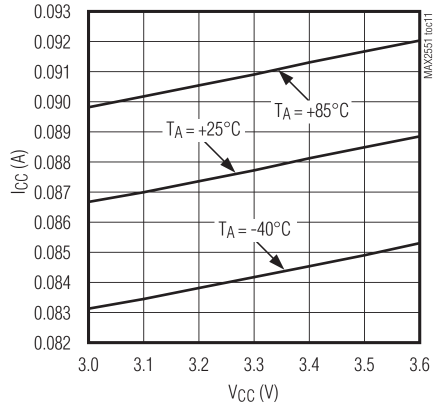
Rx IDLE MODE (LOW BAND)
SUPPLY CURRENT vs. SUPPLY VOLTAGE

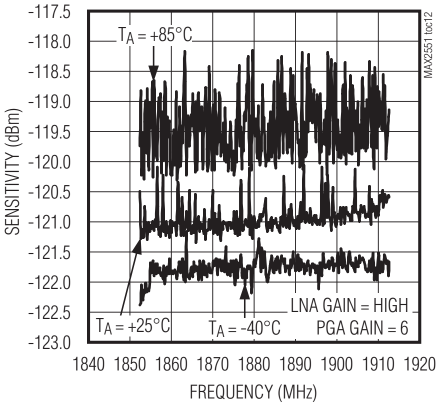


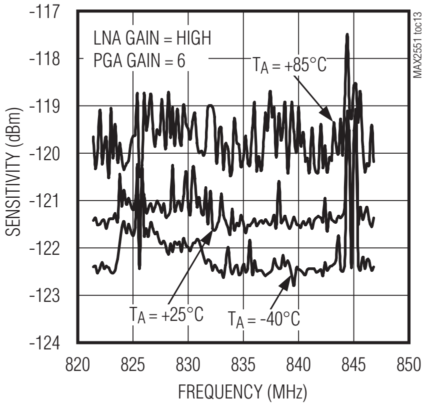
Typical Operating Characteristics (continued)

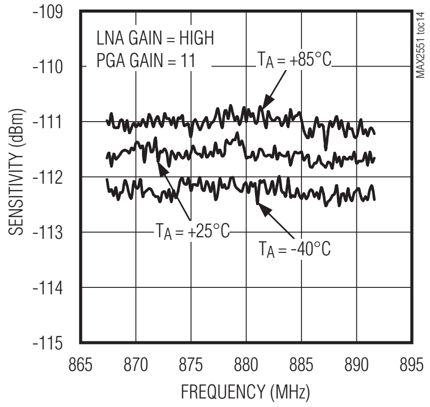
(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

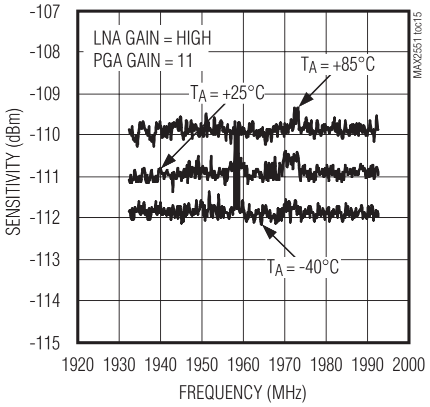

RXIN4 MONITOR MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE


RXIN5 MONITOR MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE


RXIN1 SENSITIVITY vs. FREQUENCY


RXIN3 SENSITIVITY vs. FREQUENCY

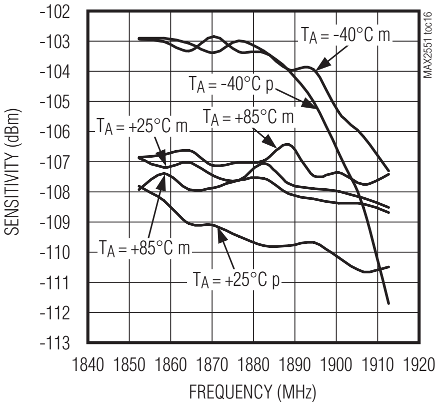

RXIN4 SENSITIVITY vs. FREQUENCY


RXIN5 SENSITIVITY vs. FREQUENCY

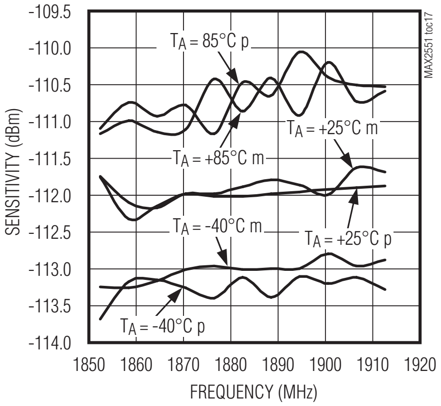
Typical Operating Characteristics (continued)

(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

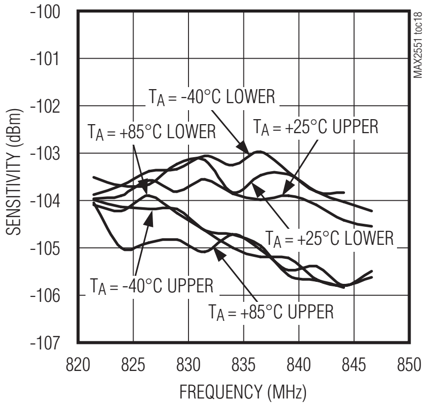
RXIN1 SENSITIVITY vs. FREQUENCY WITH -28dBm ADJACENT CHANNEL INTERFERENCE LNA GAIN = HIGH, PGA GAIN = 3



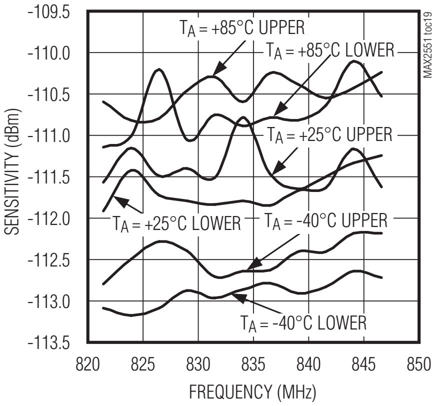
RXIN1 SENSITIVITY vs. FREQUENCY WITH -28dBm ADJACENT CHANNEL INTERFERENCE LNA GAIN = MID, PGA GAIN = 6



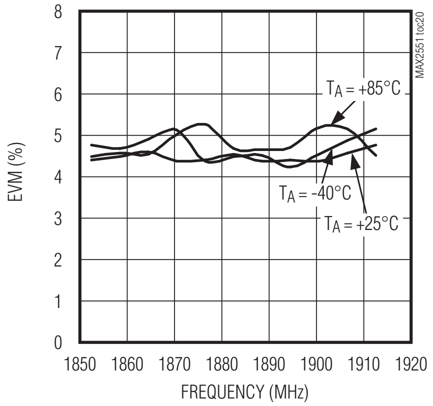
RXIN3 SENSITIVITY vs. FREQUENCY WITH -28dBm ADJACENT CHANNEL INTERFERENCE LNA GAIN = MAX, PGA GAIN = 3



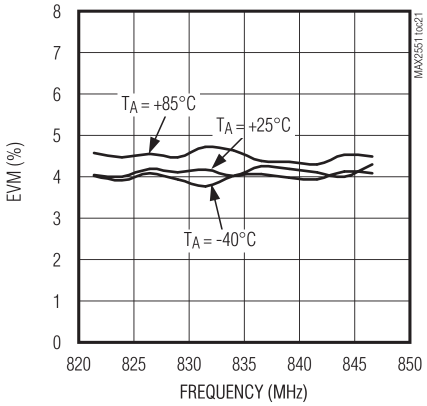
RXIN3 SENSITIVITY vs. FREQUENCY WITH -28dBm ADJACENT CHANNEL INTERFERENCE LNA GAIN = MID, PGA GAIN = 6



RXIN1 EVM vs. FREQUENCY

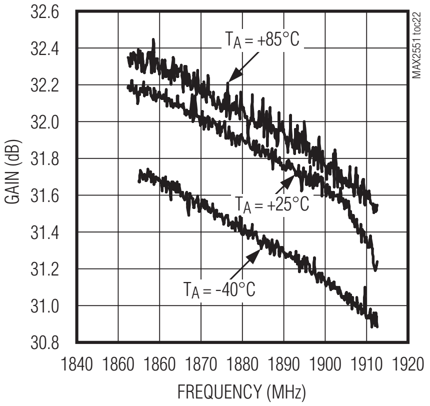


RXIN3 EVM vs. FREQUENCY

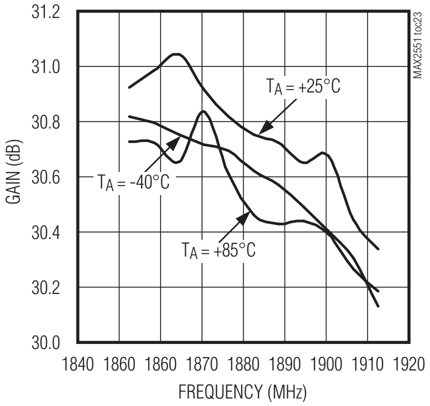


Typical Operating Characteristics (continued)

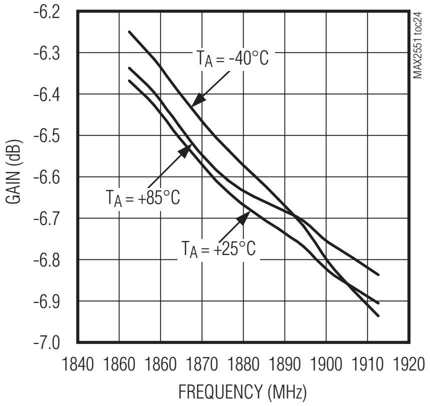
(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)



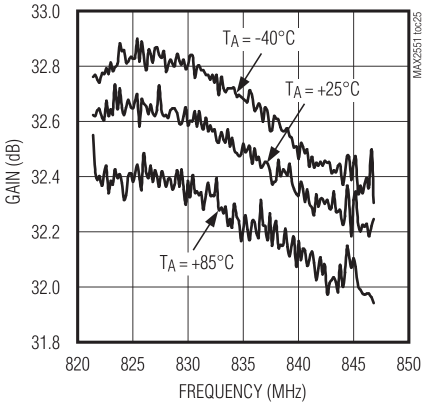
RXIN1 GAIN vs. FREQUENCY
LNA = HIGH, PGA = 6



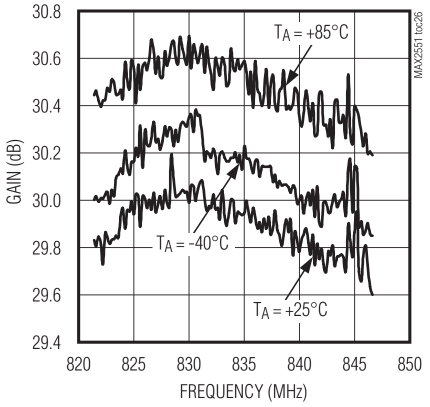
RXIN1 GAIN vs. FREQUENCY
LNA = MID, PGA = 9



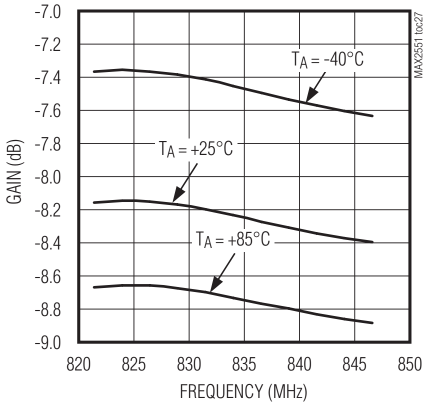
RXIN1 GAIN vs. FREQUENCY
LNA = LOW, PGA = 1



RXIN3 GAIN vs. FREQUENCY
LNA = HIGH, PGA = 6



RXIN3 GAIN vs. FREQUENCY
LNA = MID, PGA = 9

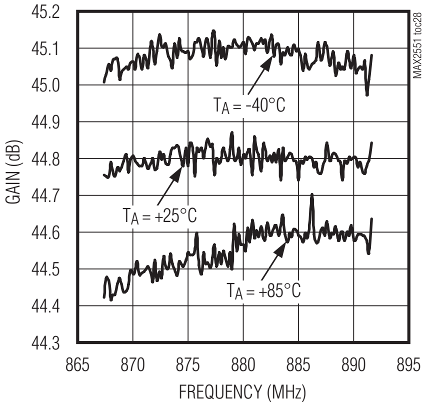


RXIN3 GAIN vs. FREQUENCY
LNA = LOW, PGA = 1

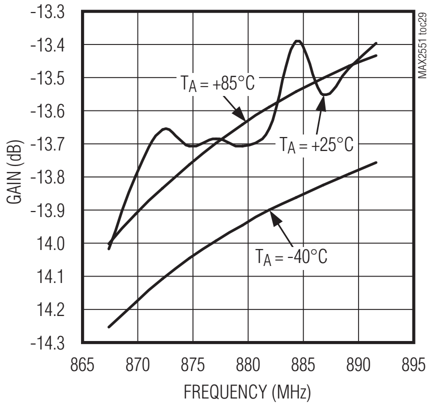
Typical Operating Characteristics (continued)

(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

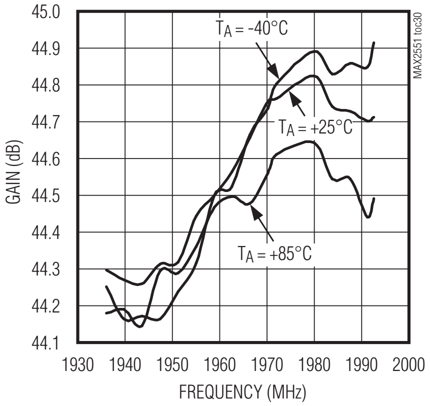
RX4 GAIN vs. FREQUENCY
LNA = HIGH, PGA = 11



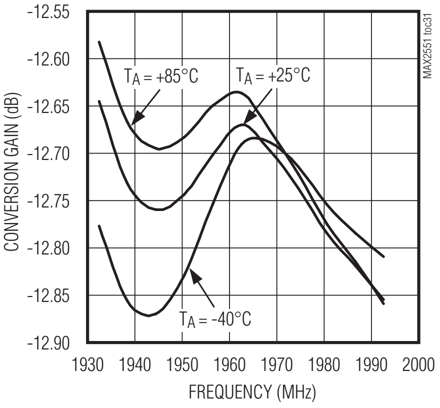
RX4 GAIN vs. FREQUENCY
LNA = LOW, PGA = 0



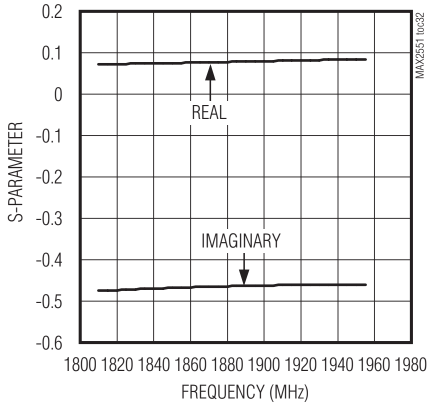
RXIN5 GAIN vs. FREQUENCY
LNA = HIGH, PGA = 11



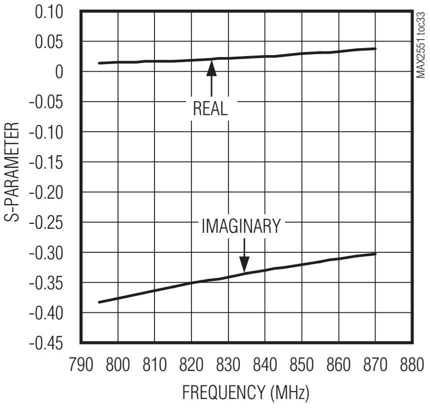
RX5 GAIN vs. FREQUENCY
LNA = LOW, PGA = 0



RXIN1 S-PARAMETER



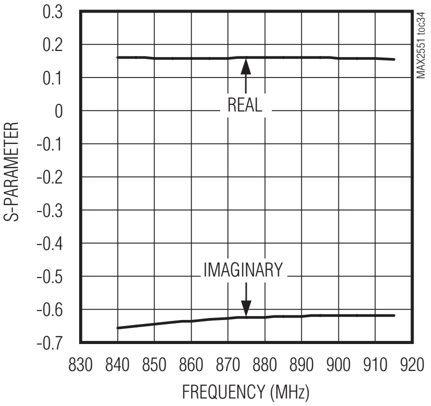
RXIN3 S-PARAMETER



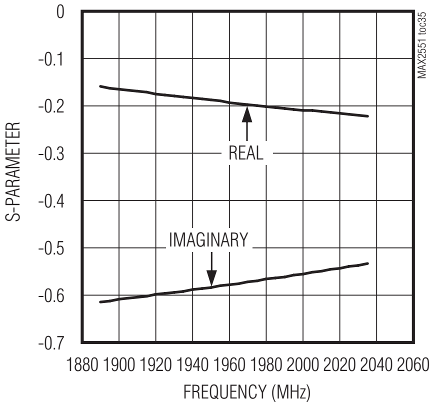
Typical Operating Characteristics (continued)

(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

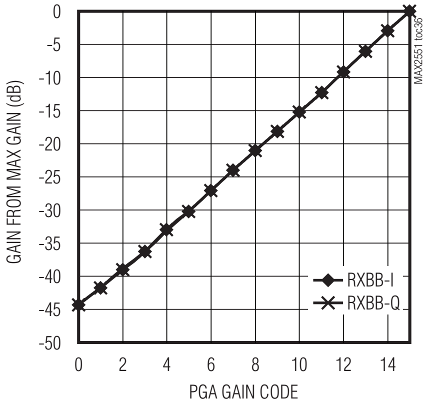
RXIN4 S-PARAMETER



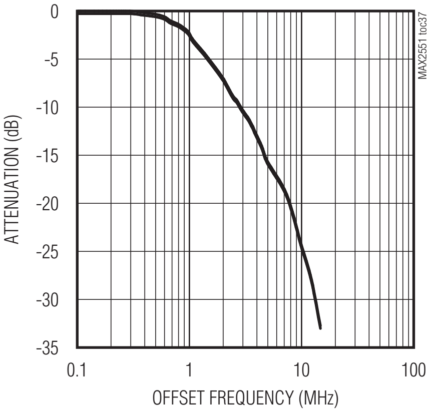
RXIN5 S-PARAMETER



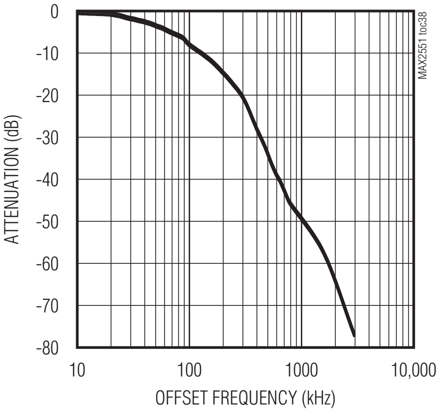
Rx GAIN vs. PGA GAIN CODE



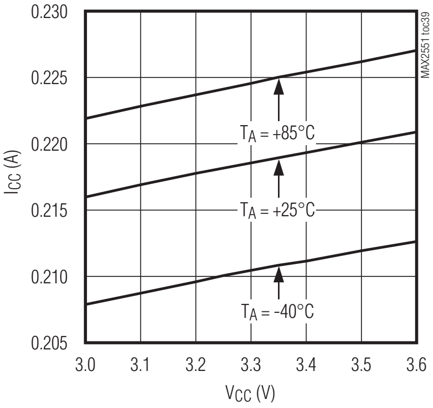
WCDMA FILTER RESPONSE vs. OFFSET FREQUENCY



GSM FILTER RESPONSE vs. OFFSET FREQUENCY



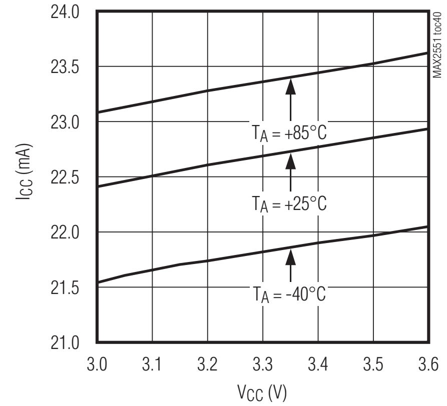
Tx-ONLY MODE (LOW BAND) SUPPLY CURRENT vs. SUPPLY VOLTAGE



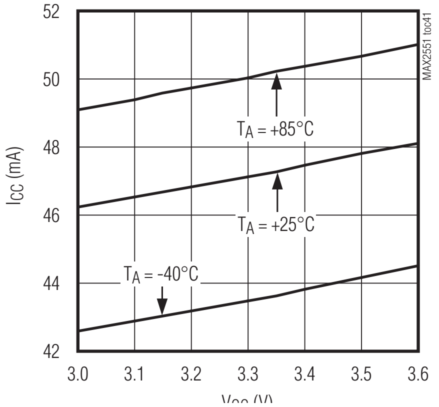
Typical Operating Characteristics (continued)

(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

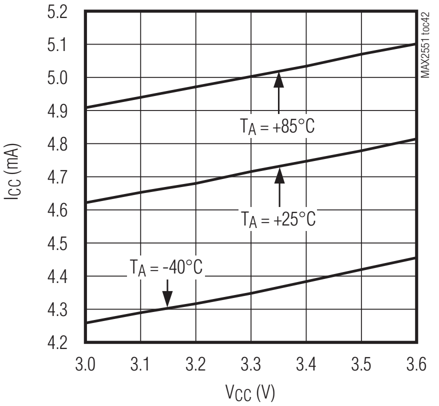
Tx-ONLY MODE (HIGH BAND) SUPPLY CURRENT vs. SUPPLY VOLTAGE



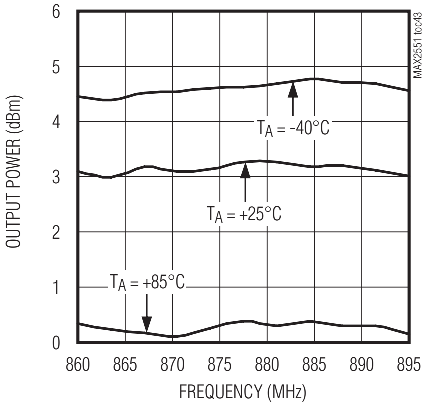
Tx IDLE MODE (LOW BAND) SUPPLY CURRENT vs. SUPPLY VOLTAGE



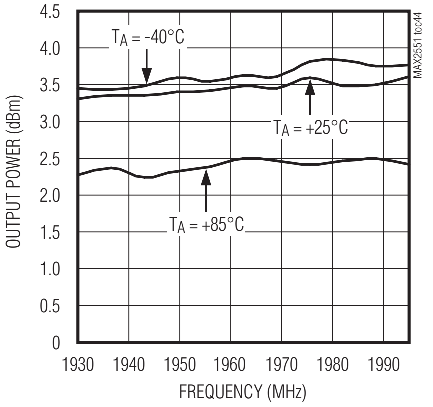
Tx IDLE MODE (HIGH BAND) SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAXIMUM OUTPUT POWER (LOW BAND) vs. FREQUENCY



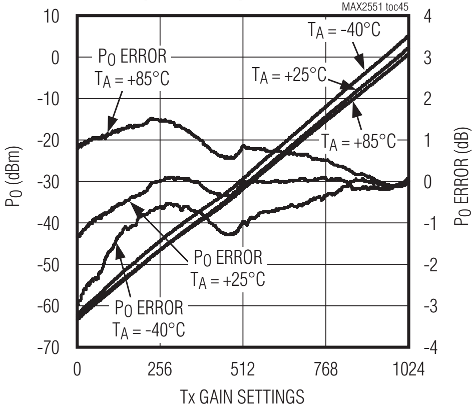
MAXIMUM OUTPUT POWER (HIGH BAND) vs. FREQUENCY



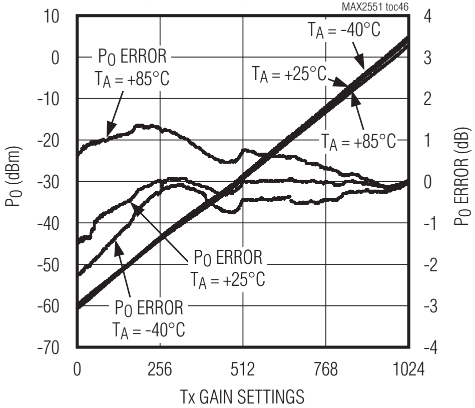
Typical Operating Characteristics (continued)

(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

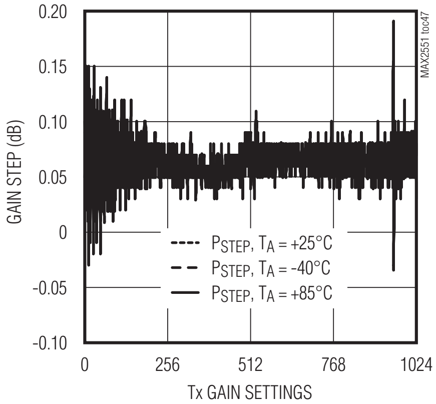
Tx OUTPUT POWER AND OUTPUT POWER ERROR (LOW BAND) vs. GAIN SETTINGS



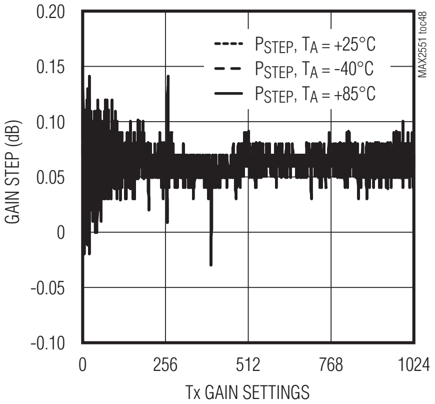
Tx OUTPUT POWER AND OUTPUT POWER ERROR (HIGH BAND) vs. GAIN SETTING



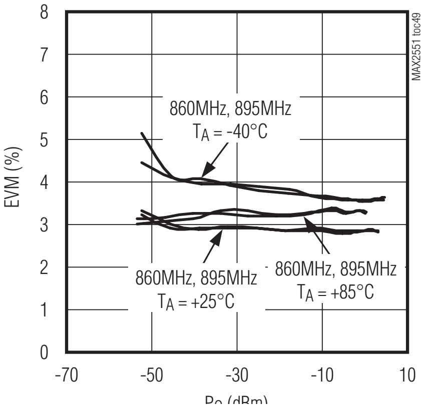
Tx GAIN STEP (LOW BAND) vs. GAIN SETTINGS



Tx GAIN STEP (HIGH BAND) vs. GAIN SETTING



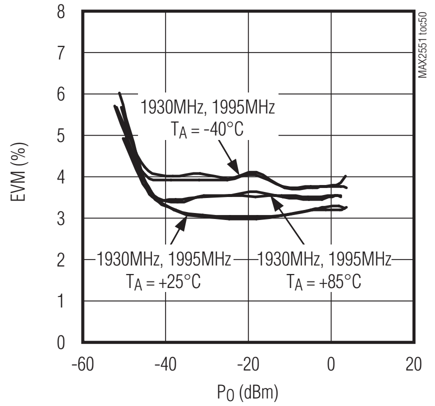
Tx TM1 EVM (LOW BAND) vs. OUTPUT POWER



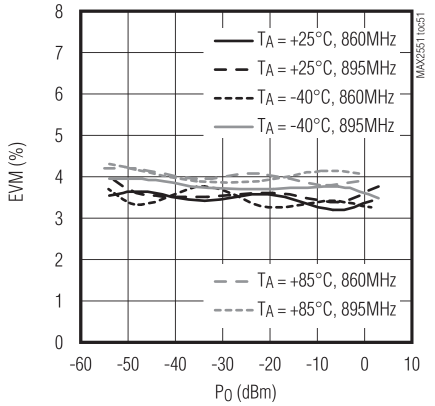
Typical Operating Characteristics (continued)

(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

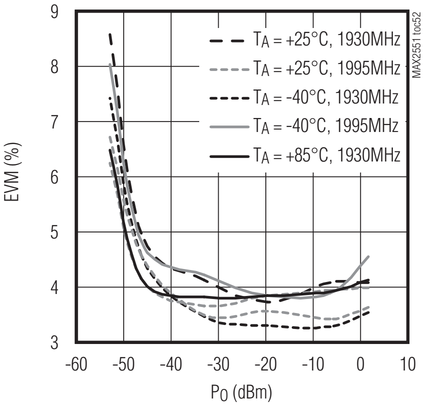
Tx TM1 EVM (HIGH BAND) vs. OUTPUT POWER



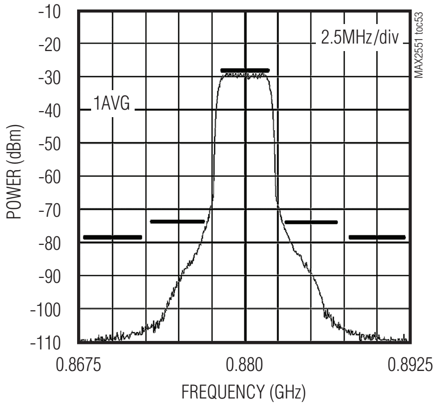
Tx TM6 EVM (LOW BAND)



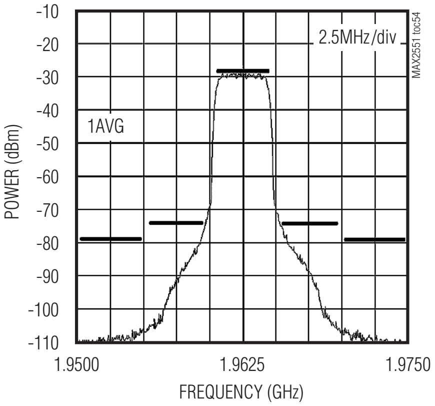
Tx TM6 EVM (HIGH BAND) vs. OUTPUT POWER



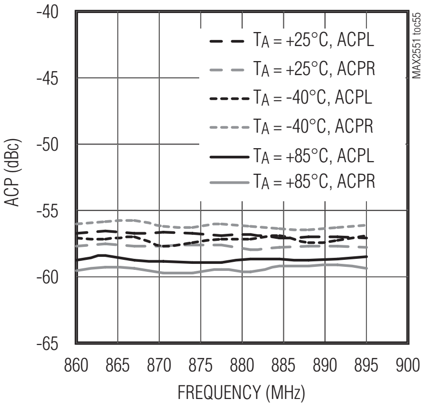
Tx OUTPUT SPECTRUM at 0dBm (LOW BAND)



Tx OUTPUT SPECTRUM at 0dBm (HIGH BAND)

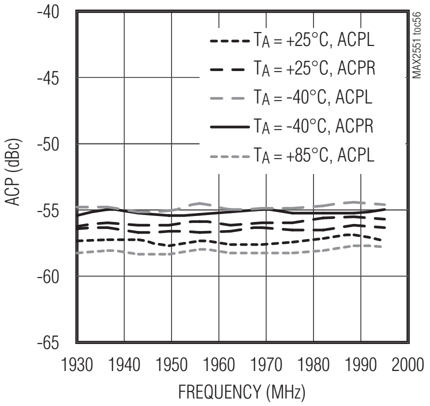


ADJACENT CHANNEL POWER (LOW BAND) RATIO vs. FREQUENCY P_{OUT} = 0dBm

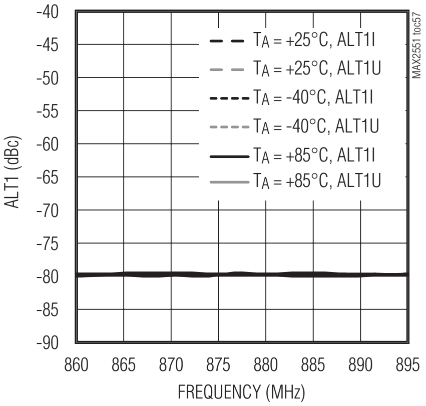


Typical Operating Characteristics (continued)

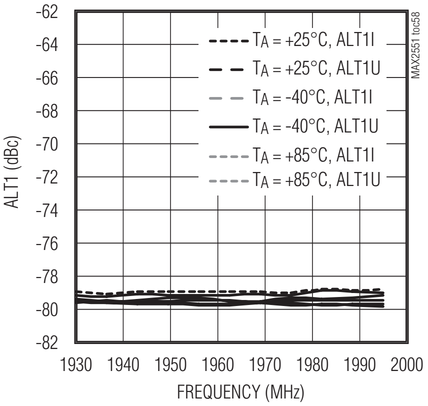
(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)



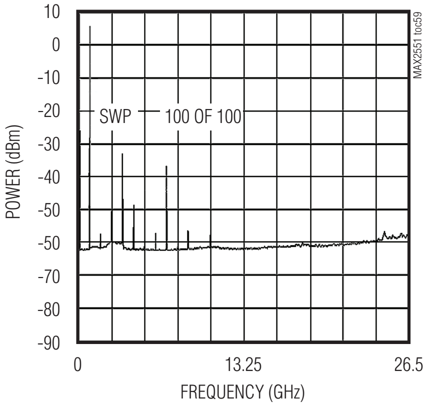
ADJACENT CHANNEL POWER (HIGH BAND) RATIO vs. FREQUENCY
P_{OUT} = 0dBm



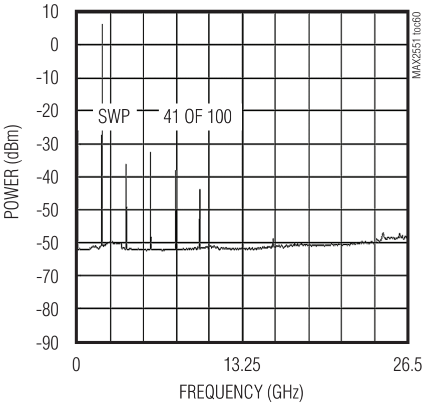
ALTERNATE CHANNEL POWER (LOW BAND) RATIO vs. FREQUENCY
P_{OUT} = 0dBm



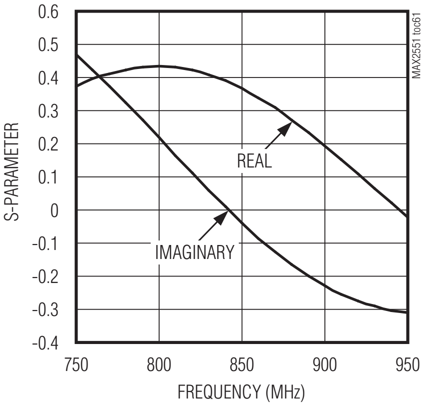
ALTERNATE CHANNEL POWER (HIGH BAND) RATIO vs. FREQUENCY
P_{OUT} = 0dBm



Tx OUTPUT SPECTRUM (LOW BAND)



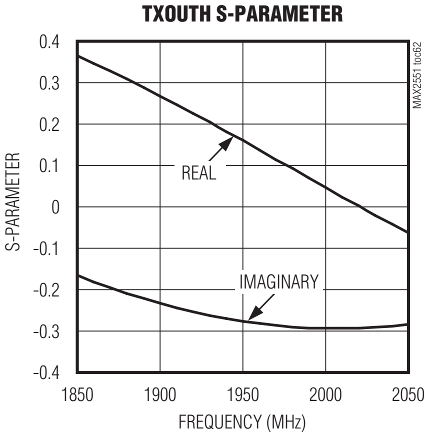
Tx OUTPUT SPECTRUM (HIGH BAND)

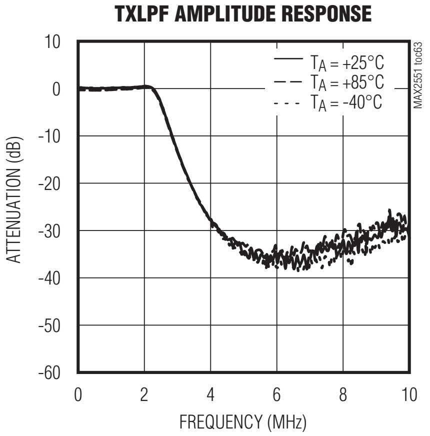


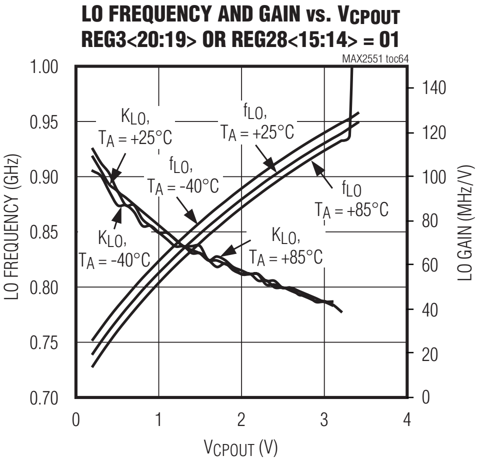
TXOUTL S-PARAMETER

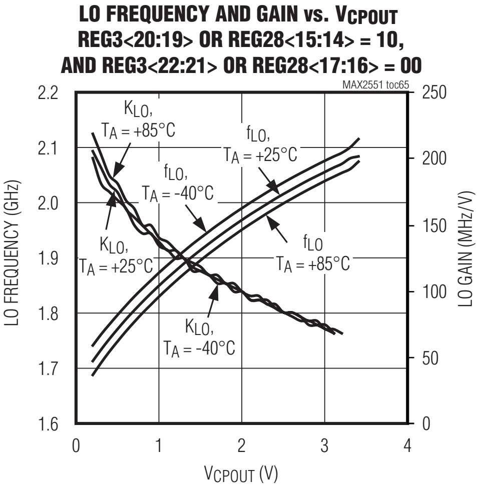
Typical Operating Characteristics (continued)

(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)


TXOUTH S-PARAMETER

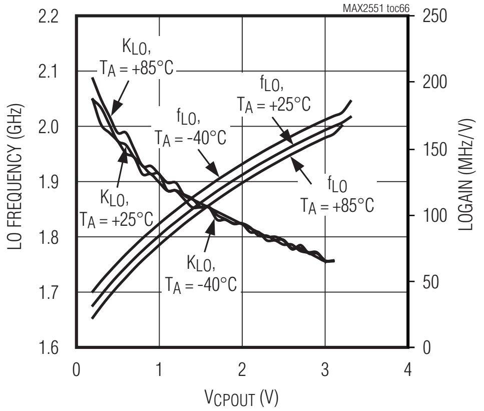

TXLPF AMPLITUDE RESPONSE

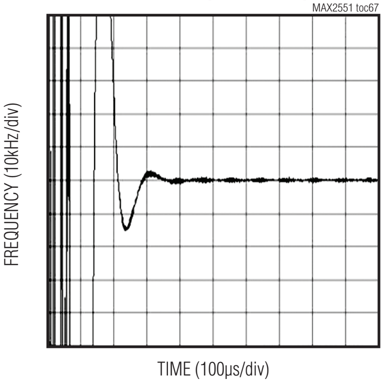

LO FREQUENCY AND GAIN vs. V_{CPOUT}
REG3<20:19> OR REG28<15:14> = 01

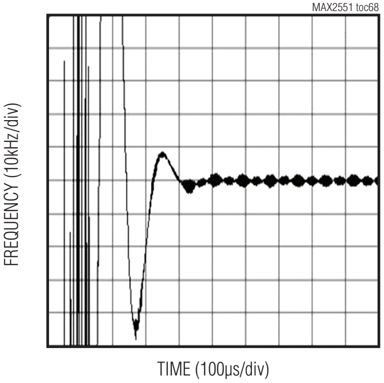

LO FREQUENCY AND GAIN vs. V_{CPOUT}
REG3<20:19> OR REG28<15:14> = 10,
AND REG3<22:21> OR REG28<17:16> = 00

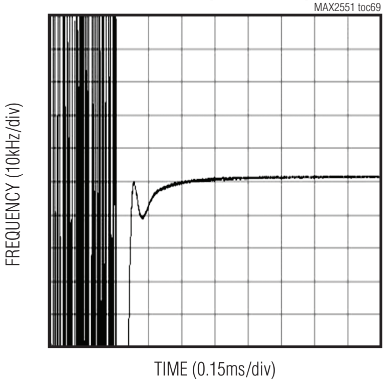
Typical Operating Characteristics (continued)

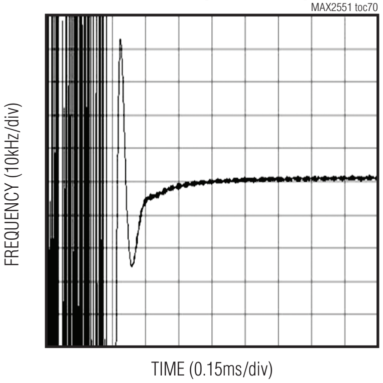
(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)


LO FREQUENCY AND GAIN vs. V_{CPOUT} REG3<20:19> OR REG28<15:14> = 10, AND REG3<22:21> OR REG28<15:14> = 01


Rx TURN-ON FREQUENCY SETTLING (LOW BAND)


Rx TURN-ON FREQUENCY SETTLING (HIGH BAND)

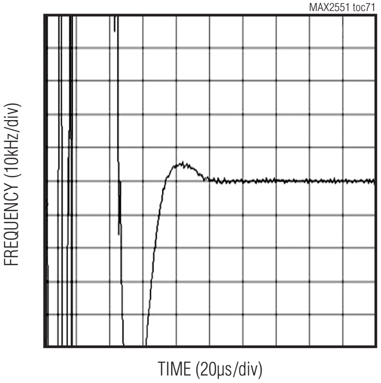

Rx CHANNEL-SWITCH FREQUENCY SETTLING (LOW BAND)


Rx CHANNEL-SWITCH FREQUENCY SETTLING (HIGH BAND)

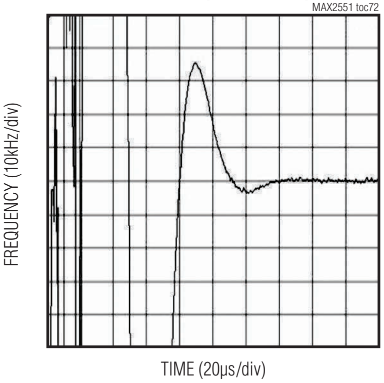
Typical Operating Characteristics (continued)

(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

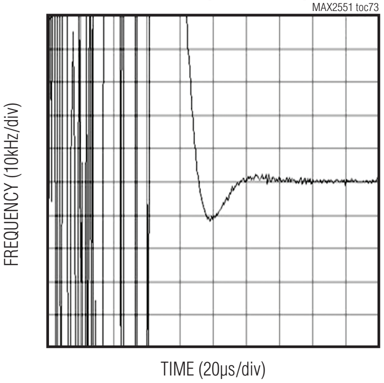
Tx TURN-ON FREQUENCY SETTLING (LOW BAND)



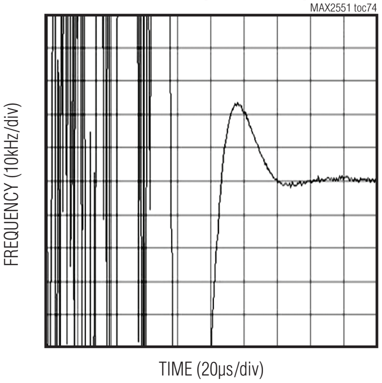
Tx TURN-ON FREQUENCY SETTLING (HIGH BAND)



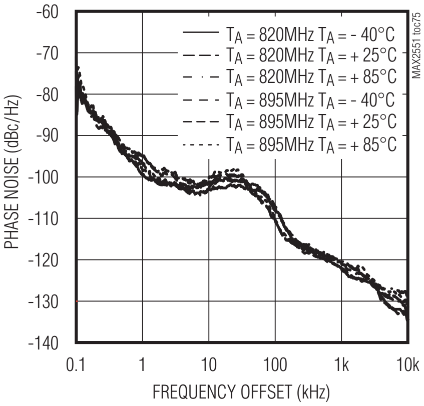
Tx CHANNEL-SWITCH FREQUENCY SETTLING (LOW BAND)



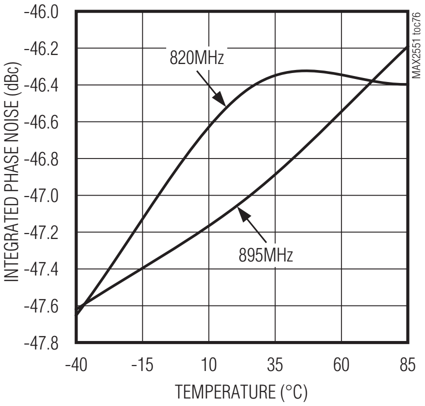
Tx CHANNEL-SWITCH FREQUENCY SETTLING (HIGH BAND)



LO PHASE NOISE (LOW BAND) vs. FREQUENCY OFFSET



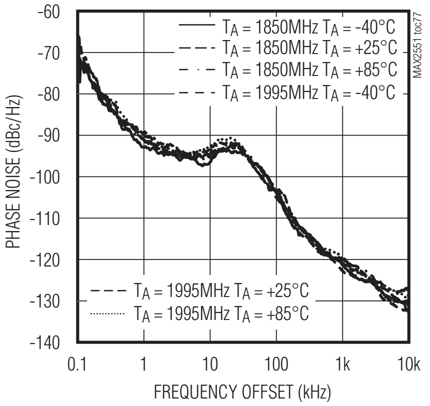
INTEGRATED PHASE NOISE (LOW BAND) vs. TEMPERATURE



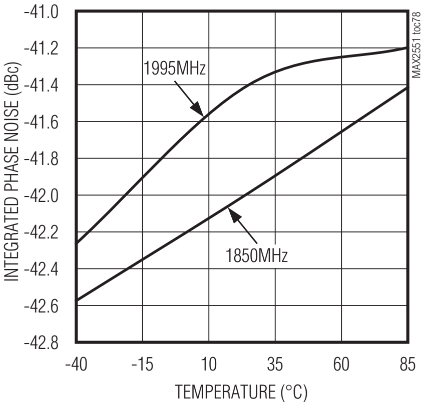
Typical Operating Characteristics (continued)

(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

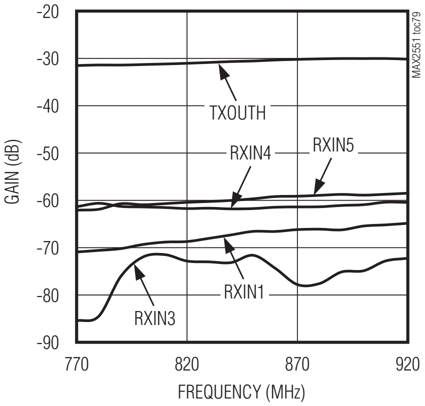
LO PHASE NOISE vs. FREQUENCY OFFSET



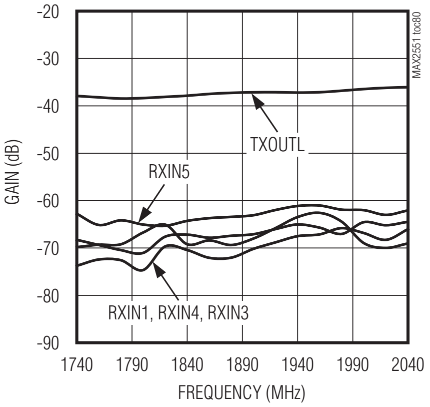
INTEGRATED PHASE NOISE (HIGH BAND) vs. TEMPERATURE



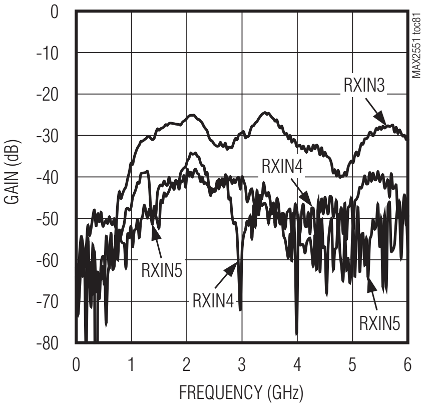
GAIN FROM TXOUTL TO OTHER RF PORTS vs. FREQUENCY



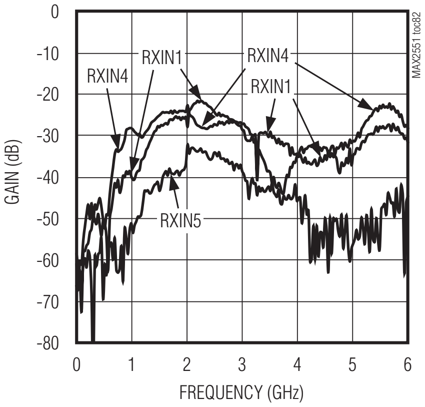
GAIN FROM TXOUTH TO OTHER RF PORTS vs. FREQUENCY



GAIN FROM OTHER RF PORTS TO RXIN1 vs. FREQUENCY

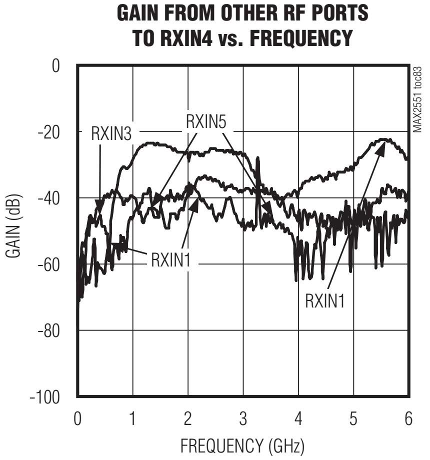


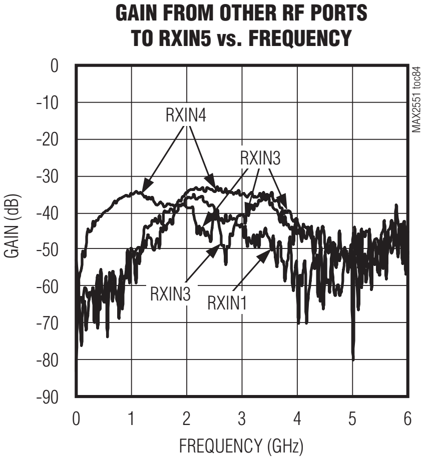
GAIN FROM OTHER RF PORTS TO RXIN3 vs. FREQUENCY

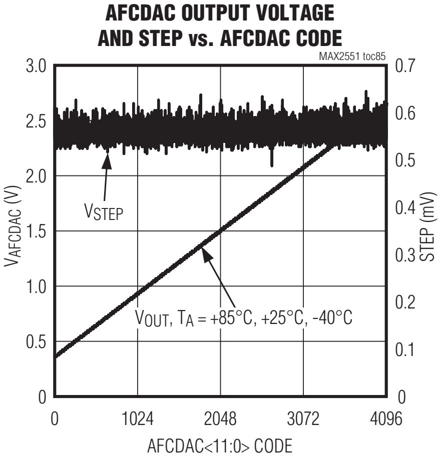


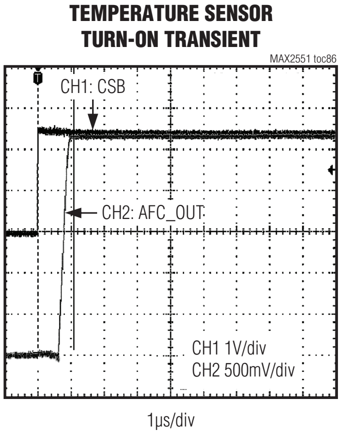
Typical Operating Characteristics (continued)

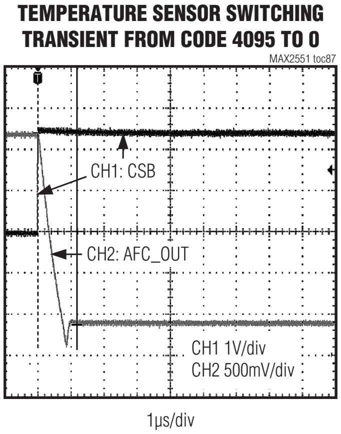
(MAX2551 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Tables 20 and 21, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

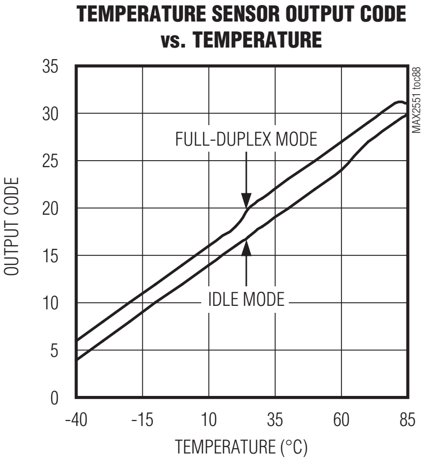




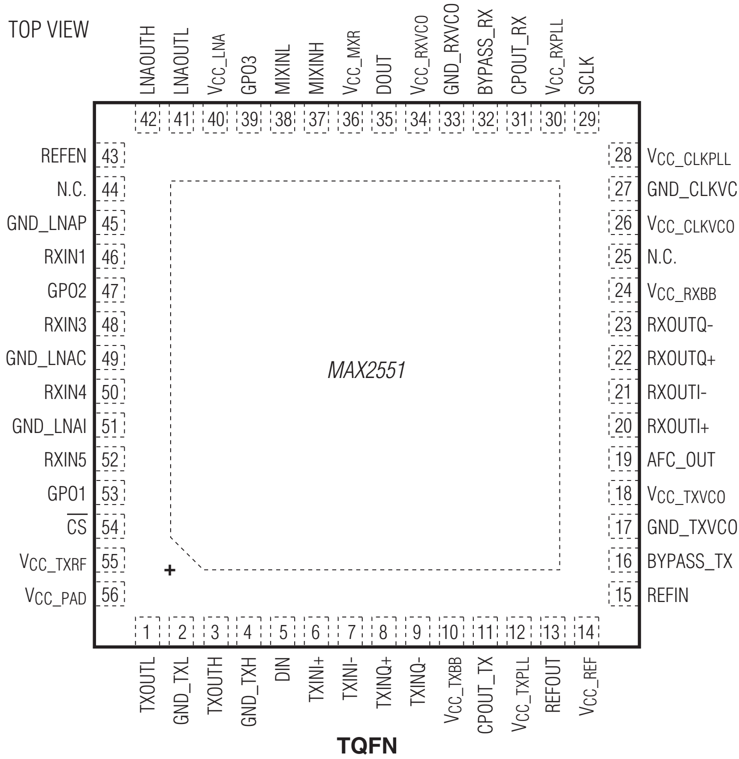








Pin Configuration


TOP VIEW
LNAOUTH 42
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V_{CC_LNA} 40
GPO3 39
MIXINL 38
MIXINH 37
V_{CC_MXR} 36
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V_{CC_RXVCO} 34
GND_RXVCO 33
BYPASS_RX 32
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V_{CC_RXPLL} 30
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REFEN 43
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GND_LNAP 45
RXIN1 46
GPO2 47
RXIN3 48
GND_LNAC 49
RXIN4 50
GND_LNAI 51
RXIN5 52
GPO1 53
$\overline{CS}$ 54
V_{CC_TXRF} 55
V_{CC_PAD} 56
28 V_{CC_CLKPLL}
27 GND_CLKVCO
26 V_{CC_CLKVCO}
25 N.C.
24 V_{CC_RXBB}
23 RXOUTQ-
22 RXOUTQ+
21 RXOUTI-
20 RXOUTI+
19 AFC_OUT
18 V_{CC_TXVCO}
17 GND_TXVCO
16 BYPASS_TX
15 REFIN
MAX2551
+
1 TXOUTL
2 GND_TXL
3 TXOUTH
4 GND_TXH
5 DIN
6 TXINI+
7 TXINI-
8 TXINQ+
9 TXINQ-
10 V_{CC_TXBB}
11 CPOUT_TX
12 V_{CC_TXPLL}
13 REFOUT
14 V_{CC_REF}
TQFN

Pin Description

PIN	NAME	FUNCTION
1	TXOUTL	Low-Band TXRF Output. Internally matched to 50Ω over the band of operation.
2	GND_TXL	Tx Ground. Connect directly to ground plane.
3	TXOUTH	High-Band TXRF Output. Internally matched to 50Ω over the band of operation.
4	GND_TXH	High-Band Tx Output Ground. Connect directly to ground plane.
5	DIN	Data Input of the 4-Wire Serial Interface
6	TXINI+	Transmitter Noninverting In-Phase Input. Accepts baseband sigma-delta modulated digital bit streams. Connect directly to the baseband processor.
7	TXINI-	Transmitter Inverting In-Phase Input. Accepts baseband sigma-delta modulated digital bit streams. Connect directly to the baseband processor.

Pin Description (continued)

PIN	NAME	FUNCTION
8	TXINQ+	Transmitter Noninverting Quadrature Input. Accepts baseband sigma-delta modulated digital bit streams. Connect directly to the baseband processor.
9	TXINQ-	Transmitter Inverting Quadrature Input. Accepts baseband sigma-delta modulated digital bit streams. Connect directly to the baseband processor.
10	V_{CC_TXBB}	Baseband Tx Path Supply. Connect to a regulated supply voltage. Bypass each supply to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
11	CPOUT_TX	Charge-Pump Output for Tx Synthesizer. Also used as the tuning voltage for Tx VCO. Connect to an external loop filter.
12	V_{CC_TXPLL}	Tx Synthesizer Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
13	REFOUT	Reference Clock Buffer Output. Configurable by the REFEN pin and SPI. See the *REFOUT Functionality* section for details.
14	V_{CC_REF}	Reference Buffer Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
15	REFIN	Reference Input Pin. Connected to TCXO. Requires a DC-blocking capacitor (1nF).
16	BYPASS_TX	Tx VCO Bias Bypass. Bypass to ground with a 470nF capacitor as close as possible.to the pin.
17	GND_TXVCO	Tx VCO Ground. Connect to the PCB ground plane with a separate via.
18	V_{CC_TXVCO}	Tx VCO Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
19	AFC_OUT	AFC DAC Output. The DAC is controlled by the register TXLO_AFCDAC (Table 43).
20	RXOUTI+	Receiver Noninverting In-Phase Output. Digital sigma-delta modulated LVDS output. Connect directly to the baseband processor.
21	RXOUTI-	Receiver Inverting In-Phase Output. Digital sigma-delta modulated LVDS output. Connect directly to the baseband processor.
22	RXOUTQ+	Receiver Noninverting Quadrature Output. Digital sigma-delta modulated LVDS output. Connect directly to the baseband processor.
23	RXOUTQ-	Receiver Inverting Quadrature Output. Digital sigma-delta modulated LVDS output. Connect directly to the baseband processor.
24	V_{CC_RXBB}	Baseband Rx Path Supply. Regulated Power-Supply Input. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
25, 44	N.C.	Leave Unconnected
26	V_{CC_CLKVCO}	Clock Generation VCO Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.

Pin Description (continued)

PIN	NAME	FUNCTION
27	GND_CLKVCO	Clock Generation Synthesizer Ground. Connect clock generation synthesizer ground to the PCB ground plane with a separate via.
28	V_{CC_CLKPLL}	Clock Generation Synthesizer Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
29	SCLK	SPI Interface Clock Input. Data is clocked in to the serial data input on the rising edge of SCLK. See Figure 4 for details.
30	V_{CC_RXPLL}	Rx Synthesizer Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
31	CPOUT_RX	Rx Synthesizer Charge Pump Output. Also used as the tuning voltage for Rx VCO. Connect to an external loop filter.
32	BYPASS_RX	Rx VCO Bias Bypass. Bypass to ground with a 470nF capacitor as close as possible to the pin.
33	GND_RXVCO	Rx VCO Ground. Connect ground to the PCB ground plane with a separate via.
34	V_{CC_RXVCO}	Rx VCO Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
35	DOUT	SPI Data Output
36	V_{CC_MXR}	Rx Mixer Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
37	MIXINH	High-Band Rx Mixer Input. RF input to mixer from an external filter (optional). Internally DC-blocked and matched to 50Ω.
38	MININL	Low-Band Rx Mixer Input. RF input to mixer from an external filter (optional). Internally DC-blocked and matched to 50Ω.
39	GPO3	General-Purpose Output. Controlled by register 7 (Table 20). GPO3 can also be configure as a PLL lock-detect output.
40	V_{CC_LNA}	LNA Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
41	LNAOUTL	Low-Band LNA Output. RF output from LNA 3 to external SAW filter. Internally DC-blocked and matched to 50Ω.
42	LNAOUTH	High-Band LNA Output. RF Output from LNA 1 to an external SAW filter. Internally DC-blocked and matched to 50Ω.
43	REFEN	Configuration for REFOUT. When REFEN = 0, REFOUT can be configured for CMOS or low-voltage output by the SPI interface (see the *REFOUT Functionality* section). When REFEN = 1, REFOUT is configured as REFIN buffer with CMOS output.
45	GND_LNAP	PCS LNA Ground. Connect directly to ground plane.
46	RXIN1	Low-Noise Amplifier Input 1. Requires AC-coupling and external matching.
47	GPO2	General-Purpose Output. Controlled by register 7<3:2>.

Pin Description (continued)

PIN	NAME	FUNCTION
48	RXIN3	Low-Noise Amplifier Input 3. Requires AC-coupling and external matching.
49	GND_LNAC	Ground for Cellular LNA. Connect directly to the ground plane.
50	RXIN4	Low-Noise Amplifier Input 4. Requires AC-coupling and external matching.
51	GND_LNAI	IMT LNA Ground. Connect directly to the ground plane.
52	RXIN5	Low-Noise Amplifier Input 5. Requires AC-coupling and external matching.
53	GPO1	General-Purpose Output. Controlled by register 23<25:24>.
54	$\overline{\text{CS}}$	Serial-Interface Chip Select. See Figure 4.
55	V_{CC_TXRF}	Tx Upconverter Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
56	V_{CC_PAD}	PA Driver Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
—	EP	Exposed Pad. Connect to a large ground plane to maximize thermal performance.

Detailed Description

Quad RF Inputs

The MAX2551 features four independent RF inputs. RXIN1 and RXIN3 are used for receiving WCDMA Band II/Band V. Band II and Band V WCDMA/PCS downlink can be monitored (network listen) by programming the part to receive through the RXIN4 and RXIN5 inputs. This allows the base station to monitor surrounding cells to select the best operating conditions (transmit power, codes, frequency, capacity, etc.)

REFOUT Functionality

The MAX2551 features a reference oscillator buffered output that is configurable by the REFEN input and Register 29. REFOUT can be configured as CMOS or as a low-voltage output. Table 2 lists all REFOUT configurations.

Receiver System Gain Control

The device features programmable-gain LNAs and programmable variable-gain baseband amplifiers, allowing the system gain to be entirely controlled by the serial interface. RX1, RX3, and RX5 have three possible gain states: high gain, medium gain, and low gain. RX4 has high and low gain modes. The gain state of the LNA in operation is programmed by the LNAGAIN bits in the RX_GAIN[15:14] register. Each LNA requires an external matching network to optimize system sensitivity. Table 3 provides S11 for each LNA input over the specified band of operation, Table 4 provides S11 of RXIN1 and RXIN3 LNA output, and Table 5 provides S11 of the mixer input. The receiver also features a separate dedicated receive path for the 1930MHz to 1995MHz band that enables monitoring.

The baseband amplifiers has 16 possible gain states with each LSB providing a gain step of 3dB. The gain state of the baseband amplifiers is programmed by the PGAGAIN bits in the RX_GAIN[11:8] register. The dynamic range of the data converters when using the recommended sampling rates is sufficient to allow for minimal switching of system gain over varying input signal power. Table 6 and Table 7 provide suggested LNA and PGA settings for various input signal power ranges. Two possible LNA/PGA gain settings are provided for the uplink band. Case 1 (Table 6) allows for 3GPP TS25.104 compliance under all conditions while case 2 (Table 7) allows best sensitivity but compromises adjacent channel selectivity and intermodulation in high-gain LNA mode.

Table 1. RF Input/Output Frequency Range

PIN	FUNCTION	FREQUENCY RANGE (MHz)
RXIN1	Band II WCDMA uplink Rx	1850 to 1915
RXIN3	Band V WCDMA uplink Rx	820 to 849
RXIN4	Band V WCDMA/GMSK monitor	865 to 894
RXIN5	Band II WCDMA/PCS monitor	1930 to 1995
TXOUTL	Band V WCDMA downlink Tx	865 to 894
TXOUTH	Band II WCDMA downlink Tx	1930 to 1995

Table 2. REFOUT Output Configurations

INPUT			OUTPUT
REFEN INPUT	REFIN_ENOUT3 (TXLO_REF<14>)	REFOUT_LV_CMOS_SEL (TXLO_REF<23>)	OUTPUT TYPE
0	0	X	Off
	1	0	CMOS
		1	Low Voltage
1	X	X	CMOS

Table 3. Typical RXIN1 (High Gain) S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	REAL	IMAGINARY
1810.0	35.4	-43.8
1815.0	35.5	-43.7
1820.0	35.6	-43.7
1825.0	35.6	-43.7
1830.0	35.7	-43.6
1835.0	35.8	-43.6
1840.0	35.9	-43.6
1845.0	36.0	-43.6
1850.0	36.1	-43.6
1855.0	36.1	-43.5
1860.0	36.2	-43.5
1865.0	36.3	-43.5
1870.0	36.4	-43.5
1875.0	36.4	-43.5
1880.0	36.5	-43.5
1885.0	36.6	-43.5
1890.0	36.6	-43.5
1895.0	36.7	-43.6
1900.0	36.7	-43.6
1905.0	36.8	-43.6
1910.0	36.9	-43.6
1915.0	36.9	-43.6
1920.0	37.0	-43.6
1925.0	37.0	-43.7
1930.0	37.0	-43.7
1935.0	37.1	-43.7
1940.0	37.1	-43.7
1945.0	37.2	-43.8
1950.0	37.2	-43.8
1955.0	37.2	-43.9

Table 4. Typical RXIN3 (High Gain) S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	REAL	IMAGINARY
795.0	38.2	-34.2
800.0	38.6	-33.8
805.0	39.0	-33.4
810.0	39.5	-33.1
815.0	39.9	-32.7
820.0	40.3	-32.4
825.0	40.8	-32.0
830.0	41.2	-31.7
835.0	41.6	-31.4
840.0	42.0	-31.2
845.0	42.5	-30.9
850.0	42.9	-30.6
855.0	43.3	-30.4
860.0	43.7	-30.2
865.0	44.2	-29.9
870.0	44.6	-29.7

Table 5. Typical RXIN4 (High Gain) S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	REAL	IMAGINARY
840.0	24.0	-57.8
845.0	24.5	-57.6
850.0	24.9	-57.4
855.0	25.3	-57.3
860.0	25.7	-57.2
865.0	26.1	-57.1
870.0	26.3	-57.0
875.0	26.6	-57.0
880.0	26.8	-56.9
885.0	26.9	-56.9
890.0	27.0	-56.8
895.0	27.1	-56.8
900.0	27.1	-56.7
905.0	27.1	-56.7
910.0	27.1	-56.6
915.0	27.0	-56.5

Table 6. Typical RXIN5 (High Gain) S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	REAL	IMAGINARY
1890.0	17.4	-35.7
1895.0	17.4	-35.5
1900.0	17.4	-35.3
1905.0	17.5	-35.1
1910.0	17.5	-34.9
1915.0	17.5	-34.7
1920.0	17.6	-34.5
1925.0	17.6	-34.3
1930.0	17.7	-34.1
1935.0	17.7	-33.9
1940.0	17.7	-33.7
1945.0	17.8	-33.5
1950.0	17.8	-33.3
1955.0	17.9	-33.1
1960.0	17.9	-32.9
1965.0	18.0	-32.7
1970.0	18.0	-32.5
1975.0	18.1	-32.3
1980.0	18.1	-32.1
1985.0	18.2	-31.9
1990.0	18.2	-31.8
1995.0	18.3	-31.6
2000.0	18.3	-31.4
2005.0	18.4	-31.2
2010.0	18.5	-31.0
2015.0	18.5	-30.8
2020.0	18.6	-30.6
2025.0	18.7	-30.4
2030.0	18.7	-30.2
2035.0	18.8	-30.0

Table 7. Typical LNAOUTH (High Gain) S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	REAL	IMAGINARY
1810.0	27.9	1.3
1815.0	28.1	1.8
1820.0	28.4	2.3
1825.0	28.7	2.8
1830.0	29.0	3.2
1835.0	29.3	3.7
1840.0	29.6	4.2
1845.0	29.9	4.7
1850.0	30.2	5.2
1855.0	30.5	5.7
1860.0	30.8	6.2
1865.0	31.1	6.6
1870.0	31.5	7.1
1875.0	31.8	7.6
1880.0	32.1	8.1
1885.0	32.5	8.6
1890.0	32.8	9.1
1895.0	33.1	9.6
1900.0	33.5	10.1
1905.0	33.9	10.6
1910.0	34.2	11.1
1915.0	34.6	11.5
1920.0	35.0	12.0
1925.0	35.4	12.5
1930.0	35.7	13.0
1935.0	36.1	13.5
1940.0	36.5	14.0
1945.0	36.9	14.5
1950.0	37.3	15.0
1955.0	37.8	15.5

Digital I/Q Receive Interface

The baseband output of the MAX2551 is in the form of a digital I/Q interface. The received signals are sampled by a 1-bit sigma-delta modulator clocked at 153.6MHz for WCDMA and 26MHz for GSMK. The digital bitstream out of the converter is transported from the MAX2551 to the baseband processor by a low-voltage differential signaling (LVDS) interface. The output data is single-bit nonreturn-to-zero (NRZ). The MAX2551 does not perform any encoding of the data and no clock is exchanged between the MAX2551 and the baseband processor.

The MAX2551 performs limited analog filtering only to minimize aliasing; all channel filtering is realized entirely in the digital domain. The digital filtering removes undesired signals as well as the inherent quantization noise of the sigma-delta modulator. In addition, the MAX2551's analog filters include a pole at approximately half the channel bandwdith that must be equalized by the digital filters.

The differential outputs require a termination resistor at the digital baseband IC inputs. The output current of the LVDS drivers are programmable by the LVDSI_2X bit in the BB_CLKOUT register to accommodate different termination resistors. Set LVDSI_2X = 1 to set the drive current to nominal for operation with 120Ω differential loads.

Digital I/Q Transmit Interface

The Tx baseband input of the MAX2551 is in the form of a sigma-delta modulated digital I/Q interface. The digital bitstream of the baseband processor is transported to the MAX2551 by a low-voltage differential signaling (LVDS) or DDR3 interface. The LVDS signal has a typical common-mode voltage of 1.2V and a differential swing of $140mV_{P-P}$, while DDR3 has a common-mode voltage of 0.75V and differential of $600mV_{P-P}$. For LVDS, the input data should be in single-bit NRZ format; no clock is exchanged between the baseband processor and the MAX2551. The MAX2551 recovers the I/Q bitstreams with an on-chip data recovery circuit. The bitstream is converted to an analog signal and filtered prior to upconversion to an RF signal.

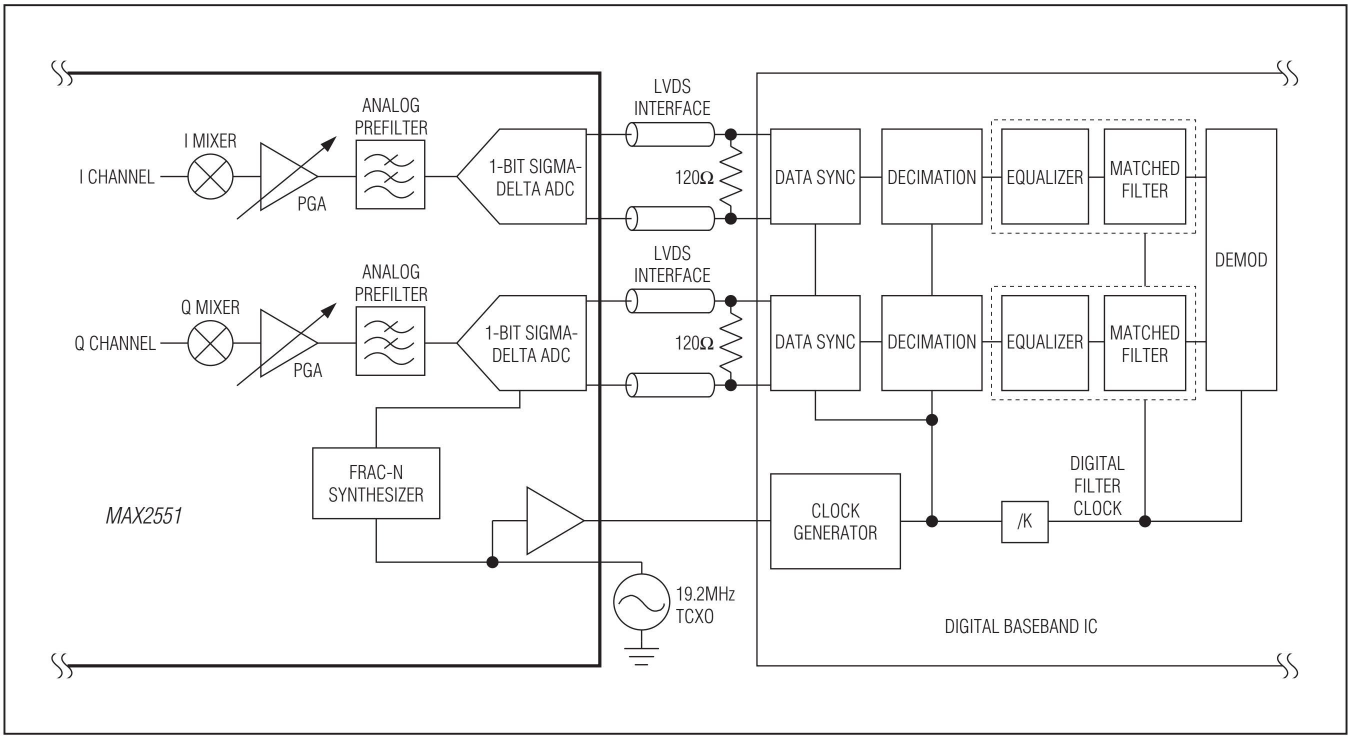
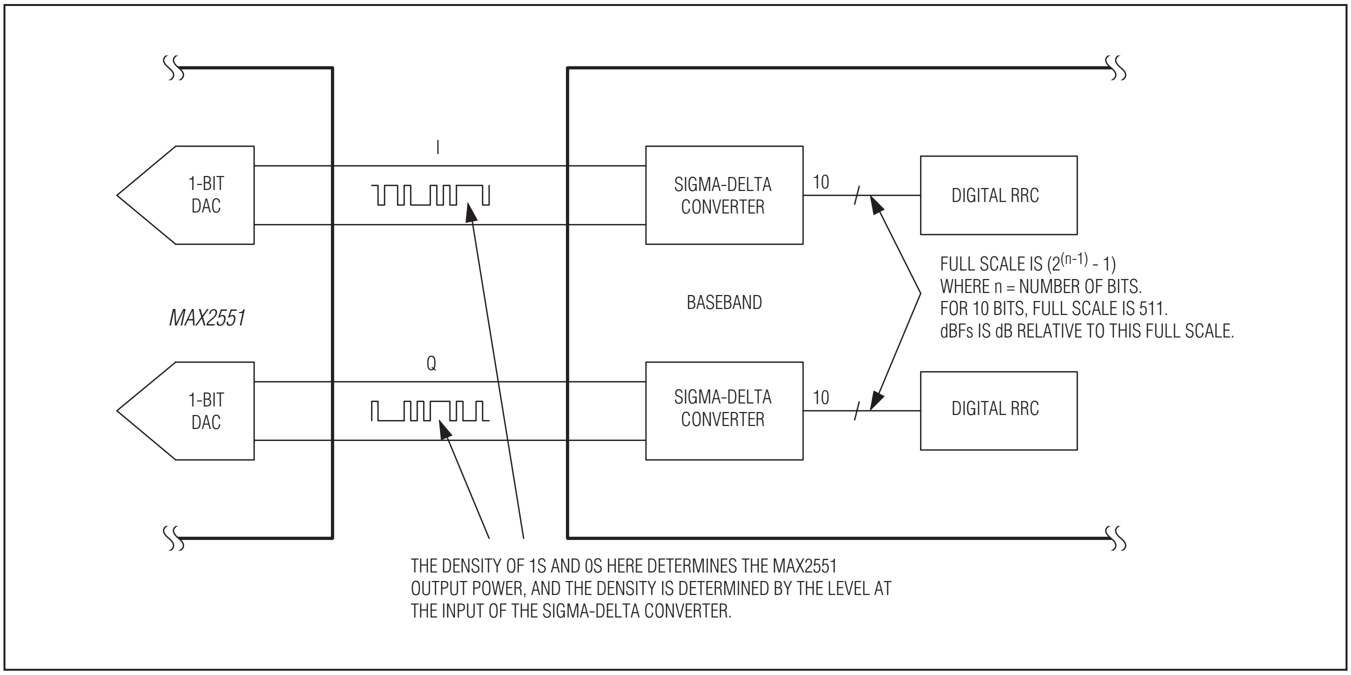

LVDS INTERFACE
ANALOG PREFILTER
I MIXER
I CHANNEL
PGA
1-BIT SIGMA-DELTA ADC
120Ω
DATA SYNC
DECIMATION
EQUALIZER
MATCHED FILTER
DEMOD
LVDS INTERFACE
ANALOG PREFILTER
Q MIXER
Q CHANNEL
PGA
1-BIT SIGMA-DELTA ADC
120Ω
DATA SYNC
DECIMATION
EQUALIZER
MATCHED FILTER
FRAC-N SYNTHESIZER
MAX2551
DIGITAL FILTER CLOCK
CLOCK GENERATOR
/K
19.2MHz TCXO
DIGITAL BASEBAND IC

Figure 1. Digital Baseband Receiver Interface


I
1-BIT DAC
SIGMA-DELTA CONVERTER
10
DIGITAL RRC
MAX2551
BASEBAND
Q
1-BIT DAC
SIGMA-DELTA CONVERTER
10
DIGITAL RRC

FULL SCALE IS $(2^{(n-1)} - 1)$
WHERE n = NUMBER OF BITS.
FOR 10 BITS, FULL SCALE IS 511.
dBFs IS dB RELATIVE TO THIS FULL SCALE.

THE DENSITY OF 1S AND 0S HERE DETERMINES THE MAX2551 OUTPUT POWER, AND THE DENSITY IS DETERMINED BY THE LEVEL AT THE INPUT OF THE SIGMA-DELTA CONVERTER.

Figure 2. Baseband Input Example

Baseband Input Level

The MAX2551 baseband input is in digital 1-bit sigma-delta converted format. There are internal 1-bit I/Q DACs that restore the level of the incoming digital signals to a repeatable analog level in the MAX2551. At a given TX_GAIN value, the RMS output power level depends on the density of the bit stream, not the voltage level of the LVDS digital signal. The density of the bit stream, in turn, depends on the input level of the sigma-delta converter, which resides in the baseband chip. The condition for the AC performance in the EC table calls for -4dBFs peak, which means -4dB relative to the full scale of the input of the sigma-delta converter. The sigma-delta converter, coded in Verilog, and implemented on FPGA has 10 bits (9 bits + sign) at the input. In this case, the full scale is ±511, and -4dBFs peak means ±322 peak excursion. The RMS level is lower than this number, depending on the peak-average ratio of the signal. For TM1, the peak-average is 10.6dB at 0.01%, so the RMS level of the baseband signal is -14.6dBFs, or ±95.

DC Offset

While the inherent DC offset at the I/Q outputs is very low, it is expected that the baseband processor will digitally remove any DC offset.

Digital Filters/Sigma Delta Modulator

Verilog code is available for implementation of the sigma-delta modulator and digital filters in the baseband processor. Contact the factory for further information.

Fractional-N Synthesizers

The MAX2551 includes three fractional-N frequency synthesizers. One synthesizer is used to generate the receive RF local oscillator (LO), the second is used to generate the transmit RF local oscillator, while the third is used to generate the ADC sampling clock. The loop filter for the ADC sampling clock synthesizer is integrated on-chip. RF synthesizers require an external loop filter. All synthesizers have 20 bits of fractional resolution.

RF Synthesizers

For the receiver the RF LO frequency is programmed by the RXLO_FRAC [19:0] (Fractional) register and the RXLO_SYN[7:0] (Integer) register. The synthesizer frequency is demonstrated by the following example.

Assume:

$$f_{REFIN} = f_{COMPARISON} = 19.2\text{MHz}$$

$$f_{LO} = f_{REFIN} \times \left(\text{RXLO\_SYN} + \frac{\text{RXLO\_FRAC}}{2^{20}}\right) \times K$$

where:

K = 1 if RXIN1, RXIN3, RXIN5

K = 0.5 if RXIN4

For the transmitter the RF LO frequency is programmed by the TXLO_FRAC [19:0] (Fractional) register and the TXLO_SYN[7:0] (Integer) register. The synthesizer frequency is demonstrated by the following example.

Assume:

$$f_{REFIN} = f_{COMPARISON} = 19.2\text{MHz}$$

$$f_{LO} = f_{REFIN} \times \left(\text{TXLO\_SYN} + \frac{\text{TXLO\_FRAC}}{2^{20}}\right) \times K$$

where:

K = 0.5 for TXOUTL

K = 1 for TXOUTH

Calculate the required divider ratio by dividing the LO frequency by the reference frequency.

$$\text{Divider} = \frac{f_{LO} \times 2}{f_{COMPARISON}} = \frac{1910\text{MHz}}{19.2\text{MHz}} = 99.479166$$

The integer-N divider is equal to the integer portion of the divider ratio, 99 in this example. Convert the integer-N decimal value to binary and program into the RXLO_SYN bits.

Integer-N Divider = 99 = 0x63 = 0110 0011 → RXLO_SYN = 0110 0011

The fractional-N divider is equal to the fractional portion of the divider ration, 0.479166 in this example. Convert the fractional portion of the divider to a 20-bit word by multiplying by 2^{20} and rounding to the nearest whole number. Then, convert the result to binary and program the bits into the RXLO_FRAC.

Fractional-N Divider = 0.479166 x 2^{20} = 502442 = 0x7AAAA → RXLO_FRAC = 0x7AAAA

ADC Clock Synthesizer

The sampling clock frequency is controlled by the CINT (BBCLK_SYN[7:0]) and CFRAC (BBCLK_FRAC[19:0]) registers. The sampling clock synthesizer does not need to be repeatedly programmed during normal operation. The sampling clock frequency (f_{ADCCLK})is 153.6MHz in WCDMA mode and 26MHz in GSM mode. The dynamic range of the converters with this sampling frequency is sufficient to meet all system specifications with very minimal control of the PGA.

Assume:

$$f_{REFIN} = f_{COMPARISON} = 19.2\text{MHz}$$

ADC Clock Synthesizer Fractional Frequency Correction

The MAX2551 ADC clock synthesizer uses a 20-bit frequency synthesizer and can be enhanced by a fractional error correction. Parameters PBYQ_RATUP and PBYQ_RATDN implement the following function.

$$\text{Fadcclk} = f_{REFIN} \times (\text{CINT} + (\text{CFRAC} + \text{PBYQ\_RATUP}/(\text{PBYQ\_RATUP} + \text{PBYQ\_RATDN}))/2^{20}) \times K$$

$$\text{PBYQ\_RATUP}/(\text{PBYQ\_RATUP} + \text{PBYQ\_RATDN}) = (f_{ADCCLK}/f_{REFIN} - \text{CINT}) \times 2^{20} \times K - \text{CFRAC}$$

where:

K = 8 if WCDMA

K = 48 if GSM/PCS/DCS

PBYQ_RATUP and PBYQ_RATDN should be chosen for the best fit.

This feature can be enabled or disabled through EN_PBYQDIV (REG15<22>). Table 8 shows the PBYQ_RATUP and PBYQ_RATDN with commonly used crystal oscillator frequencies.

Power-Down Modes

The MAX2551 features multiple power-down modes that can be controlled by hardware or software. Table 9 describes the various power-down modes.

Table 8. Typical LNAOUTL (High Gain) S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	REAL	IMAGINARY
795.0	40.1	-4.0
800.0	40.8	-3.3
805.0	41.6	-2.6
810.0	42.3	-1.9
815.0	43.1	-1.2
820.0	43.9	-0.6
825.0	44.7	0.1
830.0	45.5	0.7
835.0	46.4	1.3
840.0	47.2	1.9
845.0	48.1	2.5
850.0	49.0	3.1
855.0	49.9	3.7
860.0	50.8	4.2
865.0	51.7	4.8
870.0	52.6	5.3

Carrier and Sideband Suppression Optimization

The MAX2551 delivers a typical carrier suppression of -40dBc and a sideband suppression of -45dBc without any external calibration; however, if greater suppression is required, the MAX2551 is capable of overriding the factory settings and accepting manual calibration from the baseband processor.

RF Band Configuration

The MAX2551 has configurable VCO and LO generation to support BC0 and BC1 forward and reverse link operation. In transmit signal path, LC tank is also configurable to optimize performance in both bands. Table 10 shows the key difference in SPI settings.

General-Purpose Outputs

The MAX2551 is equipped with three general-purpose outputs. GPO3 can also be configured as a PLL lock detect for the Rx, Tx or Rx and Tx. See Table 20 for how to properly configure the general-purpose outputs.

Table 9. Typical MIXINH S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	REAL	IMAGINARY
1810.0	30.3	-37.1
1815.0	30.5	-37.2
1820.0	30.7	-37.2
1825.0	30.9	-37.3
1830.0	31.1	-37.5
1835.0	31.3	-37.6
1840.0	31.5	-37.7
1845.0	31.7	-37.8
1850.0	31.9	-37.9
1855.0	32.0	-38.1
1860.0	32.2	-38.2
1865.0	32.3	-38.4
1870.0	32.4	-38.5
1875.0	32.6	-38.7
1880.0	32.7	-38.8
1885.0	32.8	-39.0
1890.0	32.9	-39.1
1895.0	33.0	-39.3
1900.0	33.1	-39.5
1905.0	33.1	-39.6
1910.0	33.2	-39.8
1915.0	33.2	-40.0
1920.0	33.3	-40.1
1925.0	33.3	-40.3
1930.0	33.3	-40.5
1935.0	33.4	-40.6
1940.0	33.4	-40.8
1945.0	33.4	-40.9
1950.0	33.4	-41.1
1955.0	33.3	-41.3

Table 10. Typical MIXINL S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	REAL	IMAGINARY
795.0	43.5	-24.0
800.0	45.1	-23.5
805.0	46.8	-23.1
810.0	48.5	-22.8
815.0	50.3	-22.6
820.0	52.1	-22.5
825.0	54.0	-22.5
830.0	55.9	-22.6
835.0	57.9	-22.8
840.0	59.9	-23.2
845.0	61.8	-23.7
850.0	63.8	-24.4
855.0	65.8	-25.2
860.0	67.8	-26.2
865.0	69.7	-27.3
870.0	71.6	-28.6

Power-On Reset (POR)

Recommended defaults are not guaranteed upon power-up and are provided for reference only. All registers must be written with the proper values no earlier than 100µs after power-up. Figure 3 displays the time it takes for Tx/Rx PLL lock detect (GPO3) to become active after power-up and enabling the correct registers for proper operation. All reserved registers should only be written with default values.

Temperature Sensor

An on-chip temperature sensor is enabled by programming RX_ENABLE<14> = 1. To trigger temperature sensor ADC reading, program RX_MISC2<6> from 0 to 1. The ADC acquires the 5-bit logic output in 2µs; the temperature sensor needs to be on (RX_ENABLE<14> = 1) to maintain the ADC logic output. To read the 5-bit logic output through the DOUT pin, apply 4-wire SPI readout programming sequence to RX_MISC2<11:7>.

4-Wire Serial Interface

The MAX2551 includes 32 programmable 26-bit registers. The most significant bit (MSB) is the read/write selection bit (R/W in Figure 4). The next 5 bits are register address (A[4:0] in Figure 4). The 26 least significant bits (LSBs) are register data (D[25:0] in Figure 4). Register data is loaded through the 4-wire SPI/MICROWIRE™-compatible serial interface. MSB of data at the DIN pin is shifted in first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, input data is shifted at the rising edge of the clock at the SCLK pin. At $\overline{CS}$ rising edge, the 26-bit data bits are latched into the register selected by the address bits. See Figure 4. There is no power-on SPI register self-reset functionality in the MAX2551; the user must program all register values after power-up. During the read mode, register data selected by address bits is shifted out to the DOUT pin at the falling edges of the clock.

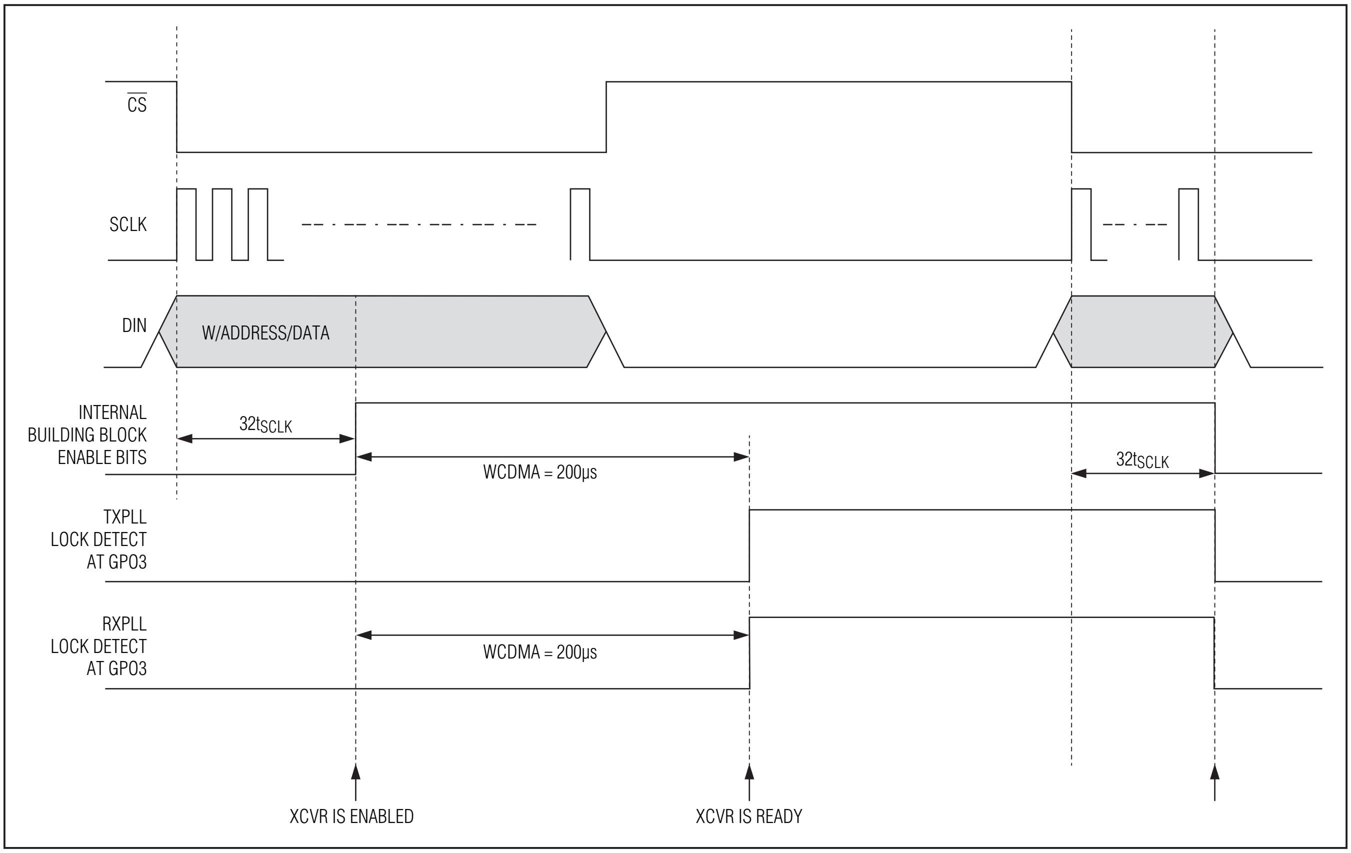


Figure 3. POR PLL Lock-Detect Time

MICROWIRE is a trademark of National Semiconductor Corp.

Table 11. Typical TXOUTL S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	REAL	IMAGINARY
700.0	25.5	63.9
750.0	52.3	76.8
800.0	103.7	59.2
850.0	107.4	-9.9
900.0	64.8	-32.6
950.0	39.6	-27.2
1000.0	27.2	-18.9
1050.0	20.7	-11.8
1100.0	16.9	-6.1
1150.0	14.5	-1.3
1200.0	12.9	2.7
1250.0	11.8	6.3
1300.0	11.1	9.4
1350.0	10.5	12.3
1400.0	10.1	15.0
1450.0	9.9	17.6
1500.0	9.7	20.1
1550.0	9.6	22.5
1600.0	9.6	24.8
1650.0	9.6	27.1
1700.0	9.7	29.4
1750.0	9.8	31.6
1800.0	10.0	33.9
1850.0	10.2	36.2
1900.0	10.4	38.6
1950.0	10.7	41.0
2000.0	11.0	43.5
2050.0	11.3	46.0
2100.0	11.7	48.6
2150.0	12.2	51.4
2200.0	12.7	54.2

Table 12. Typical TXOUTH S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	REAL	IMAGINARY
700.0	3.7	21.9
750.0	3.9	23.9
800.0	4.2	26.0
850.0	4.5	28.2
900.0	4.8	30.5
950.0	5.2	33.1
1000.0	5.8	35.8
1050.0	6.4	38.9
1100.0	7.2	42.2
1150.0	8.3	45.8
1200.0	9.7	50.0
1250.0	11.5	54.6
1300.0	14.0	60.0
1350.0	17.5	66.1
1400.0	22.5	73.2
1450.0	29.9	81.2
1500.0	41.1	89.9
1550.0	58.2	98.0
1600.0	83.9	101.3
1650.0	117.3	91.2
1700.0	146.2	58.0
1750.0	149.1	10.8
1800.0	126.3	-24.1
1850.0	97.4	-38.3
1900.0	74.0	-39.5
1950.0	57.4	-35.4
2000.0	45.8	-29.5
2050.0	37.8	-23.5
2100.0	32.0	-17.8
2150.0	27.8	-12.6
2200.0	24.7	-7.8

Table 13. LNA and PGA Gain Settings for 1850MHz to 1915MHz Uplink Band (Case 1: Use LNA Mid and Low Gain)

	ESTIMATED INPUT POWER AT LNA INPUT, P_{IN}				
	< -92dBm	**> -92dBm**	**> -85dBm**	**> -67dBm**	**> -42dBm**
LNA Gain Register Setting	Medium	Medium	Medium	Low	Low
PGA Gain Register Setting	9	8	6	6	0
Estimated Sensitivity (dBm)	-118	-113	-110	-97	-83
Estimated Maximum Wanted Modulated Signal (dBm)	-43	-36	-31	-20	-6

Table 14. Suggested LNA and PGA Gain Settings for 1850MHz to 1915MHz Uplink Band (Case 2: Use LNA in All Three Modes)

	ESTIMATED INPUT POWER AT LNA INPUT, P_{IN}				
	< -92dBm	**> -92dBm**	**> -85dBm**	**> -67dBm**	**> -42dBm**
LNA Gain Register Setting	High	Medium	Medium	Low	Low
PGA Gain Register Setting	6	8	6	6	0
Estimated Sensitivity (dBm)	-121	-113	-110	-97	-83
Estimated Maximum Wanted Modulated Signal (dBm)	-44	-36	-31	-20	-6

Table 15. PBYQ_RATUP and PBYQ_RATDN Commonly Used Crystal Oscillator Frequencies

STANDARD	f_{REFIN} (MHz)	CINT REG15 <7:0>	CFRAC REG1 <19:0>	PBYQ_RATUP REG16 <7:0>	PBYQ_RATDN REG16 <15:8>	CINT REG15 <7:0>	CFRAC REG14 <19:0>	PBYQ_RATUP REG16<7:0>	PBYQ_RATDN REG16<15:8>
	Reference Frequency	Integer Divide Ratio (dec)	Fractional Divide Ratio (dec)	Fractional LSB Dither Up (dec)	Fractional LSB Dither Down (dec)	Integer Divide Ratio (hex)	Fractional Divide Ratio (hex)	Fractional LSB Dither Up (hex)	Fractional LSB Dither Down (hex)
WCDMA	13	94	548485	59	6	5E	85E85	3B	6
	15.36	80	0	0	0	50	0	0	0
	19.2	64	0	0	0	40	0	0	0
	20	61	461373	11	14	3D	70A3D	B	E
	26	47	274242	62	3	2F	42F42	3E	3
GSM	13	96	0	0	0	60	0	0	0
	15.36	81	262144	0	0	51	40000	0	0
	19.2	65	0	0	0	41	0	0	0
	20	62	419430	2	3	3E	66666	2	3
	26	48	0	0	0	30	0	0	0

Table 16. Power-Down Modes

OPERATING MODE	REFEN PIN, REG29<14:12>	BLOCKS ENABLE REG00<18:0>	BIAS ENABLE REG20<24>	AFCDAC ENABLE REG30<19>	CDR DIVIDER ENABLE REG16<20>	CDR ENABLE REG24<18>
Sleep	0000	00000	0	0	0	0
AFC Only	0000	00000	0	1	0	0
Reference Buffer Only	1xxx or 0100	00000	0	1	0	0
Idle RX	1xxx or 0x11	00840	1	1	0	0
Idle TX	1xxx or 0x11	01000	1	1	1	1
RXIN1/TXOUTH Full Duplex	1xxx or 0x11	79BFF	1	1	1	1
RXIN1 Only	1xxx or 0x11	009FF	1	1	0	0
RXIN3/TXOUTL Full Duplex	1xxx or 0x11	79BFF	1	1	1	1
RXIN3 Only	1xxx or 0x11	009FF	1	1	0	0
RXIN4 Monitor	1xxx or 0x11	009FF	1	1	0	0
RXIN5 Monitor	1xxx or 0x11	009FF	1	1	0	0
TXOUTL Only	1xxx or 0x11	79240	1	1	1	1
TXOUTH Only	1xxx or 0x11	79240	1	1	1	1

Table 17. RF Band Configuration

INPUT PIN	RF RANGE (MHz)	VCO SELECT REG03<20:19>	VCO ROH BAND REG03<22:21>	VCO DIVIDER REG03<18:17>	LNA/MIXER SELECT REG01<5:0>	RXIN4_HB REG06<16>
RXIN1	1850 to 1915	10	01	10	18	X
RXIN3	820 to 849	01	XX	01	01	X
RXIN4	865 to 894	01	XX	01	15	0
RXIN5	1930 to 1995	10	00	10	2A	X

OUTPUT PIN	RF RANGE (MHz)	VCO SELECT REG28 <15:14>	VCO ROH BAND REG28 <17:16>	VCO DIVIDER REG28 <13:12>	PAD_ BAND REG19 <1:0>	PAD_ CTUNE REG19 <6:2>	TXLO_ IQ_GAIN REG20 <19>	UCX_ CSW REG21 <5:2>	T_UCX_ RSW REG22 <20:17>	T_UCX_ BAND_SEL REG22 <23:22>
TX_OUTL	865 to 894	01	XX	01	00	00100	1	1101	XXXX	01
TX_OUTH	1930 to 1995	10	00	10	11	00000	0	0000	0100	11

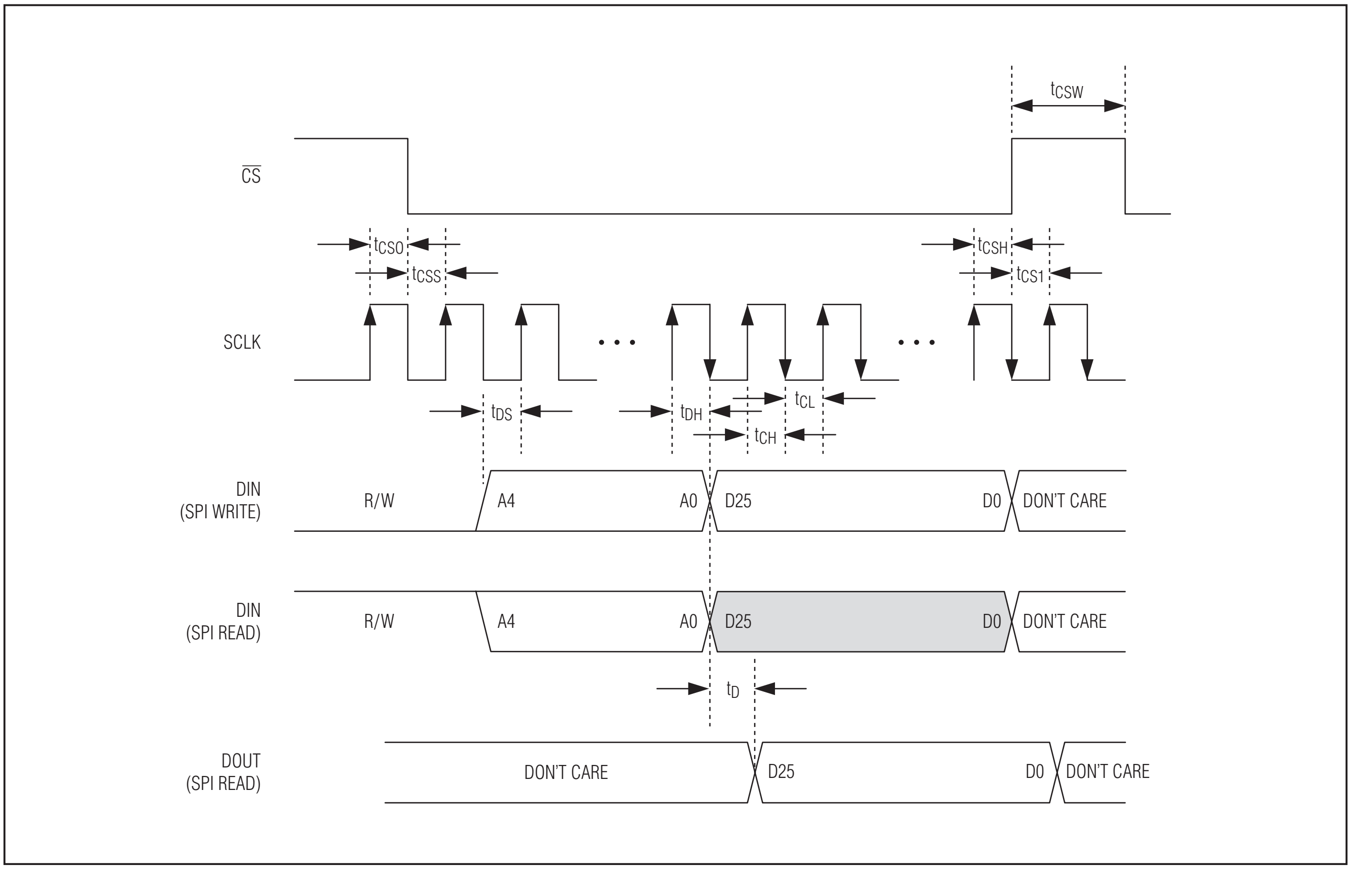

t_{CSW}
$\overline{CS}$
t_{CSO}
t_{CSS}
t_{CSH}
t_{CS1}
SCLK
t_{DS}
t_{DH}
t_{CL}
t_{CH}
DIN (SPI WRITE)
R/W
A4
A0
D25
D0
DON'T CARE
DIN (SPI READ)
R/W
A4
A0
D25
D0
DON'T CARE
t_D
DOUT (SPI READ)
DON'T CARE
D25
D0
DON'T CARE

Figure 4. SPI Timing

Table 18. SPI Serial Interface Timing

SPEC NO.	PARAMETER	SYMBOL	TYP	UNITS
SPI1	SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time	t_{CSO}	6	ns
SPI2	Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}	6	ns
SPI3	DIN to SCLK Setup Time	t_{DS}	6	ns
SPI4	DIN to SCLK Hold Time	t_{DH}	6	ns
SPI5	SCLK Pulse-Width High	t_{CH}	6	ns
SPI6	SCLK Pulse-Width Low	t_{CL}	6	ns
SPI7	Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$	t_{CSH}	6	ns
SPI8	$\overline{CS}$ High Pulse Width	t_{CSW}	50	ns
SPI9	Time Between Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK	t_{CS1}	6	ns
SPI10	SCLK Frequency	f_{CLK}	40	MHz
SPI11	Rise Time	t_R	2.5	ns
SPI12	Fall Time	t_F	2.5	ns
SPI13	SCLK Falling Edge to Valid DOUT	t_D	12.5	ns

Register and Bit Descriptions (If Applicable)

The operating mode of the MAX2551 is completely controlled by 32 on-chip registers.

Recommended defaults are not guaranteed upon power-up and are provided for reference only. All registers must be written with the proper values no earlier than 10µs after power-up (once $V_{CC\_}$ is 90% of final value). All reserved registers should only be written with default values.

Table 19. Brief Register Map

REGISTER NO.	REGISTER NAME	ADDRESS	FUNCTION
0	RX_ENABLE	00000	Enable bits for various internal functions
1	RX_GAIN	00001	Gain control of LNA and PGA
2	Reserved	00010	—
3	RX_LNA	00011	LNA bias, Rx synthesizer configuration
4	Reserved	00100	—
5	Reserved	00101	—
6	RX_LPF	00110	RXLPF configuration
7	GPO_CONFIG	00111	Configuration of GPOs
8	Reserved	01000	—
9	Reserved	01001	—
10	RXLO_FRAC	01010	Receive synthesizer fractional division ratio
11	RXLO_SYN	01011	Configuration of Rx synthesizer
12	BBCLK_OUT	01100	ADC configuration
13	Reserved	01101	—
14	BBCLK_FRAC	01110	ADC clock generator fractional division ratio
15	BBCLK_SYN	01111	Configuration of clock generator synthesizer
16	BBCLK_MISC	10000	Dithering clock generator synthesizer
17	BBCLK_SPARE	10001	Miscellaneous setting for clock generator
18	TX_LPF	10010	LPF settings for Tx path
19	TX_PAD	10011	PA driver settings
20	TX_UPX1	10100	Tx upconverter bias
21	TX_UPX2	10101	Tx upconverter bias adjustment and V2I attenuation
22	TX_UPX3	10110	Tx upconverter DC offset adjustment
23	TX_GAIN1	10111	Tx path gain setting
24	TX_GAIN2	11000	Tx path gain curve adjustment
25	Reserved	11001	—
26	Reserved	11010	—
27	TXLO_FRAC	11011	Transmit synthesizer fractional division ratio
28	TXLO_SYN	11100	Configuration of Tx synthesizer
29	TXLO_REF	11101	Configuring REFOUT and REFIN
30	TXLO_AFCDAC	11110	AFC DAC Word
31	Reserved	11111	—

Table 20. RX_ENABLE Register 0 (Address = 00000)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	LNAEN	LNA Enable	0 = Disable, 1 = Enable	0	1	1	1	1	0	0	1	1	0	0	0	0	0
1	RXMXREN	Rx Mixer Enable	0 = Disable 1 = Enable	0	1	1	1	1	0	0	1	1	0	0	0	0	0
2	RXLPFEN	Rx LPF Enable	0 = Disable 1 = Enable	0	1	1	1	1	0	0	1	1	0	0	0	0	0
3	PGAQEN	Rx Q PGA Enable	0 = Disable 1 = Enable	0	1	1	1	1	0	0	1	1	0	0	0	0	0
4	PGAIEN	Rx I PGA Enable	0 = Disable 1 = Enable	0	1	1	1	1	0	0	1	1	0	0	0	0	0
5	ADCEN	ADC Enable	0 = Disable 1 = Enable	0	1	1	1	1	0	0	1	1	0	0	0	0	0
6	ADCCLKEN	ADC Clock Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	0	0	0
7	LVDSQ	Rx Q LVDS Enable	0 = Disable 1 = Enable	0	1	1	1	1	0	0	1	1	0	0	0	0	0
8	LVDSI	Rx I LVDS Enable	0 = Disable 1 = Enable	0	1	1	1	1	0	0	1	1	0	0	0	0	0
9	TXVGCEN	Tx VGC Enable	0 = Disable 1 = Enable	0	0	0	0	0	1	1	1	1	0	0	0	0	0
10	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	RXSYNEN	Rx SYN Enable	0 = Disable 1 = Enable	0	1	1	1	1	0	0	1	1	1	0	0	0	0
12	TXSYNEN	Tx SYN Enable	0 = Disable 1 = Enable	0	0	0	0	0	1	1	1	1	0	1	0	0	0
13	BBLBEN	BB Loopback Enable	0 = Disable 1 = Enable	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	TSEN	Temperature Sensor Enable	0 = Disable 1 = Enable	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	PADEN	PA Driver Enable	0 = Disable 1 = Enable	0	0	0	0	0	1	1	1	1	0	0	0	0	0
16	TXLPFEN	Tx LPF Enable	0 = Disable 1 = Enable	0	0	0	0	0	1	1	1	1	0	0	0	0	0

Table 20. RX_ENABLE Register 0 (Address = 00000) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
17	TXLOEN	Tx LO Enable	0 = Disable 1 = Enable	0	0	0	0	0	1	1	1	1	0	0	0	0	0
18	UPCXEN	Upconverter Enable	0 = Disable 1 = Enable	0	0	0	0	0	1	1	1	1	0	0	0	0	0
19	Reserved	Reserved		0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				1	0	0	0	0	0	0	0	0	0	0	0	0	0
21				2	0	0	0	0	0	0	0	0	0	0	0	0	0
22				3	0	0	0	0	0	0	0	0	0	0	0	0	0
23				4	0	0	0	0	0	0	0	0	0	0	0	0	0
24				5	0	0	0	0	0	0	0	0	0	0	0	0	0
25				6	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 21. RX_GAIN Register 1 (Address = 00001)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	LNASEL <2:0>	LNA Selection	<2:0> = 000 = RXIN1 (PCS) <2:0> = 001 = RXIN3 (CELL) <2:0> = 101 = RXIN4 (GSM) <2:0> = X10 = RXIN5 (IMT)	0	0	1	1	0	0	1	0	1	0	0	1	1	1
1				1	0	0	0	1	0	0	0	0	0	0	0	0	0
2				2	0	0	1	0	0	0	0	0	0	0	0	0	0
3	BandSel_Mix	Rx Mixer Select	0 = CEL mixer (default) 1 = PCS mixer	0	1	0	0	1	1	0	1	0	1	1	0	0	0

Table 21. RX_GAIN Register 1 (Address = 00001) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
4	MX_SW <1:0>	Rx Mixer Input Select	If BandSel_Mix = 0 (CELL) X0 = CELL input X1 = GSM input If BandSel_Mix = 1 (PCS) 00 = DCS input 01 = PCS input 10 = IMT input 11 = None	0	1	0	1	0	1	0	1	0	1	1	0	0	0
5				1	0	0	0	1	0	0	0	0	0	0	0	0	0
6	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				1	0	0	0	0	0	0	0	0	0	0	0	0	0
8	PGAGAIN <3:0>	Rx PGA Gain Control	<3:0> = 0000 = Min gain (default) <3:0> = 0001 = Min gain + 3dB … <3:0> = 1110 = Max gain - 3dB <3:0> = 1111 = Max gain	0	0	0	1	1	0	0	0	0	0	0	0	0	0
9				1	1	1	1	1	0	0	1	1	1	0	0	0	0
10				2	1	1	0	0	0	0	1	1	1	0	0	0	0
11				3	0	0	1	1	0	0	0	0	0	0	0	0	0
12	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				1	0	0	0	0	0	0	0	0	0	0	0	0	0
14	LNAGAIN <1:0>	LNA Gain Control	<1:0> = 00 = Low gain <1:0> = 01 = Mid gain (not available for RXIN4) <1:0> = 10 = High gain (default) <1:0> = 11 = Do **not** use	0	0	0	0	0	1	1	0	0	0	1	1	1	1
15				1	1	1	1	1	0	0	1	1	1	0	0	0	0
16	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				1	0	0	0	0	0	0	0	0	0	0	0	0	0
18				3	0	0	0	0	0	0	0	0	0	0	0	0	0
19				4	0	0	0	0	0	0	0	0	0	0	0	0	0
20				5	0	0	0	0	0	0	0	0	0	0	0	0	0
21				6	0	0	0	0	0	0	0	0	0	0	0	0	0
22				7	0	0	0	0	0	0	0	0	0	0	0	0	0
23				8	0	0	0	0	0	0	0	0	0	0	0	0	0
24				9	0	0	0	0	0	0	0	0	0	0	0	0	0
25				10	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 22. Reserved Register 2 (Address = 00010)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	1	1	1	1	1	1	1	1	1	1	1	1	1
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	1	1	1	1	1	1	1	1	1	1	1	1	1
24				24	1	1	1	1	1	1	1	1	1	1	1	1	1
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 23. RX_LNA Register 3 (Address = 00011)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	1	1	1	1	1	1	1	1	1	1	1	1	1
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11	RXSYN_ RBYP	Rx RF PLL Loop Filter	Rx RF PLL Loop Filter Adjust 0 = WCDMA 1 = Not used	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				1	0	0	0	0	0	0	0	0	0	0	0	0	0
14				2	1	1	1	1	1	1	1	1	1	1	1	1	1
15				3	1	1	1	1	1	1	1	1	1	1	1	1	1
16				4	1	1	1	1	1	1	1	1	1	1	1	1	1
17	RVCO_DIV2 <1:0>	Rx RF VCO Prescaler Divider	Rx RF VCO Prescaler Divide Ratio Configuration <1:0> = 01 = CELL <1:0> = 10 = PCS	0	0	1	1	0	0	1	0	1	0	0	1	1	1
18				1	1	0	0	1	1	0	1	0	1	1	0	0	0
19	RVCO_SEL <1:0>	Rx RF VCO Selection	<1:0> = 00 = Disable <1:0> = 01 = ROL (CELL) <1:0> = 10 = ROH (PCS) <1:0> = 11 = Not used	0	0	1	1	0	0	1	0	1	0	0	1	1	1
20				1	1	0	0	1	1	0	1	0	1	1	0	0	0
21	RVCOTUNE <1:0>	Rx RF VCO ROH Band Selection	<1:0> = 00 = band2 (CELL) <1:0> = 01 = band3 (PCS) <1:0> = 11 = Not used	0	1	1	0	0	1	1	1	1	1	1	1	1	1
22				1	0	0	0	0	0	0	0	0	0	0	0	0	0
23	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
24				1	0	0	0	0	0	0	0	0	0	0	0	0	0
25				2	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 24. Reserved Register 4 (Address = 00100)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	1	1	1	1	1	1	1	1	1	1	1	1	1
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	1	1	1	1	1	1	1	1	1	1	1	1	1
12				12	1	1	1	1	1	1	1	1	1	1	1	1	1
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	1	1	1	1	1	1	1	1	1	1	1	1	1
18				18	1	1	1	1	1	1	1	1	1	1	1	1	1
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	1	1	1	1	1	1	1	1	1	1	1	1	1
23				23	1	1	1	1	1	1	1	1	1	1	1	1	1
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 25. Reserved Register 5 (Address = 00101)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	1	1	1	1	1	1	1	1	1	1	1	1	1
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	1	1	1	1	1	1	1	1	1	1	1	1	1
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	1	1	1	1	1	1	1	1	1	1	1	1	1
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 26. RX_LPF Register 6 (Address = 00110)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	1	1	1	1	1	1	1	1	1	1	1	1	1
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	1	1	1	1	1	1	1	1	1	1	1	1	1
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	1	1	1	1	1	1	1	1	1	1	1	1	1
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17	LPFBYPASS	Rx LPF Bypass	0 = Normal operation 1 = Bypass Rx LPF	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				1	0	0	0	0	0	0	0	0	0	0	0	0	0
20				2	0	0	0	0	0	0	0	0	0	0	0	0	0
21				3	0	0	0	0	0	0	0	0	0	0	0	0	0
22				4	0	0	0	0	0	0	0	0	0	0	0	0	0
23	BBMODE	Rx LPF Bandwidth Select	000 = WCDMA 011 = GSM	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				1	0	0	0	0	0	0	0	0	0	0	0	0	0
25				2	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 27. GPO_CONFIG Register 7 (Address = 00111)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	GPO3_LD_ RD_sel_LSB		GPO3 Output Mux Select LSB MSB in REG7<17> 00 = RXPLL LD 01 = TXPLL LD 10 = Output selected by GPO3<1:0> 11 = RXPLL LD and TXPLL LD and CLKPLL LD	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	GPO2<1:0>	GPO2 Output Select	<1:0> = 00 = High-Z <1:0> = 01 = High-Z <1:0> = 10 = Low-Z low <1:0> = 11 = Low-Z high	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3				1	0	0	0	0	0	0	0	0	0	0	0	0	0
4	GPO3<1:0>	GPO3 Output Select	<1:0> = 00 = High-Z <1:0> = 01 = High-Z <1:0> = 10 = Low-Z low <1:0> = 11 = Low-Z high	0	1	1	1	1	1	1	1	1	1	1	1	1	1
5				1	0	0	0	0	0	0	0	0	0	0	0	0	0
6	TS_TRIG	Temperature Sensor Reading Trigger	0 = Not trigger reading 1 = Trigger reading	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	Temp_out <4:0>	Temperature Sensor Output	To be read at DOUT pin through SPI readback	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				1	0	0	0	0	0	0	0	0	0	0	0	0	0
9				2	0	0	0	0	0	0	0	0	0	0	0	0	0
10				3	0	0	0	0	0	0	0	0	0	0	0	0	0
11				4	0	0	0	0	0	0	0	0	0	0	0	0	0
12	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				1	0	0	0	0	0	0	0	0	0	0	0	0	0
14				2	1	1	1	1	1	1	1	1	1	1	1	1	1
15				3	0	0	0	0	0	0	0	0	0	0	0	0	0
16				4	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 27. GPO_CONFIG Register 7 (Address = 00111) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
17	GPO3_LD_ RD_sel_MSB		GPO3 Output Mux Select MSB LSB in REG7<1> 00 = RXPLL LD 01 = TXPLL LD 10 = Output selected by GPO3<0:1> 11 = RXPLL LD and TXPLL LD and CLKPLL LD	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
19				1	1	1	1	1	1	1	1	1	1	1	1	1	1
20	DOUT_DRV <1:0>	DOUT Drive Strength	<1:0> = 00 = 1x <1:0> = 01 = 2x <1:0> = 10 = 3x <1:0> = 11 = 4x	0	1	1	1	1	1	1	1	1	1	1	1	1	1
21				1	1	1	1	1	1	1	1	1	1	1	1	1	1
22	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				1	0	0	0	0	0	0	0	0	0	0	0	0	0
24				2	0	0	0	0	0	0	0	0	0	0	0	0	0
25				3	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 28. Reserved Register 8 (Address = 01000)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 29. Reserved Register 9 (Address = 01001)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 30. RXLO_FRAC Register 10 (Address = 01010)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	RFFRAC <19:0>	Receiver RF Synthesizer Fractional Division Ratio	See the *RF Synthesizers* section	0	1	0	0	0	1	1	1	0	1	1	0	0	0
1				1	0	0	0	0	1	1	0	0	0	1	0	0	0
2				2	1	0	0	0	0	0	1	0	1	0	0	0	0
3				3	0	0	0	0	1	1	0	0	0	1	0	0	0
4				4	1	0	0	0	0	0	1	0	1	0	0	0	0
5				5	0	0	0	0	1	1	0	0	0	1	0	0	0
6				6	1	0	0	0	0	0	1	0	1	0	0	0	0
7				7	0	0	0	0	1	1	0	0	0	1	0	0	0
8				8	1	0	0	0	0	0	1	0	1	0	0	0	0
9				9	0	0	0	0	1	1	0	0	0	1	0	0	0
10				10	1	0	0	0	0	0	1	1	1	0	0	0	0
11				11	0	0	0	0	1	1	0	0	0	1	0	0	0
12				12	1	0	0	0	0	0	1	0	1	0	0	0	0
13				13	0	0	0	0	1	1	0	0	0	1	0	0	0
14				14	1	0	0	0	0	0	1	0	1	0	0	0	0
15				15	1	0	0	1	1	1	1	0	1	1	1	1	1
16				16	1	1	0	0	0	1	1	1	1	0	1	1	1
17				17	0	1	1	0	1	1	0	1	0	1	1	1	1
18				18	0	0	1	1	1	1	0	0	0	1	0	0	0
19				19	1	0	1	1	1	1	1	0	1	1	1	1	1
20	Reserved	—	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
21				1	0	0	0	0	0	0	0	0	0	0	0	0	0
22				2	0	0	0	0	0	0	0	0	0	0	0	0	0
23				3	0	0	0	0	0	0	0	0	0	0	0	0	0
24				4	0	0	0	0	0	0	0	0	0	0	0	0	0
25				5	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 31. RXLO_SYN Register 11 (Address = 01011)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	RINT<7:0>	Rx RF PLL Integer Divide Ratio	See the *RF Synthesizers* section	0	1	0	0	1	1	0	1	0	1	1	0	0	0
1				1	1	0	0	1	0	1	1	0	1	0	1	1	1
2				2	0	0	1	1	0	1	0	0	0	0	1	1	1
3				3	0	1	1	0	0	0	0	1	0	0	0	0	0
4				4	0	1	1	0	0	1	0	1	0	0	1	1	1
5				5	1	0	0	1	1	0	1	0	1	1	0	0	0
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8	RRD	Rx Reference Divide Ratio	0 = Divide-by-1 1 = Divide-by-2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
10				1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				2	1	1	1	1	1	1	1	1	1	1	1	1	1
12				3	0	0	0	0	0	0	0	0	0	0	0	0	0
13				4	0	0	0	0	0	0	0	0	0	0	0	0	0
14				5	0	0	0	0	0	0	0	0	0	0	0	0	0
15				6	0	0	0	0	0	0	0	0	0	0	0	0	0
16				7	0	0	0	0	0	0	0	0	0	0	0	0	0
17				8	0	0	0	0	0	0	0	0	0	0	0	0	0
18	RCPI<2:0>	Rx PLL Charge-Pump Current	Rx RF PLL Charge-Pump Current 000 = Not used 001 = 200µA 011 = 600µA 110 = 1200µA	0	1	1	1	1	1	1	1	1	1	1	1	1	1
19				1	1	1	1	1	1	1	1	1	1	1	1	1	1
20				2	0	0	0	0	0	0	0	0	0	0	0	0	0
21	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				1	0	0	0	0	0	0	0	0	0	0	0	0	0
23				2	1	1	1	1	1	1	1	1	1	1	1	1	1
24				3	1	1	1	1	1	1	1	1	1	1	1	1	1
25				4	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 32. BBCLK_OUT Register 12 (Address = 01100)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	ADF<2:0>	ADC Clock Divide Ratio	000 = 1 for WCDMA 001 = Not used 010 = Not used 011 = 6 for GSM 100~111 = Not used	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
4				1	0	0	0	0	0	0	0	0	0	0	0	0	0
5				2	0	0	0	0	0	0	0	0	0	0	0	0	0
6				3	0	0	0	0	0	0	0	0	0	0	0	0	0
7				4	0	0	0	0	0	0	0	0	0	0	0	0	0
8				5	0	0	0	0	0	0	0	0	0	0	0	0	0
9	LVDSI_2X	RxBB LVDS 2X Current Enable	0 = 220Ω load 1 = 100Ω load	0	1	1	1	1	1	1	1	1	1	1	1	1	1
10	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
11				1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				2	0	0	0	0	0	0	0	0	0	0	0	0	0
13				3	0	0	0	0	0	0	0	0	0	0	0	0	0
14				4	0	0	0	0	0	0	0	0	0	0	0	0	0
15				5	0	0	0	0	0	0	0	0	0	0	0	0	0
16				6	0	0	0	0	0	0	0	0	0	0	0	0	0
17				7	0	0	0	0	0	0	0	0	0	0	0	0	0
18				8	0	0	0	0	0	0	0	0	0	0	0	0	0
19				9	0	0	0	0	0	0	0	0	0	0	0	0	0
20				10	1	1	1	1	1	1	1	1	1	1	1	1	1
21				11	0	0	0	0	0	0	0	0	0	0	0	0	0
22				12	0	0	0	0	0	0	0	0	0	0	0	0	0
23				13	0	0	0	0	0	0	0	0	0	0	0	0	0
24				14	0	0	0	0	0	0	0	0	0	0	0	0	0
25				15	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 33. Reserved Register 13 (Address = 01101)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				0	1	1	1	1	1	1	1	1	1	1	1	1	1
3				1	0	0	0	0	0	0	0	0	0	0	0	0	0
4				2	0	0	0	0	0	0	0	0	0	0	0	0	0
5				3	1	1	1	1	1	1	1	1	1	1	1	1	1
6				0	1	1	1	1	1	1	1	1	1	1	1	1	1
7				1	0	0	0	0	0	0	0	0	0	0	0	0	0
8				2	0	0	0	0	0	0	0	0	0	0	0	0	0
9				3	0	0	0	0	0	0	0	0	0	0	0	0	0
10				4	0	0	0	0	0	0	0	0	0	0	0	0	0
11				5	1	1	1	1	1	1	1	1	1	1	1	1	1
12				0	1	1	1	1	1	1	1	1	1	1	1	1	1
13				0	1	1	1	1	1	1	1	1	1	1	1	1	1
14				0	1	1	1	1	1	1	1	1	1	1	1	1	1
15				1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				2	0	0	0	0	0	0	0	0	0	0	0	0	0
17				0	1	1	1	1	1	1	1	1	1	1	1	1	1
18				1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				2	0	0	0	0	0	0	0	0	0	0	0	0	0
20				0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 34. BBCLK_FRAC Register 14 (Address = 01110)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	CFRAC <19:0>	ADC Clock PLL Fractional Divide Ratio	WCDMA: For f_{REFIN} = 13.0MHz = 85E85 (hex) 15.36MHz = 00000 (hex) 19.2MHz = 00000 (hex) 26.0MHz = 42F4s (hex) GSM: For f_{REFIN} = 13.0MHz = 00000 (hex) 15.36MHz = 40000 (hex) 19.2MHz = 00000 (hex) 26.0MHz = 00000 (hex)	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0
20	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
21				1	0	0	0	0	0	0	0	0	0	0	0	0	0
22				2	0	0	0	0	0	0	0	0	0	0	0	0	0
23				3	0	0	0	0	0	0	0	0	0	0	0	0	0
24				4	0	0	0	0	0	0	0	0	0	0	0	0	0
25				5	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 35. BBCLK SYN Register 15 (Address = 01111)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	CINT<7:0>	ADC Clock PLL Integer Divide Ratio	WCDMA: For f_{REFIN} = 13.0MHz = 5E (hex) 15.36MHz = 50 (hex) 19.2MHz = 40 (hex) 26.0MHz = 2F (hex) GSM: For f_{REFIN} = 13.0MHz = 60 (hex) 15.36MHz = 51 (hex) 19.2MHz = 41 (hex) 26.0MHz = 30 (hex)	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8	CRD	ADC Clock PLL Reference Divide Ratio	0 = Divide-by-1 (default) 1 = Divide-by-2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				2	1	1	1	1	1	1	1	1	1	1	1	1	1
12				3	0	0	0	0	0	0	0	0	0	0	0	0	0
13				4	0	0	0	0	0	0	0	0	0	0	0	0	0
14				5	0	0	0	0	0	0	0	0	0	0	0	0	0
15				6	0	0	0	0	0	0	0	0	0	0	0	0	0
16				7	0	0	0	0	0	0	0	0	0	0	0	0	0
17				8	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 35. BBCLK SYN Register 15 (Address = 01111) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
18	CCPI<2:0>	ADC Clock PLL Charge Pump Current	000 = 0µA, do **not** use 001 = 25µA 010 = 50µA (f_{REFIN} = 26MHz) 011 = 75µA (f_{REFIN} = 19.2MHz 100 = 100µA (f_{REFIN} = 13MHz) 111 = 175µA	0	1	1	1	1	1	1	1	1	1	1	1	1	1
19				1	1	1	1	1	1	1	1	1	1	1	1	1	1
20				2	0	0	0	0	0	0	0	0	0	0	0	0	0
21	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	EN_ PBYQDIV	ADC Clock PLL P/Q Rational Division Enable	ADC Clock PLL P/Q Rational Division Enable 0 = Disabled 1 = Enable	1	1	1	1	1	1	1	1	1	1	1	1	1	1
23	CINTB	ADC Clock PLL Integer/ Fractional Mode	ADC Clock Integer/Fractional Mode 0 = Integer mode 1 = Fractional mode	1	1	1	1	1	1	1	1	1	1	1	1	1	1
24	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 36. BBCLK_MISC Register 16 (Address = 10000)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	PBYQ_ RATUP<7:0>	ADC Clock Fractional LSB Dither **Up** Number of Cycles LSB Is High	WCDMA: For f_{REFIN} = 13.0MHz = 3B (hex) 15.36MHz = 00 (hex) 19.2MHz = 00 (hex) 20.0MHz = 0B (hex) 26.0MHz = 3E (hex) GSM: For f_{REFIN} = 13.0MHz = 00 (hex) 15.36MHz = 00 (hex) 19.2MHz = 00 (hex) 26.0MHz = 00 (hex)	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8	PBYQ_ RATDN<7:0>	ADC Clock Fractional LSB Dither **Down** Number of Cycles LSB Is Low	DC Clock Fractional LSB Dither **Down**. Number of cycles LSB is low. WCDMA: For f_{REFIN} = 13.0MHz = 06 (hex) 15.36MHz = 00 (hex) 19.2MHz = 00 (hex) 20.0MHz = 0E (hex) 26.0MHz = 03 (hex) GSM: For f_{REFIN} = 13.0MHz = 00 (hex) 15.36MHz = 00 (hex) 19.2MHz = 00 (hex) 26.0MHz = 00 (hex)	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				1	0	0	0	0	0	0	0	0	0	0	0	0	0
10				2	0	0	0	0	0	0	0	0	0	0	0	0	0
11				3	0	0	0	0	0	0	0	0	0	0	0	0	0
12				4	0	0	0	0	0	0	0	0	0	0	0	0	0
13				5	0	0	0	0	0	0	0	0	0	0	0	0	0
14				6	0	0	0	0	0	0	0	0	0	0	0	0	0
15				7	0	0	0	0	0	0	0	0	0	0	0	0	0
16	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				1	0	0	0	0	0	0	0	0	0	0	0	0	0
18				2	1	1	1	1	1	1	1	1	1	1	1	1	1
19				3	1	1	1	1	1	1	1	1	1	1	1	1	1
20	CDR_DIV2_ EN	CLK VCO to CDR Divide-by-2 Enable	CLK VCO to CDR Divide-by-2 Enable 0 = Disable 1 = Enable	0	0	0	0	0	1	1	1	1	0	0	0	0	0
21	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				1	0	0	0	0	0	0	0	0	0	0	0	0	0
23				2	0	0	0	0	0	0	0	0	0	0	0	0	0
24				3	0	0	0	0	0	0	0	0	0	0	0	0	0
25				4	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 37. BBCLK_SPARE Register 17 (Address = 10001)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	1	1	1	1	1	1	1	1	1	1	1	1	1
12				12	1	1	1	1	1	1	1	1	1	1	1	1	1
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0
18	DIE_ID_sel	Die ID Readout Select	Affect REG17<25:19> 0 = Read register value 1 = Read die ID	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	DIE_ID<6:0>	Die ID Readout Bits at DOUT pin	DIE_ID<2:0> 001 = 1Z 010 = 2Z 011 = 3Z	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				1	0	0	0	0	0	0	0	0	0	0	0	0	0
21				2	0	0	0	0	0	0	0	0	0	0	0	0	0
22				3	0	0	0	0	0	0	0	0	0	0	0	0	0
23				4	0	0	0	0	0	0	0	0	0	0	0	0	0
24				5	0	0	0	0	0	0	0	0	0	0	0	0	0
25				6	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 38. TX_LPF Register 18 (Address = 10010)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5	TXLPFB <2:0>	TXLPF Bandwidth	000 = Do not use 001 = WCDMA 010 = Do not use 011 = Do not use 100~111 = Do not use	0	1	1	1	1	1	1	1	1	1	1	1	1	1
6				1	0	0	0	0	0	0	0	0	0	0	0	0	0
7				2	0	0	0	0	0	0	0	0	0	0	0	0	0
8	TXLPFMD <1:0>	TXLPF Operating Mode	<1:0> = 00 = Shut down <1:0> = 01 = LPF bypass <1:0> = 10 = Do not use <1:0> = 11 = Normal operation (WCDMA)	0	1	1	1	1	1	1	1	1	1	1	1	1	1
9				1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	BBLB	TXLPF Baseband Loopback	0 = Enable loopback 1 = Normal operation	0	1	1	1	1	1	1	1	1	1	1	1	1	1
11	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				1	1	1	1	1	1	1	1	1	1	1	1	1	1
13				2	1	1	1	1	1	1	1	1	1	1	1	1	1
14				3	0	0	0	0	0	0	0	0	0	0	0	0	0
15				4	1	1	1	1	1	1	1	1	1	1	1	1	1
16				5	1	1	1	1	1	1	1	1	1	1	1	1	1
17				6	1	1	1	1	1	1	1	1	1	1	1	1	1
18				7	1	1	1	1	1	1	1	1	1	1	1	1	1
19				8	0	0	0	0	0	0	0	0	0	0	0	0	0
20				9	1	1	1	1	1	1	1	1	1	1	1	1	1
21				10	0	0	0	0	0	0	0	0	0	0	0	0	0
22				11	1	1	1	1	1	1	1	1	1	1	1	1	1
23				12	0	0	0	0	0	0	0	0	0	0	0	0	0
24				13	0	0	0	0	0	0	0	0	0	0	0	0	0
25	TXINDACF	Tx DAC Bandwidth Select	Tx DAC Bandwidth 1 = 15MHz	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 39. TX_PAD Register 19 (Address = 10011)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	PAD_BAND <2:0>	PA Driver Frequency Band	<1:0> = 00 = CELL <1:0> = 01 = Do not use <1:0> = 10 = PCS <1:0> = 11 = Do not use	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	1	0	0	1	1	0	1	0	1	1	0	0	0
2	PAD_CTUNE <4:0>	PA Driver Center Frequency Select	CELL = 00100 PCS = 10001	0	1	0	0	1	1	0	1	0	1	1	0	0	0
3				1	0	0	0	0	0	0	0	0	0	0	0	0	0
4				2	0	1	1	0	0	1	0	1	0	0	1	1	1
5				3	0	0	0	0	0	0	0	0	0	0	0	0	0
6				4	1	0	0	1	1	0	1	0	1	1	0	0	0
7	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				1	0	0	0	0	0	0	0	0	0	0	0	0	0
9				2	1	1	1	1	1	1	1	1	1	1	1	1	1
10				3	1	1	1	1	1	1	1	1	1	1	1	1	1
11				4	0	0	0	0	0	0	0	0	0	0	0	0	0
12				5	0	0	0	0	0	0	0	0	0	0	0	0	0
13				6	1	1	1	1	1	1	1	1	1	1	1	1	1
14				7	0	0	0	0	0	0	0	0	0	0	0	0	0
15				8	1	1	1	1	1	1	1	1	1	1	1	1	1
16				9	1	1	1	1	1	1	1	1	1	1	1	1	1
17				10	1	1	1	1	1	1	1	1	1	1	1	1	1
18				11	1	1	1	1	1	1	1	1	1	1	1	1	1
19				12	0	0	0	0	0	0	0	0	0	0	0	0	0
20				13	0	0	0	0	0	0	0	0	0	0	0	0	0
21				14	0	0	0	0	0	0	0	0	0	0	0	0	0
22				15	0	0	0	0	0	0	0	0	0	0	0	0	0
23				16	0	0	0	0	0	0	0	0	0	0	0	0	0
24				17	0	0	0	0	0	0	0	0	0	0	0	0	0
25				18	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 40. TX_UPX1 Register 20 (Address = 10100)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	1	1	1	1	1	1	1	1	1	1	1	1	1
5				5	1	1	1	1	1	1	1	1	1	1	1	1	1
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	1	1	1	1	1	1	1	1	1	1	1	1	1
13				13	1	1	1	1	1	1	1	1	1	1	1	1	1
14				14	1	1	1	1	1	1	1	1	1	1	1	1	1
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	1	1	1	1	1	1	1	1	1	1	1	1	1
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0
19	TXLO_IQ_GAIN	TXLO IQ Phase Adjust Slope	0 = PCS bands 1 = CELL band	0	0	1	1	0	0	1	0	1	0	0	1	1	1
20	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
21				1	0	0	0	0	0	0	0	0	0	0	0	0	0
22				2	0	0	0	0	0	0	0	0	0	0	0	0	0
23				3	0	0	0	0	0	0	0	0	0	0	0	0	0
24	BIAS_EN	Master Bias Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	0	0	0
25	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 41. TX_UPX2 Register 21 (Address = 10101)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	UCX_CSW <3:0>	UCX Tank Frequency Adjust	0000 = PCS 1101 = CELL	0	0	1	1	0	0	1	0	1	0	0	1	1	1
3				1	0	0	0	0	0	0	0	0	0	0	0	0	0
4				2	0	1	1	0	0	1	0	1	0	0	1	1	1
5				3	0	1	1	0	0	1	0	1	0	0	1	1	1
6	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				1	0	0	0	0	0	0	0	0	0	0	0	0	0
8				2	0	0	0	0	0	0	0	0	0	0	0	0	0
9				3	0	0	0	0	0	0	0	0	0	0	0	0	0
10				4	0	0	0	0	0	0	0	0	0	0	0	0	0
11				5	0	0	0	0	0	0	0	0	0	0	0	0	0
12				6	1	1	1	1	1	1	1	1	1	1	1	1	1
13				7	0	0	0	0	0	0	0	0	0	0	0	0	0
14				8	0	0	0	0	0	0	0	0	0	0	0	0	0
15				9	1	1	1	1	1	1	1	1	0	0	0	0	0
16				10	0	0	0	0	0	0	0	0	0	0	0	0	0
17				11	0	0	0	0	0	0	0	0	0	0	0	0	0
18				12	1	1	1	1	1	1	1	1	1	1	1	1	1
19				13	0	0	0	0	0	0	0	0	0	0	0	0	0
20				14	1	1	1	1	1	1	1	1	1	1	1	1	1
21				15	0	0	0	0	0	0	0	0	0	0	0	0	0
22				16	0	0	0	0	0	0	0	0	0	0	0	0	0
23				17	0	0	0	0	0	0	0	0	0	0	0	0	0
24				18	0	0	0	0	0	0	0	0	0	0	0	0	0
25				19	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 42. TX_UPX3 Register 22 (Address = 10110)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	1	1	1	1	1	1	1	1	1	1	1	1	1
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	1	1	1	1	1	1	1	1	1	1	1	1	1
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	1	1	1	1	1	1	1	1	1	1	1	1	1
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0
22	T_UCX_ BAND_SEL <1:0>	Upconverter Band Select	<1:0> = 00 = Do not use <1:0> = 01 = CELL band <1:0> = 10 = Do not use <1:0> = 11 = PCS band	0	1	1	1	1	1	1	1	1	1	1	1	1	1
23				1	1	0	0	1	1	0	1	0	1	1	0	0	0
24	UCX_V2I_ MODE_F <1:0>	Upconverter V2I Bandwidth	<1:0> = 00 = Do not use <1:0> = 01 = WCDMA <1:0> = 10 = Do not use <1:0> = 11 = Do not use	0	1	1	1	1	1	1	1	1	1	1	1	1	1
25				1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 43. TX_GAIN1 Register 23 (Address = 10111)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	TX_GAIN <9:0>	Tx Gain	000 (hex) = Minimum gain 3FF (hex) = Maximum gain	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	1	1	1	1	1	1	1	1	1	1	1	1	1
5				5	1	1	1	1	1	1	1	1	1	1	1	1	1
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1
10	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				2	0	0	0	0	0	0	0	0	0	0	0	0	0
13				3	0	0	0	0	0	0	0	0	0	0	0	0	0
14				4	1	1	1	1	1	1	1	1	1	1	1	1	1
15				5	1	1	1	1	1	1	1	1	1	1	1	1	1
16				6	0	0	0	0	0	0	0	0	0	0	0	0	0
17				7	0	0	0	0	0	0	0	0	0	0	0	0	0
18				8	0	0	0	0	0	0	0	0	0	0	0	0	0
19				9	0	0	0	0	0	0	0	0	0	0	0	0	0
20				10	0	0	0	0	0	0	0	0	0	0	0	0	0
21				11	1	1	1	1	1	1	1	1	1	1	1	1	1
22				12	0	0	0	0	0	0	0	0	0	0	0	0	0
23				13	0	0	0	0	0	0	0	0	0	0	0	0	0
24	GPO1<1:0>	GPO1 Output Select	<1:0> = 00 = High-Z <1:0> = 01 = High-Z <1:0> = 10 = Low-Z low <1:0> = 11 = Low-Z high	0	1	1	1	1	1	1	1	1	1	1	1	1	1
25				1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 44. TX_GAIN2 Register 24 (Address = 11000)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6	TXINDACI <5:0>	TXBB DAC Bias Current	TXBB DAC Bias Current 010100 = WCDMA	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				1	0	0	0	0	0	0	0	0	0	0	0	0	0
8				2	1	1	1	1	1	1	1	1	1	1	1	1	1
9				3	0	0	0	0	0	0	0	0	0	0	0	0	0
10				4	1	1	1	1	1	1	1	1	1	1	1	1	1
11				5	0	0	0	0	0	0	0	0	0	0	0	0	0
12	TXINDACZI	TXBB Differential Input Impedance	0 = 220Ω 1 = 100Ω	0	1	1	1	1	1	1	1	1	1	1	1	1	1
13	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				1	0	0	0	0	0	0	0	0	0	0	0	0	0
15				2	0	0	0	0	0	0	0	0	0	0	0	0	0
16				3	0	0	0	0	0	0	0	0	0	0	0	0	0
17				4	0	0	0	0	0	0	0	0	0	0	0	0	0
18	CDR_EN	CDR Enable	CDR Enable 0 = Disable 1 = Enable	0	0	0	0	0	1	1	1	1	0	0	0	0	0
19	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
20				1	1	1	1	1	1	1	1	1	1	1	1	1	1
21	TXBB_LVDS_ DDR3	TXBB Input LVDS/DDR3 Select	TXBB Input LVDS/DDR3 Select 0 = LVDS 1 = DDR3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				1	0	0	0	0	0	0	0	0	0	0	0	0	0
24				2	0	0	0	0	0	0	0	0	0	0	0	0	0
25				3	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 45. Reserved Register 25 (Address = 11001)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 46. Reserved Register 26 (Address = 11010)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	1	1	1	1	1	1	1	1	1	1	1	1	1
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	1	1	1	1	1	1	1	1	1	1	1	1	1
20				20	1	1	1	1	1	1	1	1	1	1	1	1	1
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 47. TXLO_FRAC Register 27 (Address = 11011)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	TFRAC <19:0>	Tx RF PLL Fractional Divide Ratio	AAAAB (hex) = CELL band 36AAB (hex) = PCS band	0	0	0	0	0	0	0	0	0	0	1	1	1	1
1				1	0	0	0	0	0	0	0	0	0	0	1	1	1
2				2	0	0	0	0	0	0	0	0	0	1	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	1	1	1
4				4	0	0	0	0	0	0	0	0	0	1	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	1	1	1
6				6	0	0	0	0	0	0	0	0	0	1	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	1	1	1
8				8	0	0	0	0	0	0	0	0	0	1	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	1	1	1
10				10	0	0	0	0	0	0	0	0	0	1	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	1	1	1
12				12	0	0	0	0	0	0	0	0	0	1	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	1	1	1
14				14	0	0	0	0	0	0	0	0	0	1	0	0	0
15				15	1	0	0	1	1	0	1	0	1	0	1	1	1
16				16	0	0	0	0	0	0	0	0	0	1	0	0	0
17				17	0	1	1	0	1	1	0	1	0	0	1	1	1
18				18	1	1	1	1	1	1	1	1	1	0	0	0	0
19				19	1	1	1	1	1	1	1	1	1	0	1	1	1
20	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
21				1	0	0	0	0	0	0	0	0	0	0	0	0	0
22				3	0	0	0	0	0	0	0	0	0	0	0	0	0
23				4	0	0	0	0	0	0	0	0	0	0	0	0	0
24				5	0	0	0	0	0	0	0	0	0	0	0	0	0
25				6	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 48. TXLO_SYN Register 28 (Address = 11100)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	TINT<7:0>	Tx RF PLL Integer Divide Ratio	5B (hex) = CELL 66 (hex) = PCS	0	1	0	0	1	1	0	1	0	1	0	1	1	1
1				1	1	0	0	1	1	0	1	0	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	0	0	0
3				3	0	1	1	0	0	1	0	1	0	0	1	1	1
4				4	0	1	1	0	0	1	0	1	0	0	1	1	1
5				5	1	0	0	1	1	0	1	0	1	1	0	0	0
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8	TRD	Tx Reference Divide Ratio	0 = Divide-by-1 1 = Divide-by-2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
10				1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				2	1	1	1	1	1	1	1	1	1	1	1	1	1
12	TVCO_DIV2 <1:0>	Tx RF VCO Prescaler Divide Ratio Configuration	<1:0> = 01 = CELL <1:0> = 10 = PCS	0	0	1	1	0	0	1	0	1	0	0	1	1	1
13				1	1	0	0	1	1	0	1	0	1	1	0	0	0
14	TVCO_SEL <1:0>	Tx RF VCO Selection	<1:0> = 00 = Disable <1:0> = 01 = ROL <1:0> = 10 = ROH <1:0> = 11 = Not used	0	0	1	1	0	0	1	0	1	0	0	1	1	1
15				1	1	0	0	1	1	0	1	0	1	1	0	0	0
16	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				1	0	0	0	0	0	0	0	0	0	0	0	0	0
18	TCPI<2:0>	Tx RF PLL Charge Pump Current	000 = 0μA, 001 = 200μA ... 100 = 800μA ... 110 = 1200μA	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				1	0	0	0	0	0	0	0	0	0	0	0	0	0
20				2	1	1	1	1	1	1	1	1	1	1	1	1	1
21	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
22				1	0	0	0	0	0	0	0	0	0	0	0	0	0
23				2	1	1	1	1	1	1	1	1	1	1	1	1	1
24				3	1	1	1	1	1	1	1	1	1	1	1	1	1
25				4	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 49. TXLO_REF Register 29 (Address = 11101)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12	REFIN_ ENOUT1	Reference Rx PLL Output Enable	Reference for Rx PLL Enable 0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	1	1	1
13	REFIN_ ENOUT2	Reference Tx PLL Output Enable	Reference for Tx PLL Enable 0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	0	0	0
14	REFIN_ ENOUT3	REFOUT Enable	REFOUT Enable 0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	0	1	0
15	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				1	0	0	0	0	0	0	0	0	0	0	0	0	0
17				2	0	0	0	0	0	0	0	0	0	0	0	0	0
18				3	1	1	1	1	1	1	1	1	1	1	1	1	1
19				4	0	0	0	0	0	0	0	0	0	0	0	0	0
20				5	1	1	1	1	1	1	1	1	1	1	1	1	1
21	REFOUT_ DRV<1:0>	REFOUT Buffer Drive Strength	REFOUT Drive Strength 00 = 1x 01 = 2x 10 = 3x 11 = 4x	0	1	1	1	1	1	1	1	1	1	1	1	1	1
22				1	1	1	1	1	1	1	1	1	1	1	1	1	1
23	REFOUT_LV_ CMOS_SEL	REFOUT Output Driver Select	0 = CMOS 1 = Low voltage	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 50. TXLO_AFCDAC Register 30 (Address = 11110)

BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	AFCDAC <11:0>	AFCDAC Output Voltage	800 (hex) V_{AFCOUT} = 0.4 + (2.5 - 0.4) x AFCDAC/2^{12}	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	1	1	1	1	1	1	1	1	1	1	1	1	1
12	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				1	0	0	0	0	0	0	0	0	0	0	0	0	0
14				2	0	0	0	0	0	0	0	0	0	0	0	0	0
15				3	0	0	0	0	0	0	0	0	0	0	0	0	0
16				4	0	0	0	0	0	0	0	0	0	0	0	0	0
17				5	0	0	0	0	0	0	0	0	0	0	0	0	0
18				6	0	0	0	0	0	0	0	0	0	0	0	0	0
19	AFCDAC_EN	AFCDAC Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	1	1	0
20	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				1	0	0	0	0	0	0	0	0	0	0	0	0	0
22				2	0	0	0	0	0	0	0	0	0	0	0	0	0
23				3	0	0	0	0	0	0	0	0	0	0	0	0	0
24				4	0	0	0	0	0	0	0	0	0	0	0	0	0
25				5	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 51. Reserved Register 31 (Address = 11111)

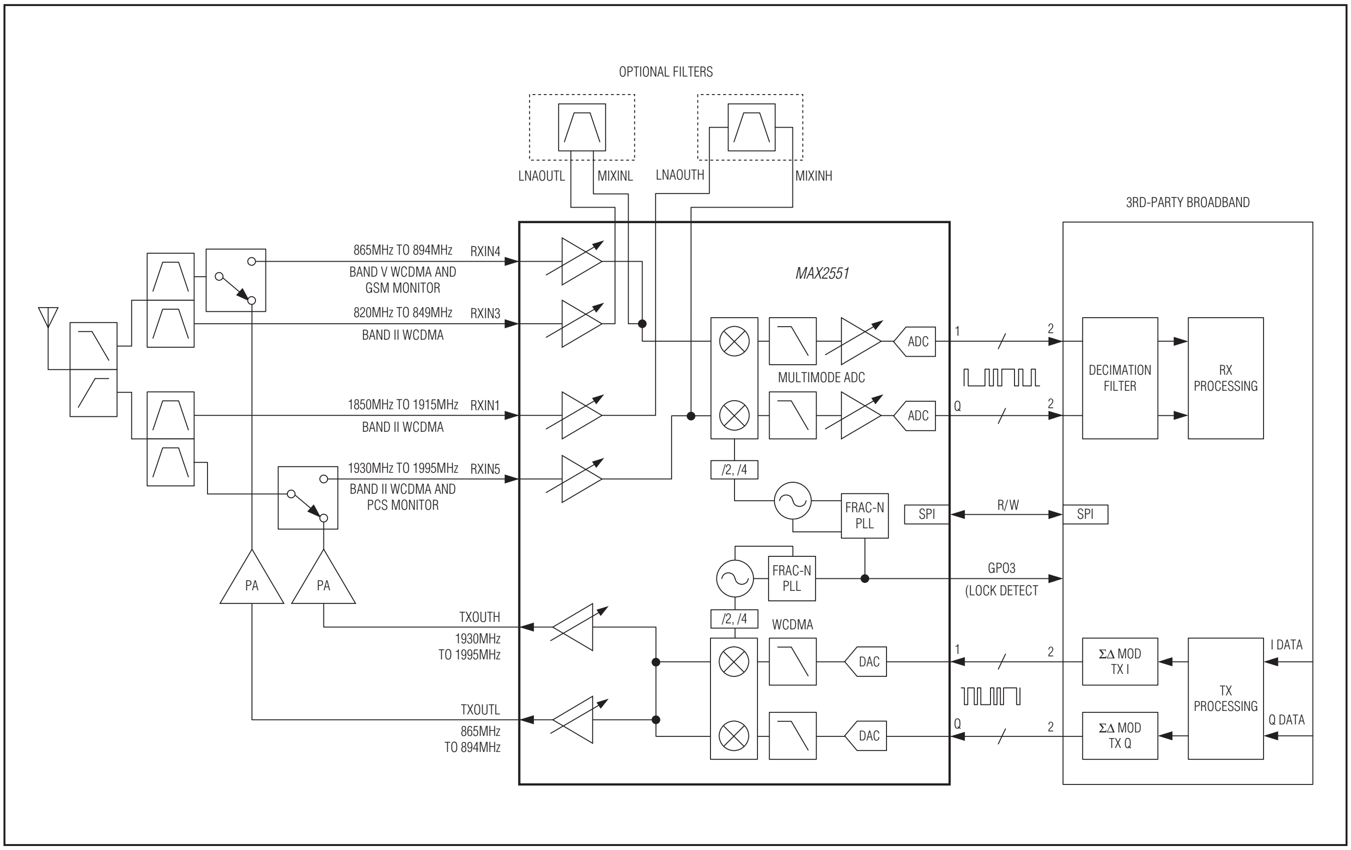
BIT	BIT ID	NAME	DEFINITION	BIT	RXIN1 ONLY	RXIN3 ONLY	RXIN4 ONLY	RXIN5 ONLY	TXH ONLY	TXL ONLY	RX1/TXH FDD	RX3/TXL FDD	RXIN1 IDLE	TXH IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	1	1	1	1	1	1	1	1	1	1	1	1	1
18				18	1	1	1	1	1	1	1	1	1	1	1	1	1
19				19	1	1	1	1	1	1	1	1	1	1	1	1	1
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	1	1	1	1	1	1	1	1	1	1	1	1	1
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0

Applications Information

Layout Considerations

The EV kit and reference design serve as a guide for PCB layout. Keep RF signal lines as short as possible to minimize losses and radiation. Use controlled impedance on all high-frequency traces. The exposed paddle must be soldered evenly to the board's ground plane for proper operation. Use abundant ground vias between RF traces to minimize undesired coupling. Bypass each $V_{CC\_}$ pin to ground with capacitors placed as close as possible to the pin.

Simplified Block Diagram


OPTIONAL FILTERS
LNAOUTL
MIXINL
LNAOUTH
MIXINH
3RD-PARTY BROADBAND
865MHz TO 894MHz
RXIN4
BAND V WCDMA AND
GSM MONITOR
820MHz TO 849MHz
RXIN3
BAND II WCDMA
1850MHz TO 1915MHz
RXIN1
BAND II WCDMA
1930MHz TO 1995MHz
RXIN5
BAND II WCDMA AND
PCS MONITOR
PA
PA
TXOUTH
1930MHz
TO 1995MHz
TXOUTL
865MHz
TO 894MHz
MAX2551
MULTIMODE ADC
ADC
ADC
/2, /4
FRAC-N
PLL
FRAC-N
PLL
/2, /4
WCDMA
DAC
DAC
SPI
1
Q
2
2
R/W
GPO3
(LOCK DETECT
1
Q
2
2
DECIMATION
FILTER
RX
PROCESSING
SPI
ΣΔ MOD
TX I
ΣΔ MOD
TX Q
TX
PROCESSING
I DATA
Q DATA

Ordering Information

PART	BAND	TEMP RANGE	PIN-PACKAGE
MAX2551ETN+	II and V	-40°C to +85°C	56 TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed paddle.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN	T5677+2	21-0144	90-0043

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—

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