# SPDT SWITCH GaAs MMIC

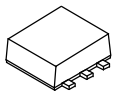
## ■ GENERAL DESCRIPTION

The NJG1608KB2 is a SPDT switch IC featured low insertion loss, medium handling power and high isolation.

The NJG1608KB2 is suitable for switching of Tx/Rx signals at sub-microwave applications. The NJG1608KB2 exhibits wide frequency range from 100MHz to 6.0GHz at low operating voltage of 2.5V, and is operated up to 25dBm at 3.0V operating voltage.

The Pb free FLP6-B2 package is applied.

## ■ PACKAGE OUTLINE

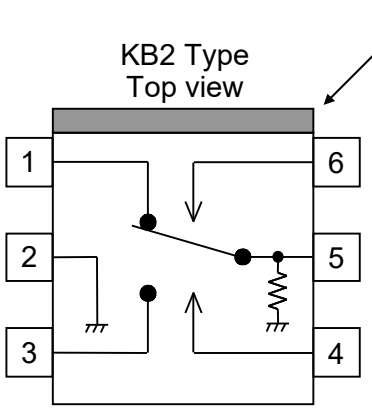


NJG1608KB2

## ■ FEATURES

| | | |
|---|---|---|
| ●Single low voltage control | +2.5~+6.5V | |
| ●Low insertion loss | 0.30dB typ. | @f=2.0GHz |
| | 0.35dB typ. | @f=2.5GHz |
| | 0.60dB typ. | @f=5.85GHz |
| ●High isolation | 29dB typ. | @f=2.0GHz |
| | 30dB typ. | @f=2.5GHz |
| | 18dB typ. | @f=5.85GHz |
| ●Handling power | $P_{-1dB}$=30dBm typ. | @f=2.5GHz, $V_{CTL}$=3.0V |
| ●Ultra-small and ultra-thin package | FLP6-B2 (Package size: 2.0mmx2.1mmx0.75mm typ.) | |

## ■ PIN CONFIGURATION




Pin connection

1.P1
2.GND
3.P2
4.VCTL2
5.PC
6.VCTL1

## ■ TRUTH TABLE

"H"=$V_{CTL\ (H)}$, "L"=$V_{CTL\ (L)}$

| $V_{CTL1}$ | H | L |
|---|---|---|
| $V_{CTL2}$ | L | H |
| PC – P1 | OFF | ON |
| PC – P2 | ON | OFF |

## ■ ABSOLUTE MAXIMUM RATINGS

($T_a$=25°C, $Z_s$=$Z_l$=50Ω)

| PARAMETER | SYMBOL | CONDITIONS | RATINGS | UNITS |
|---|---|---|---|---|
| Input Power | $P_{in}$ | $V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=3.0V | 32 | dBm |
| Control Voltage | $V_{CTL}$ | $V_{CTL\ (H)}$-$V_{CTL\ (L)}$ | 7.5 | V |
| Power Dissipation | $P_D$ | on PCB board | 550 | mW |
| Operating Temp. | $T_{opr}$ | | -40~+85 | °C |
| Storage Temp. | $T_{stg}$ | | -55~+150 | °C |

## ■ ELECTRICAL CHARACTERISTICS

(with application circuit, $V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=3.0V, $Z_S$=$Z_l$=50Ω, $T_a$=25°C)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Operating voltage (LOW) | $V_{CTL\ (L)}$ | | -0.2 | 0 | 0.2 | V |
| Operating voltage (HIGH) | $V_{CTL\ (H)}$ | | 2.5 | 3.0 | 6.5 | V |
| Control current | $I_{CTL}$ | f=2.0GHz | - | 5 | 10 | μA |
| Insertion loss 1 | LOSS1 | f=2.0GHz | - | 0.30 | 0.45 | dB |
| Insertion loss 2 | LOSS2 | f=2.5GHz | - | 0.35 | 0.50 | dB |
| Insertion loss 3 | LOSS3 | f=5.85GHz | | 0.60 | 0.80 | dB |
| Isolation 1 (PC-P1, PC-P2, P1-P2) | ISL1 | f=2.0GHz, | 26 | 29 | - | dB |
| Isolation 2 (PC-P1, PC-P2, P1-P2) | ISL2 | f=2.5GHz, | 27 | 30 | - | dB |
| Isolation 3 (PC-P1, PC-P2, P1-P2) | ISL3 | f=5.85GHz | 16 | 18 | | dB |
| Input power at 1dB compression point 1 | $P_{-1dB}$(1) | f=2.5GHz | 28 | 30 | - | dBm |
| Input power at 1dB compression point 2 | $P_{-1dB}$(2) | f=5.85GHz | 25 | 27 | - | dBm |
| VSWR (PC, P1, P2) | VSWR | f=0.1~5.85GHz, ON State | - | 1.4 | 1.6 | |
| Switching time | $T_{SW}$ | f=0.1~5.85GHz | - | 100 | - | ns |

## ■ TERMINAL INFORMATION

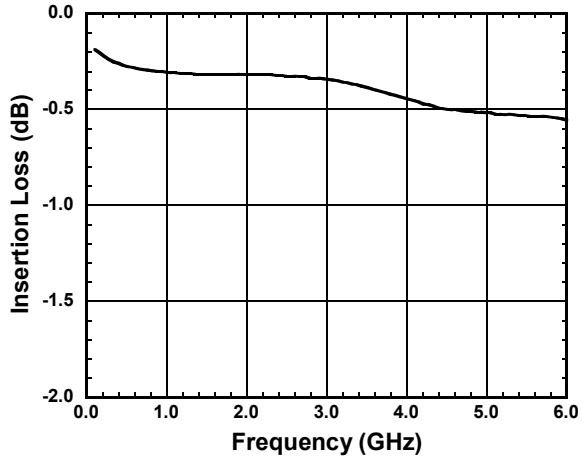
| No. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | P1 | RF port. This port is connected with PC port by controlling 4th pin ($V_{CTL(H)}$) to 2.5~6.5V and 6th pin($V_{CTL(L)}$) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit |
| 2 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 3 | P2 | RF port. This port is connected with PC port by controlling 6th pin ($V_{CTL(H)}$) to 2.5~6.5V and 4th pin($V_{CTL(L)}$) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit. |
| 4 | VCTL2 | Control port 2. The voltage of this port controls PC to P1 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of 6th pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching time delay from 10pF~1000pF range. |
| 5 | PC | Common RF port. In order to block the DC bias voltage of internal circuit, an external capacitor is required. |
| 6 | VCTL1 | Control port 1. The voltage of this port controls PC to P2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of 4th pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching time delay from 10pF~1000pF range. |

## ■ ELECTRICAL CHARACTERISTICS

(0.1~6.0GHz, with application circuit, without DC Blocking Capacitor, Losses of external circuit are excluded.)

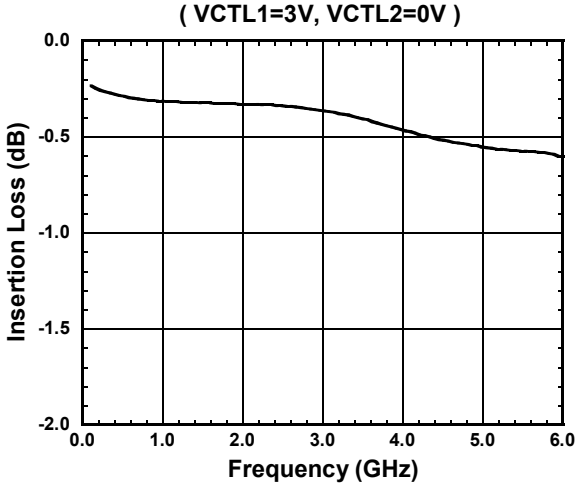
**PC-P1 Insertion Loss vs. Frequency**

**( VCTL1=0V, VCTL2=3V )**



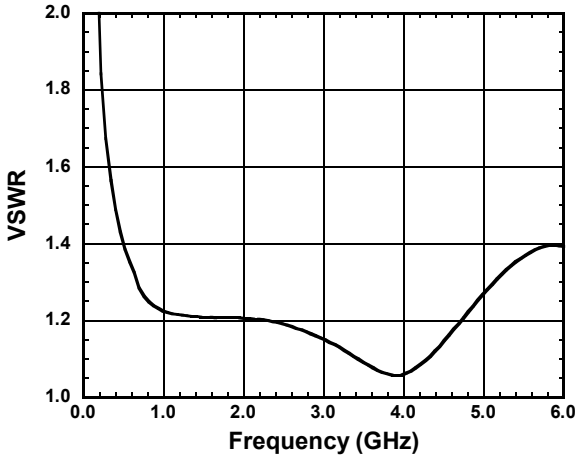

**PC-P2 Insertion Loss vs. Frequency**

**( VCTL1=3V, VCTL2=0V )**



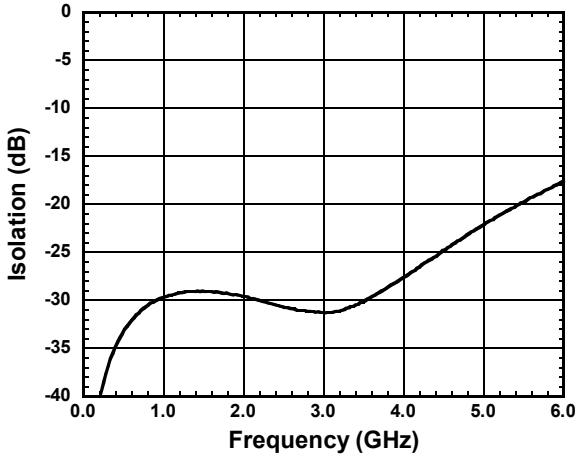

**PC VSWR vs. Frequency**

**( PC-P1 ON, VCTL1=0V, VCTL2=3V )**



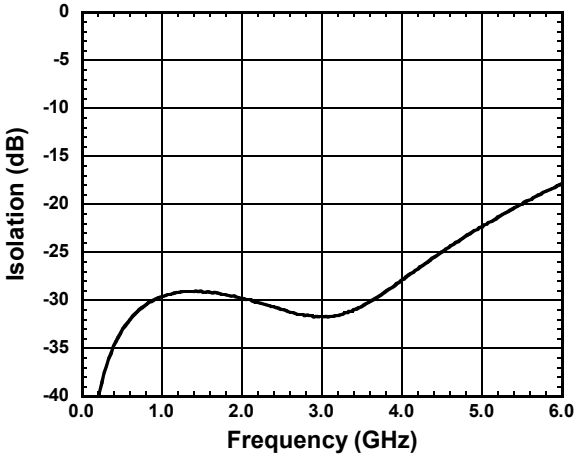

**PC-P1 Isolation vs. Frequency**

**( VCTL1=3V, VCTL2=0V )**




**PC-P2 Isolation vs. Frequency**

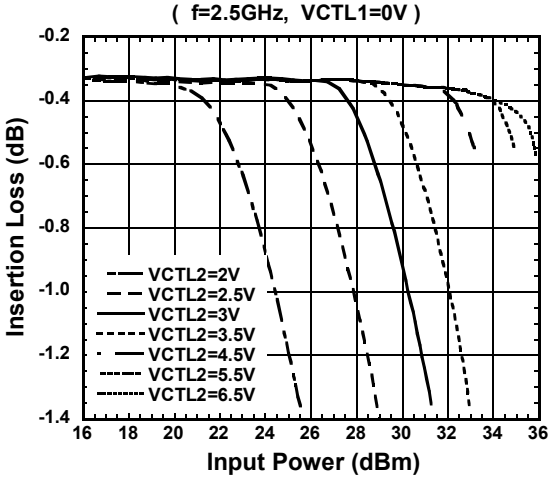
**( VCTL1=0V, VCTL2=3V )**



## ■ ELECTRICAL CHARACTERISTICS

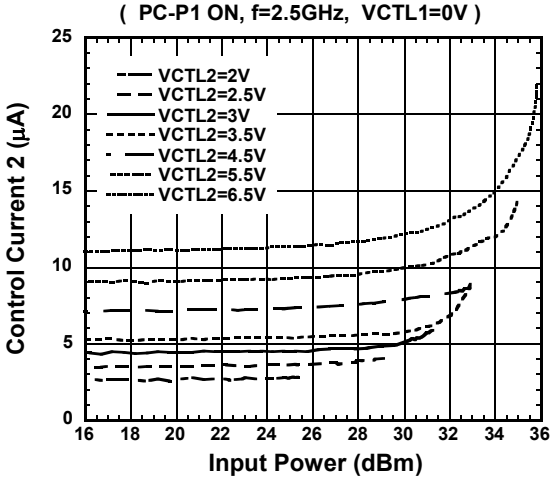
**PC-P1 Insertion Loss vs. Input Power**

**( f=2.5GHz, VCTL1=0V )**



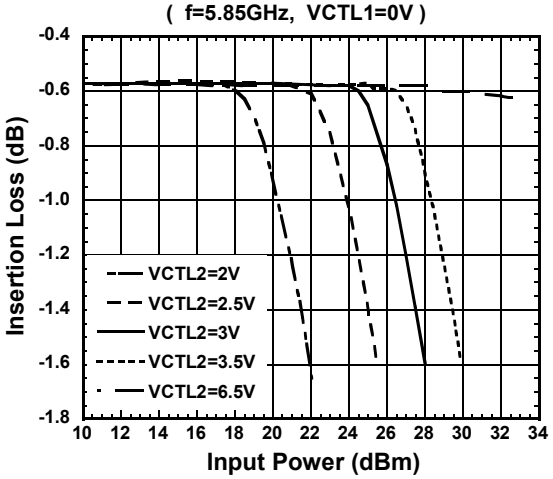

**Control Current 2 vs. Input Power**

**( PC-P1 ON, f=2.5GHz, VCTL1=0V )**



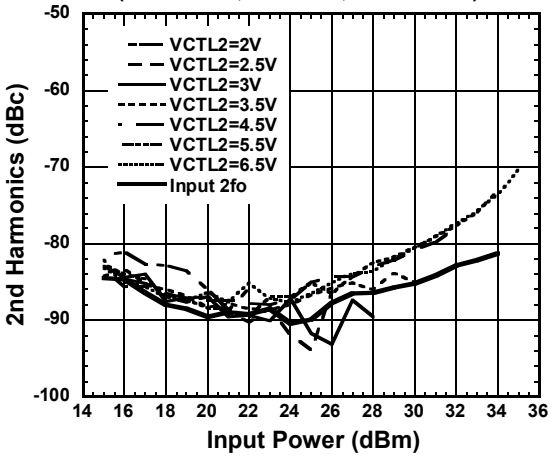

**PC-P1 Insertion Loss vs. Input Power**

**( f=5.85GHz, VCTL1=0V )**



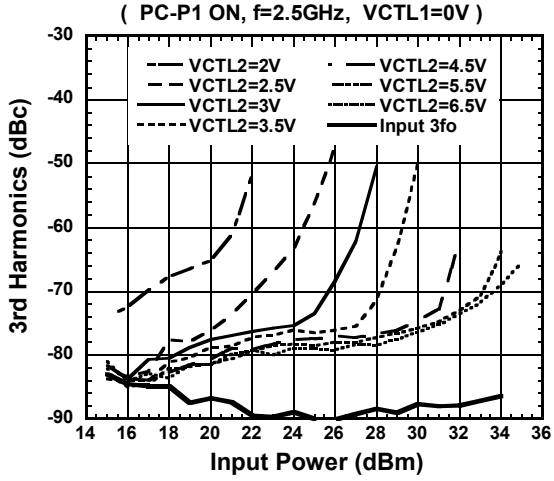

**2nd Harmonics vs. Input Power**

**( PC-P1 ON, f=2.5GHz, VCTL1=0V )**

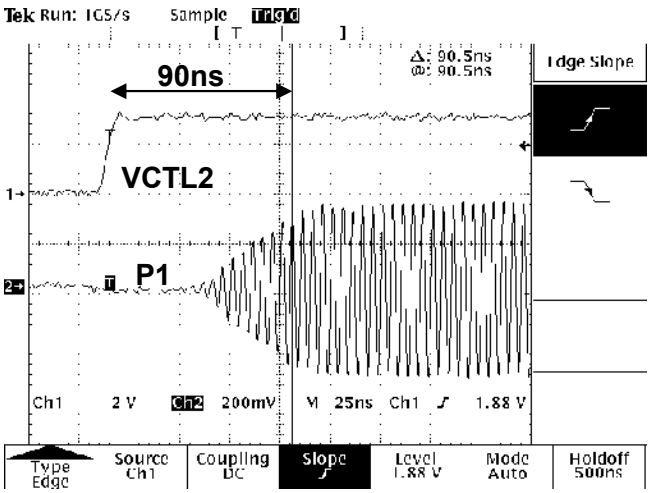


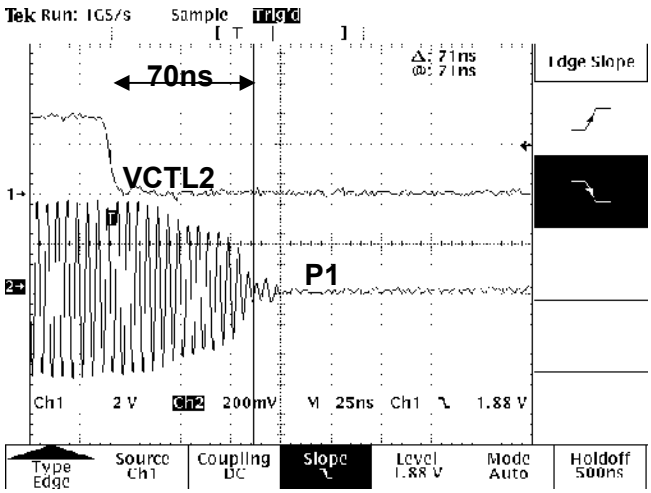

**3rd Harmonics vs. Input Power**

**( PC-P1 ON, f=2.5GHz, VCTL1=0V )**

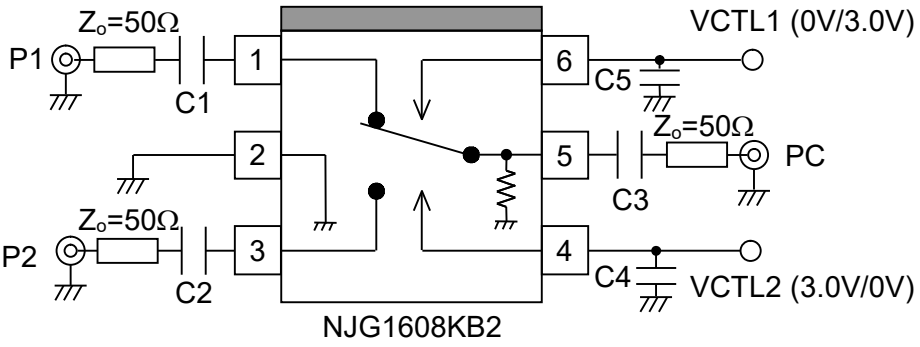


## ■ ELECTRICAL CHARACTERISTICS



## ■ APPLICATION CIRCUIT

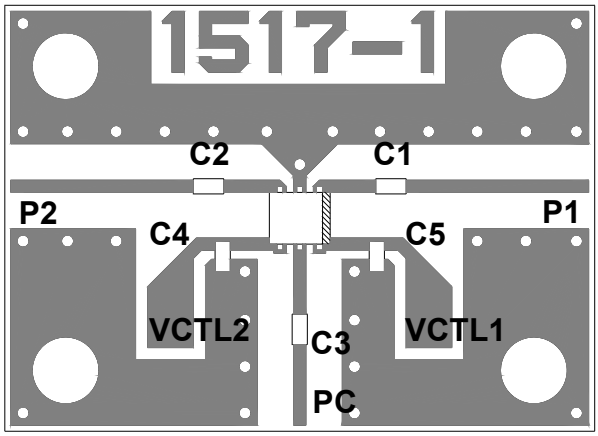



Parts List

| Parts number | List 1 | List 2 | List 3 | Notes |
|---|---|---|---|---|
| | 100~500MHz | 0.5~2.0GHz | 2.0~6.0GHz | |
| C1~C3 | 1000pF | 56pF | 16pF | GRM15 MURATA |
| C4, C5 | 10pF | 10pF | 10pF | GRM15 MURATA |

## ■ TEST PCB LAYOUT

(TOP VIEW)

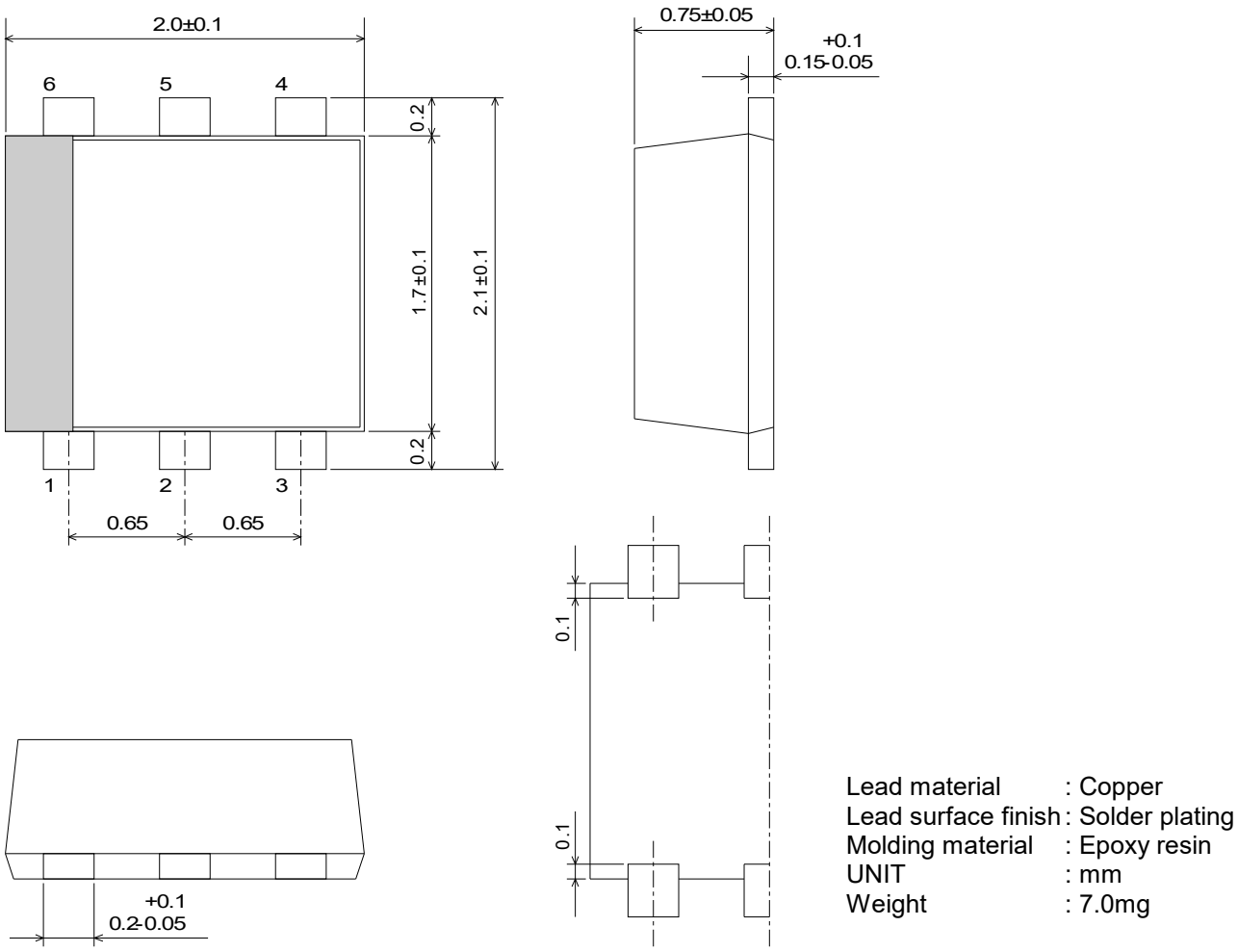



PCB SIZE=19.4x14.0mm
PCB: FR-4, t=0.2mm
CAPACITOR: size 1005
STRIPLINE WIDTH=0.4mm

**PRECAUTIONS**

[1] The DC blocking capacitors have to be placed at RF terminal of P1, P2 and PC. Please choose appropriate capacitance values to the application frequency.
[2] To reduce stripline influence on RF characteristics, please locate bypass capacitors (C4, C5) close to each terminal.
[3] For good isolation, the GND terminal ($2^{nd}$ pin) must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.

## ■PACKAGE OUTLINE (FLP6-B2)




| | |
|---|---|
| Lead material | : Copper |
| Lead surface finish | : Solder plating |
| Molding material | : Epoxy resin |
| UNIT | : mm |
| Weight | : 7.0mg |

**Cautions on using this product**

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

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    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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