TPD2S300 USB Type C Short-to-VBUS and IEC ESD Protector for the CC Pins

1 Features

- 2 Channels of Short-to-V_{BUS} Overvoltage Protection (CC1, CC2): 24-V_{DC} Tolerant
- 2 Channels of IEC 61000-4-2 ESD Protection (CC1, CC2)
- Low quiescent current: 3.23 µA (Typical), V_{PWR}, V_M = 3.3 V
- CC1, CC2 Overvoltage Protection FETs 200 mA capable for passing V_{CONN} power
- CC Dead Battery Resistors Integrated for handling dead battery use case in mobile devices
- 1.4-mm × 1.4-mm WCSP Package

2 Applications

- Smartphones
- Laptop PC
- Tablets
- Wall Adaptors
- Power Banks
- Power Drills

3 Description

The TPD2S300 is a single chip USB Type-C port protection solution that provides 20-V Short-to-V_{BUS} overvoltage and IEC ESD protection for the CC1 and CC2 pins.

Since the release of the USB Type-C connector, many products and accessories for USB Type-C have been released which do not meet the USB Type-C specification. One example of this is USB Type-C Power Delivery adaptors that start out with 20 V on the V_{BUS} line. Another concern for USB Type-C is that mechanical twisting and sliding of the connector could short pins due to the close proximity they have in this small connector. This can cause 20-V V_{BUS} to be shorted to the CC pins. Also, due to the close proximity of the pins in the Type-C connector, there is a heightened concern that debris and moisture is going to cause the 20-V V_{BUS} pin to be shorted to the CC pins.

These non-ideal equipments and mechanical events make it necessary for the CC pins to be 20-V tolerant, even though they only operate at 5 V or lower. The TPD2S300 enables the CC pins to be 20-V tolerant without interfering with normal operation by providing overvoltage protection on the CC pins. The device places high voltage FETs in series on the CC lines. When a voltage above the OVP threshold is detected on these lines, the high voltage switches are opened up, isolating the rest of the system from the high voltage condition present on the connector.

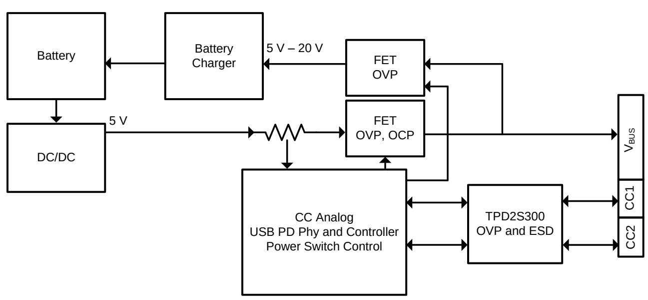
Finally, most systems require IEC61000-4-2 system level ESD protection for their external pins. The TPD2S300 integrates IEC 61000-4-2 ESD protection for the CC1 and CC2 pins, removing the need to place high voltage TVS diodes externally on the connector.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD2S300	WCSP (9)	1.40 mm × 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



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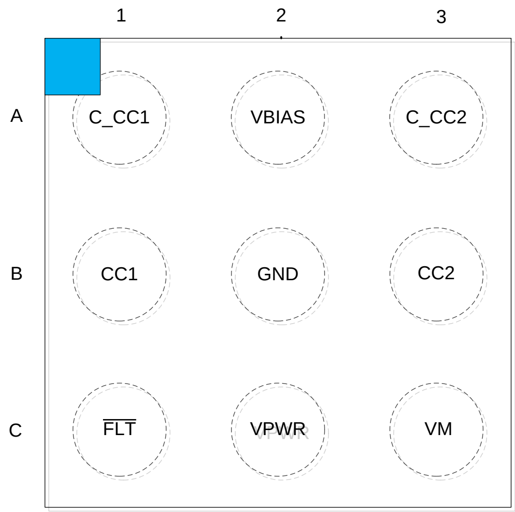
4 Revision History

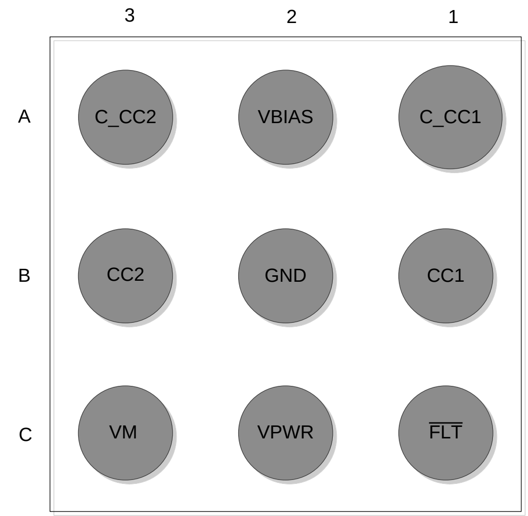
DATE	REVISION	NOTES
April 2017	*	Initial release.

5 Pin Configuration and Functions

YFF Package
9-Pin WCSP
Top Side Marking View



YFF Package
9-Pin WCSP
Bottom, Bump View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	C_CC1	I/O	Connector side of the CC1 OVP FET. Connect to either CC pin of the USB Type-C connector
A2	VBIAS	Power	Pin for ESD support capacitor. Place a 0.1-µF capacitor on this pin to ground
A3	C_CC2	I/O	Connector side of the CC2 OVP FET. Connect to either CC pin of the USB Type-C connector
B1	CC1	I/O	System side of the CC1 OVP FET. Connect to either CC pin of the CC/PD controller
B2	GND	GND	Ground
B3	CC2	I/O	System side of the CC2 OVP FET. Connect to either CC pin of the CC/PD controller
C1	$\overline{\text{FLT}}$	O	Open drain for fault reporting
C2	VPWR	Power	2.7 V–4.5 V power supply
C3	VM	I	Voltage mode pin. Place 2.7 V–4.5 V on pin to operate for CC, PD, and FRS. Place 8.7 V–22 V on pin to operate the device in low resistance mode as well

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_I	Input voltage	V_{PWR}	–0.3	5.5	V
		VM	–0.3	28	V
V_O	Output voltage	$\overline{FLT}$	–0.3	6	V
		VBIAS	–0.3	24	V
V_{IO}	I/O voltage	CC1, CC2	–0.3	6	V
		C_CC1, C_CC2	–0.3	24	V
T_A	Operating free air temperature		–40	85	°C
T_J	Operating junction temperature		–40	105	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 ESD Ratings—IEC Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, C_CC1, C_CC2	Contact discharge	±8000	V
			Air-gap discharge	±15000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage	V_{PWR}	2.7	3.3	4.5	V
		VM	2.7		22	V
V_O	Output voltage	$\overline{FLT}$ Pull-up resistor power rail	2.7		5.5	V
V_{IO}	I/O voltage	CC1, CC2, C_CC1, C_CC2	0		5.5	V
I_{VCONN}	V_{CONN} current	Current flowing from CCx to C_CCx			200	mA
	External components[1]	$\overline{FLT}$ Pull-up resistance	1.7		300	kΩ
		VBIAS capacitance[2]		0.1		µF
		V_{PWR} capacitance, V_M capacitance	0.3	1		µF

(1) For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented must be within the minimum and maximums listed in the table.
(2) The VBIAS pin requires a minimum 35-V_{DC} rated capacitor. A 50-V_{DC} rated capacitor is recommended to reduce capacitance derating. See the *VBIAS Capacitor Selection* section for more details on VBIAS capacitor selection.

6.5 Thermal Information

THERMAL METRIC (1)		TPD2S300 YFF (WCSP) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CC OVP SWITCHES						
$R_{ON\_VCONN\_1}$	On resistance of CC OVP FETs VCONN operation	VM = 8.7 V, CCx = 3 V, I_{CCx} = 0.6 A, –40°C ≤ T_J ≤ 105°C			0.560	Ω
$R_{ON\_VCONN\_2}$	On resistance of CC OVP FETs VCONN operation	VM = 8.7 V, CCx = 4.87 V, I_{CCx} = 0.2 A, –40°C ≤ T_J ≤ 105°C			0.608	Ω
R_{ON_FRS}	On resistance of CC OVP FETs fast role swap operation	VM = 2.7 V, CCx = 0.49 V, I_{CCx} = 30 mA, –40°C ≤ T_J ≤ 105°C			1.3	Ω
$R_{ON\_CC\_ANA}$	On resistance of CC OVP FETs CC analog operation	VM = 2.7 V, CCx = 2.45 V, I_{CCx} = 400 µA, –40°C ≤ T_J ≤ 105°C			18.7	Ω
R_{ON_PD}	On resistance of CC OVP FETs CC USB-PD operation	VM = 2.7 V, CCx = 1.2 V, I_{CCx} = 250 µA, –20°C ≤ T_J ≤ 105°C			13	Ω
$R_{ONFLAT\_VCONN\_1}$	On resistance flatness of CC OVP FETs VCONN operation	VM = 8.7 V, sweep CCx from 0 V to 5.5 V, measure the difference in resistance. I_{CCx} = 0.2 A, –40°C ≤ T_J ≤ 105°C			0.2	Ω
C_{ON_CC}	Equivalent on capacitance for CC pins	Capacitance from C_CCx or CCx to GND when device is powered. V_{C_CCx}/V_{CCx} = 0 V to 1.2 V, f = 400 kHz, –40°C ≤ T_J ≤ 105°C	30		120	pF
VTH_DB	Threshold voltage of the pull-down FET in series with RD during dead battery	I_C_CCx = 80 uA	0.5	0.9	1.2	V
R_D	Dead battery pull-down resistance (only present when device is unpowered). Effective resistance of R_D and FET in series	V_{PWR} = 0 V, V_{C_CCx} = 2.6 V	4.1	5.1	6.1	kΩ
V_{OVPCC_RISE}	Rising overvoltage protection threshold on C_CCx pins	Place 5.5 V on C_CCx pins. Step up voltage until the $\overline{FLT}$ pin is asserted .–20°C ≤ T_J ≤ 105°C	5.55		6.18	V
V_{OVPCC_HYS}	OVP threshold hysteresis	Place 6.5 V on C_CCx. Step down the voltage on C_CCx until the $\overline{FLT}$ pin is deasserted. Measure the difference between rising and falling OVP thresholds		50		mV
BW_{ON}	On bandwidth single ended (–3dB)	Measure the –3-dB bandwidth from C_CCx to CCx. Single ended measurement, 50-Ω system. Vcm = 0 V to 1.2 V		80		MHz
V_{STBUS_CC}	Short-to-VBUS tolerance on the C_CCx pins	Hot-Plug C_CCx with a 1 meter USB Type C Cable. Place a 30-Ω load on CCx			24	V

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{STBUS\_CC\_CLAMP}$	Short-to-VBUS system-side clamping voltage on the CCx pins	Hot-Plug C_CCx with a 1-meter USB Type C Cable. Hot-plug voltage C_CCx = 2 4V. VPWR = 3.3 V. Place a 30-Ω load on CCx		8		V
POWER SUPPLY AND LEAKAGE CURRENTS						
V_{PWR_UVLO}	V_{PWR} undervoltage lockout threshold	Place 1 V on VPWR and raise the voltage until the CC FETs turn ON	1.9	2.3	2.55	V
$V_{PWR\_UVLO\_HYS}$	V_{PWR} UVLO hysteresis	Place 3 V on VPWR and lower the voltage until the CC FETs turn off. Calculate the difference between the rising and falling UVLO threshold	50	100	200	mV
I_{VPWR_1S}	VPWR quiescent current for 1S battery	VPWR = 3.3 V, VM = 3.3 V, C_CCx = 3.6 V, –40°C ≤ T_J ≤ 105°C		3.23	7	µA
I_{VM_1S}	VM quiescent current for 1S battery	VPWR = 3.3 V, VM = 3.3 V, C_CCx = 3.6 V, –40°C ≤ T_J ≤ 105°C			1	µA
$I_{VPWR\_1S\_Max}$	VPWR quiescent current for 1S battery max	VPWR = 4.5 V, VM = 4.5 V, C_CCx = 3.6 V, –40°C ≤ T_J ≤ 105°C			12	µA
$I_{VM\_1S\_Max}$	VM quiescent current for 1S battery max	VPWR = 4.5 V, VM = 4.5 V, C_CCx = 3.6 V, –40°C ≤ T_J ≤ 105°C			1	µA
I_{VPWR_3S}	VPWR quiescent current for 3S battery	VPWR = 3.6 V, VM = 13.5 V, C_CCx = 3.6 V, –40°C ≤ T_J ≤ 105°C			8	µA
I_{VM_3S}	VM quiescent current for 3S battery	VPWR = 3.6 V, VM = 13.5 V, C_CCx = 3.6 V, –40°C ≤ T_J ≤ 105°C			3.5	µA
I_{VPWR_4S}	VPWR quiescent current for 4S battery	VPWR = 3.6 V, VM = 18 V, C_CCx = 3.6 V, –40°C ≤ T_J ≤ 105°C			8	µA
I_{VM_4S}	VM quiescent current for 4S battery	VPWR = 3.6 V, VM = 18 V, C_CCx = 3.6 V, –40°C ≤ T_J ≤ 105°C			4.5	µA
I_{CC_LEAK}	Leakage current for CC pins when device is powered	VPWR = 3.3 V, VM = 3.3 V, VC_CCx = 3.6 V, CCx pins are floating, measure leakage into C_CCx pins. Result must be same if CCx side is biased and C_CCx is left floating			5	µA
$I_{C\_CC\_LEAK\_OVP}$	Leakage current for C_CCx pins when device is in OVP	VPWR = VM = 0 V or 3.3 V, VC_CCx = 24 V, CCx = 0 V, measure leakage into C_CCx pins			1500	µA
$I_{CC\_LEAK\_OVP}$	Leakage current for CCx pins when device is in OVP	VPWR = VM = 0 V or 3.3 V, VC_CCx = 24 V, CCx = 0 V, measure leakage flowing out of CCx pins			40	µA
$\overline{\text{FLT}}$ PIN						
V_{OL}	Low-level output voltage for $\overline{\text{FLT}}$ pin	IOL = 3 mA. Measure the voltage at the $\overline{\text{FLT}}$ pin			0.4	V

6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
POWER-ON AND POWER-OFF TIMINGS					
t_{ON}	Time from crossing rising VPWR UVLO until CC OVP FETs are on. VPWR slew rate = 0.347 V/µs			200	µs
dV_{PWR_OFF}/dt	Minimum slew rate allowed to guarantee CC FETs turn off during a power off	–0.5			V/µs
OVERVOLTAGE PROTECTION					
$t_{OVP\_RESPONSE\_CC}$	OVP response time on the CC pins. Time from OVP asserted until OVP FETs turn off. Hot-Plug C_CCx to 24 V with a 1-m cable. C_CCx slew rate = 4 V/ns. Place a 30-Ω on CCx		145		ns
$t_{OVP\_RECOVERY\_CC}$	OVP recovery time on the CC pins. Time from OVP removal until FET turns back on.VM = 10.8 V. Step C_CCx down from 6.3 V to 3.3 V at a 0.343-V/µs slew rate		30		µs
$t_{OVP\_RECOVERY\_CC}$	OVP recovery time on the CC pins. Time from OVP removal until FET turns back on.VM = 3.3 V. Step C_CCx down from 6.3 V to 0.49 V at a 0.321-V/µs slew rate		200		µs
$t_{OVP\_FLT\_ASSERTION}$	Time from OVP asserted to $\overline{FLT}$ assertion.$\overline{FLT}$ assertion is when the $\overline{FLT}$ pin reaches 10% of its starting value. C_CCx from 0 V to 6.3 V at a 0.645-V/µs slew rate		1		µs
$t_{OVP\_FLT\_DEASSERTION}$	Time from OVP removal to $\overline{FLT}$ deassertion. $\overline{FLT}$ deassertion is when the $\overline{FLT}$ pin reaches 90% of its final value. C_CCx from 6.3 V to 0 V at a 0.696-V/µs slew rate		20		µs

6.8 Typical Characteristics

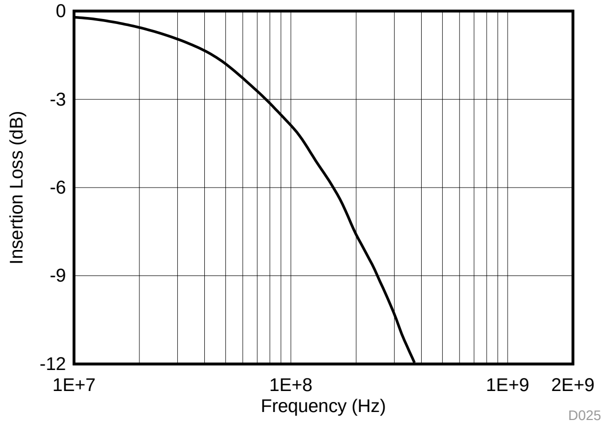


Figure 1. CC S21 BW

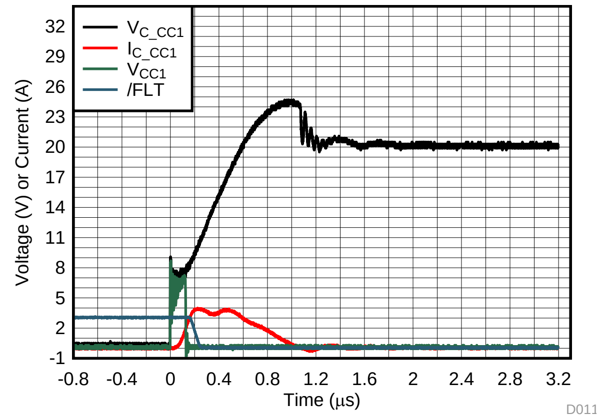


Figure 2. CC Short-to-V_{BUS} 20-V VM = 3.3 V

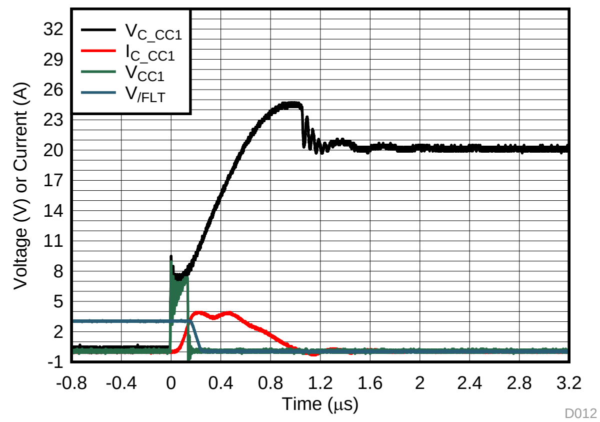


Figure 3. CC Short-to-V_{BUS} 20-V VM = 13 V

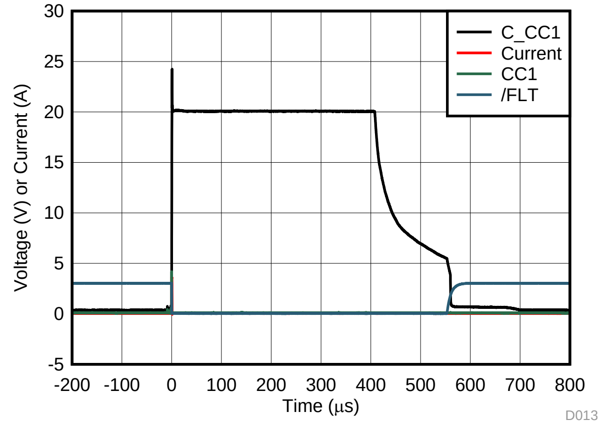


Figure 4. CC OVP Recovery VM = 3.3 V

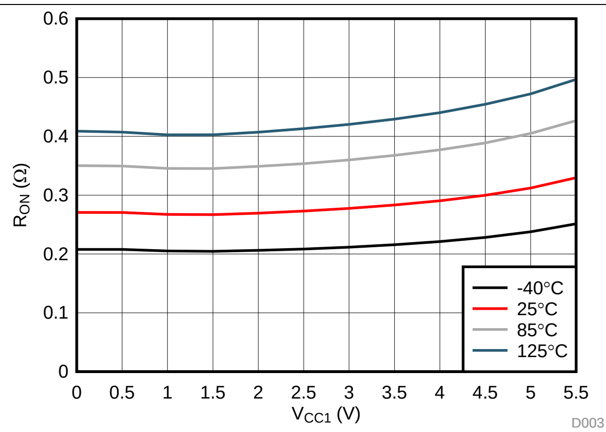


Figure 5. CC R_{ON} Flatness, V_M = 8.7 V

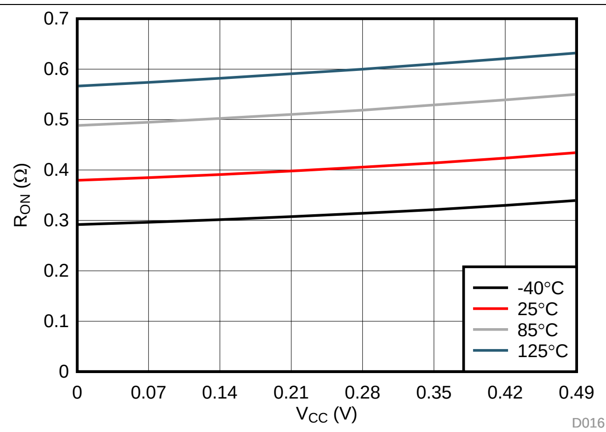


Figure 6. CC R_{ON} Flatness, V_M = 2.7 V

Typical Characteristics (continued)

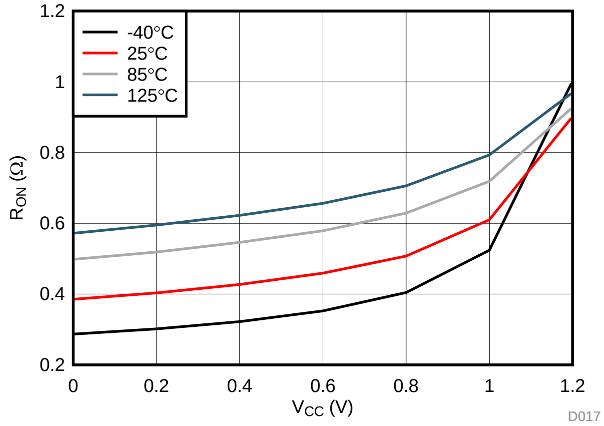


Figure 7. CC R_{ON} Flatness, V_M = 2.7 V

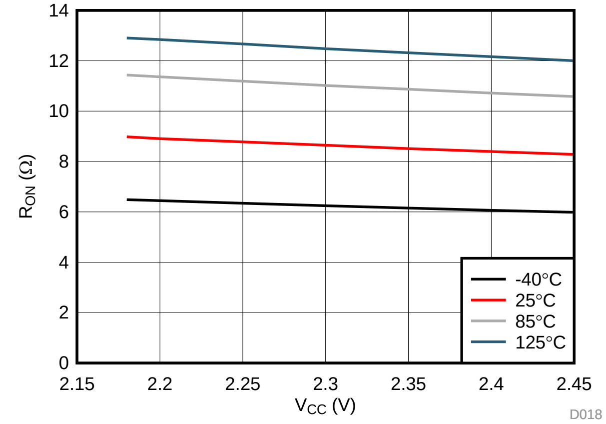


Figure 8. CC R_{ON} Flatness, V_M = 2.7 V

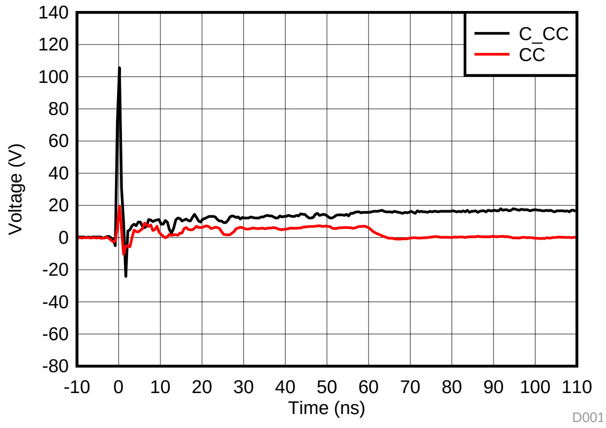


Figure 9. CC IEC 61000-4-2 8-kV Response Waveform

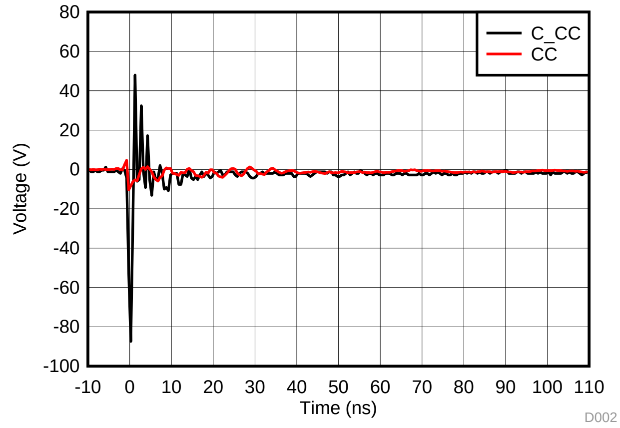


Figure 10. CC IEC 61000-4-2 –8-kV Response Waveform

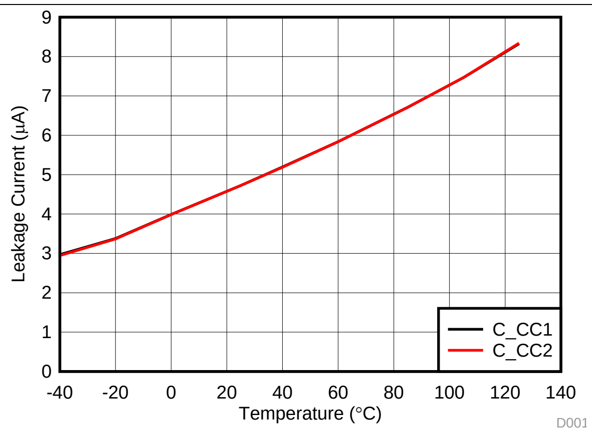


Figure 11. CC Path Leakage Current vs Ambient Temperature at C_CC = 5.5 V

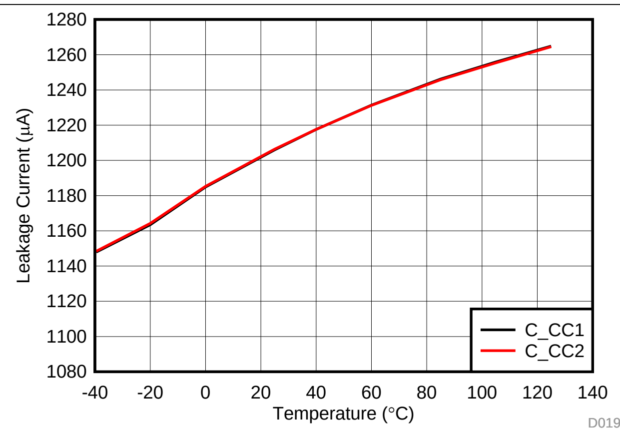


Figure 12. C_CC OVP Leakage Current vs Ambient Temperature at C_CC = 24 V

Typical Characteristics (continued)

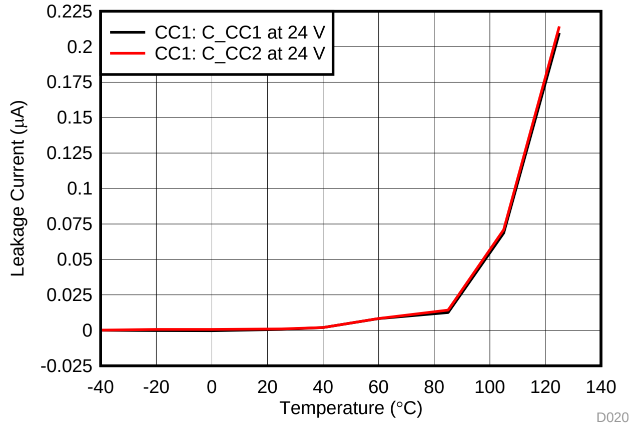


Figure 13. CC OVP Leakage Current vs Ambient Temperature at C_CC = 24 V

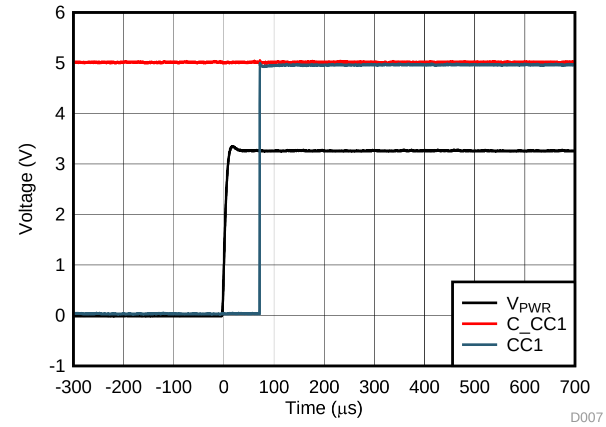


Figure 14. CC FET Turnon Timing

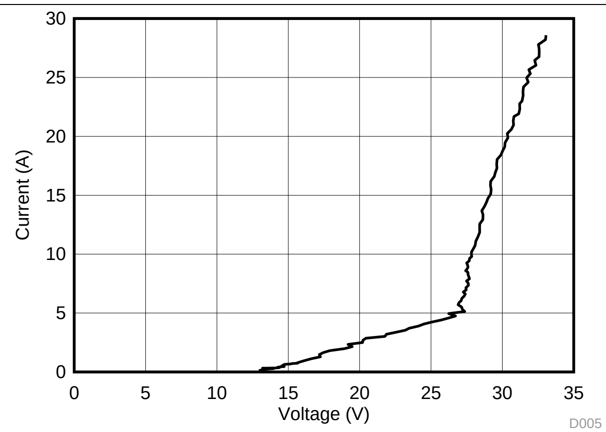


Figure 15. C_CC TLP Curve Unpowered

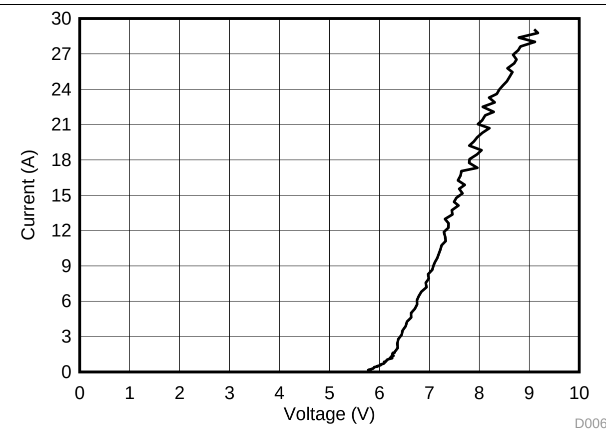


Figure 16. CC TLP Curve Unpowered

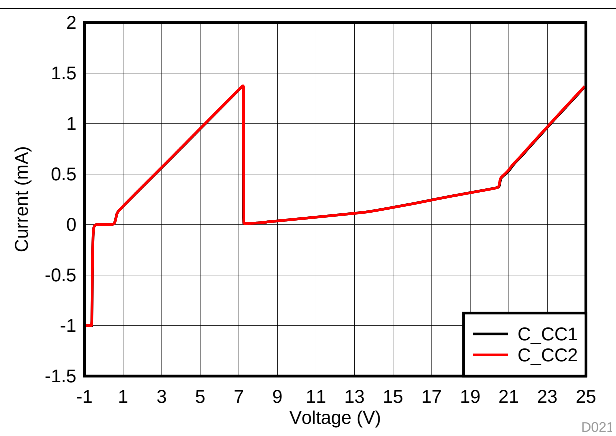


Figure 17. CC IV Curve

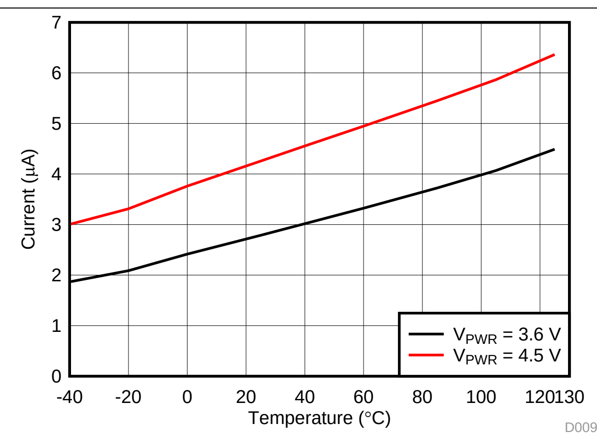


Figure 18. V_{PWR} Supply Leakage vs Ambient Temperature With C_CC Floating or GND

Typical Characteristics (continued)

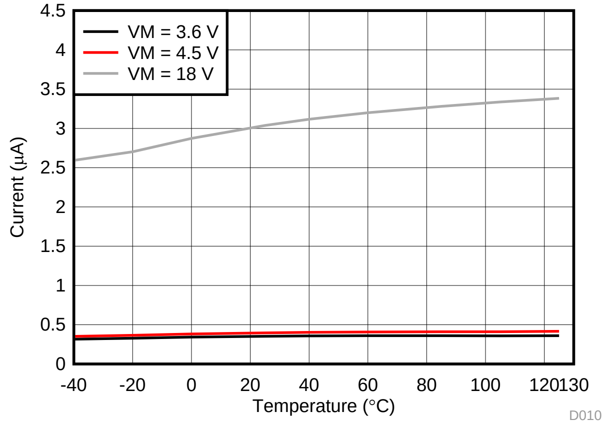


Figure 19. V_M Supply Leakage vs Ambient Temperature With C_CC Floating or GND

7 Detailed Description

7.1 Overview

The TPD2S300 is a low quiescent current, single chip USB Type-C port protection solution that provides 24-V Short-to-V_{BUS} overvoltage and IEC ESD protection. Due to the small pin pitch of the USB Type-C connector and non-compliant USB Type-C cables and accessories, the V_{BUS} pins can get shorted to the CC pins inside the USB Type-C connector. Because of this Short-to-V_{BUS} event, the CC pins need to be short-to-V_{BUS} tolerant, to support protection on the full USB PD voltage range. Even if a device does not support 20-V operation on V_{BUS}, non complaint adaptors can start out with 20-V V_{BUS} condition, making it necessary for any USB Type-C device to support 20-V protection. Although the USB-PD specification has a maximum VBUS voltage of 21.5 V, non-complaint adaptors could go outside this maximum. Therefore, the TPD2S300 integrates two channels of 24-V Short-to-V_{BUS} overvoltage protection for the CC1 and CC2 pins of the USB Type-C connector.

Additionally, IEC 61000-4-2 system level ESD protection is required in order to protect a USB Type-C port from ESD strikes generated by end product users. The TPD2S300 integrates two channels of IEC61000-4-2 ESD protection for the CC1 and CC2 pins of the USB Type-C connector. Additionally, high voltage IEC ESD protection that is at least 22-V DC tolerant is required for the CC lines in order to simultaneously support IEC ESD and Short-to-V_{BUS} protection (although 24-V DC tolerant is recommended, which the TPD2S300 integrates); there are not many discrete market solutions that can provide this kind of protection. This high-voltage IEC ESD diode is what the TPD2S300 integrates, specifically designed to guarantee it works in conjunction with the overvoltage protection FETs inside the device. This sort of solution is very hard to generate with discrete components.

7.2 Functional Block Diagram

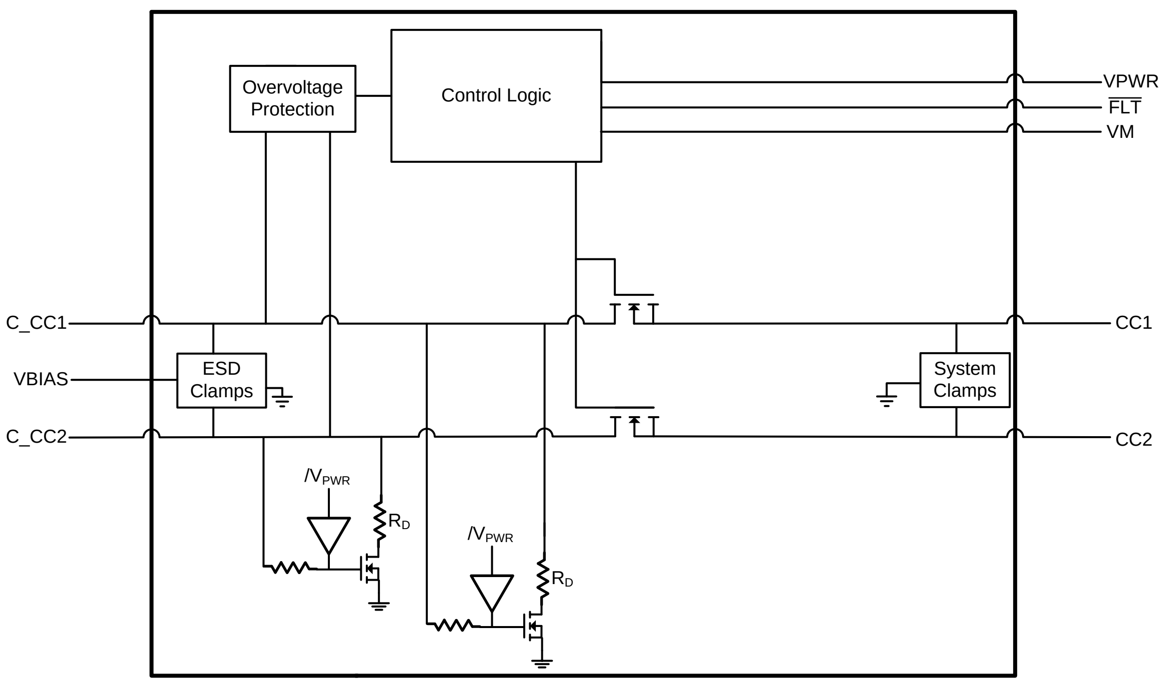


Figure 20. TPD2S300

7.3 Feature Description

7.3.1 2-Channels of Short-to-V_{BUS} Overvoltage Protection (CC1, CC2 Pins): 24-V_{DC} Tolerant

The TPD2S300 provides 2-channels of Short-to-V_{BUS} Overvoltage Protection for the CC1 and CC2 pins of the USB Type-C connector. The TPD2S300 is able to handle 24-V DC on its C_CC1 and C_CC2 pins. This is necessary because according to the USB PD specification, with V_{BUS} set for 20-V operation, the V_{BUS} voltage is allowed to legally swing up to 21 V, and 21.5 V on voltage transitions from a different USB PD V_{BUS} voltage. The TPD2S300 builds in tolerance up to 24-V_{BUS} to provide margin above this 21.5 V specification to be able to support USB PD adaptors that may break the USB PD specification.

When a short-to-V_{BUS} event occurs, ringing happens due to the RLC elements in the hot-plug event. With very low resistance in this RLC circuit, ringing up to twice the settling voltage can appear on the connector. More than 2x ringing can be generated if any capacitor on the line derates in capacitance value during the short-to-V_{BUS} event. This means that more than 44 V could be seen on a USB Type-C pin during a Short-to-V_{BUS} event. The TPD2S300 has built in circuit protection to handle this ringing. The diode clamps used for IEC ESD protection also clamp the ringing voltage during the short-to-V_{BUS} event to limit the peak ringing to around 30 V. Additionally, the overvoltage protection FETs integrated inside the TPD2S300 are 30-V tolerant, therefore being capable of supporting the high voltage ringing waveform that is experienced during the short-to-V_{BUS} event. The well designed combination of voltage clamps and 30-V tolerant OVP FETs insures the TPD2S300 can handle Short-to-V_{BUS} hot-plug events with hot-plug voltages as high as 24-V_{DC}.

The TPD2S300 has an extremely fast turnoff time of 145 ns typical. Furthermore, additional voltage clamps are placed after the OVP FET on the system side (CC1, CC2) pins of the TPD2S300, to further limit the voltage and current that is exposed to the USB Type-C CC/PD controller during the 145 ns interval while the OVP FET is turning off. The combination of connector side voltage clamps, OVP FETs with extremely fast turnoff time, and system side voltage clamps all work together to insure the level of stress seen on the CC1 and CC2 pin during a short-to-V_{BUS} event is comparable to an HBM ESD event. This is done by design, as any USB Type-C CC/PD controller has built in HBM ESD protection.

7.3.2 2-Channels of IEC61000-4-2 ESD Protection (CC1, CC2 Pins)

The TPD2S300 integrates 2-Channels of IEC 61000-4-2 system level ESD protection for the CC1 and CC2 pins of the USB Type-C connector. USB Type-C ports on end-products need system level IEC ESD protection in order to provide adequate protection for the ESD events that the connector can be exposed to from end users. High-voltage IEC ESD protection that is 24-V DC tolerant is required for the CC lines in order to simultaneously support IEC ESD and Short-to-V_{BUS} protection; there are not many discrete market solutions that can provide this kind of protection. The TPD2S300 integrates this type of high-voltage ESD protection so a system designer can meet both IEC ESD and Short-to-V_{BUS} protection requirements in a single device.

7.3.3 Low Quiescent Current: 3.23 µA (Typical), V_{PWR}, V_M = 3.3 V

The TPD2S300 is designed with a very low quiescent current of 3.23 µA (typical) when V_{PWR} = 3.3 V and V_M = 3.3 V. The TPD2S300 is designed to have a very low quiescent current to support applications like smart-phones where device battery life is crucial. See the *Electrical Characteristics* table for complete range of quiescent currents for different V_{PWR} and V_M voltages.

7.3.4 CC1, CC2 Overvoltage Protection FETs 200 mA Capable for Passing V_{CONN} Power

The CC pins on the USB Type-C connector serve many functions; one of the functions is to be a provider of power to active cables. Active cables are required when desiring to pass greater than 3 A of current on the V_{BUS} line or when the USB Type-C port uses the super-speed lines (TX1+, TX2–, RX1+, RX1–, TX2+, TX2–, RX2+, RX2–). When CC is configured to provide power, it is called V_{CONN}. V_{CONN} is a DC voltage source in the range of 3 V–5.5 V. If supporting V_{CONN}, a V_{CONN} provider must be able to provide 1 W of power to a cable; this translates into a current range of 200 mA at 5-V V_{CONN}. Therefore, the TPD2S300 has been designed to handle 200 mA of DC current and to have an RON low enough to provide a specification compliant V_{CONN} voltage to the active cable.

7.3.5 CC Dead Battery Resistors Integrated for Handling Dead Battery Use Case in Mobile Devices

An important feature of USB Type-C and USB PD is the ability for this connector to serve as the sole power source to mobile devices. With support up to 100 W, the USB Type-C connector supporting USB PD can be used to power a whole new range of mobile devices not previously possible with legacy USB connectors.

Feature Description (continued)

When the USB Type-C connector is the sole power supply for a battery powered device, the device must be able to charge from the USB Type-C connector even when its battery is dead. In order for a USB Type-C power adapter to supply power on V_{BUS}, R_D pull-down resistors must be exposed on the CC pins of the sink device. These R_D resistors are typically included inside a USB Type-C CC/PD controller. However, when the TPD2S300 is used to protect the USB Type-C port, the OVP FETs inside the device isolates these R_D resistors in the CC/PD controller when the mobile device has no power. This is because when the TPD2S300 has no power, the OVP FETs are turned off to guarantee overvoltage protection in a dead battery condition. Therefore, the TPD2S300 integrates high voltage, dead battery R_D pull-down resistors to allow dead battery charging simultaneously with high-voltage OVP protection.

When the TPD2S300 is unpowered, and the R_P pull-up resistor is connected from a power adaptor, this R_P pull-up resistor activates the R_D resistor inside the TPD2S300. This enables V_{BUS} to be applied from the power adaptor even in a dead battery condition. Once power is restored back to the system and back to the TPD2S300 on its VPWR pin, the TPD2S300 removes its R_D pull-down resistor and turns on its OVP FETs within 200 µs. The amount of time the TPD2S300 does not have either its R_D exposed or the PD controller's R_D exposed on the CC lines is even less, around 30µs in the worst case, to minimize the probability the USB-C/PD controller in the source device interprets this as a disconnect from the sink. This way connection remains uninterrupted.

If desiring to power the CC/PD controller during dead battery mode and if the CC/PD Controller is configured as a DRP, it is critical that the TPD2S300 be powered before or at the same time that the CC/PD controller is powered. It is also critical that when unpowered, the CC/PD controller also expose its dead battery resistors. When the TPD2S300 gets powered, it exposes the CC pins of the CC/PD controller within 200 µs. Once the TPD2S300 turns on, the R_D pull-down resistors of the CC/PD controller must be present immediately, in order to guarantee the power adaptor connected to power the dead battery device keeps its V_{BUS} turned on. If the power adaptor sees the CC voltage go high to the SRC.Open region, it can disconnect V_{BUS}. This removes power from the device with its battery still not sufficiently charged, which consequently removes power from the CC/PD controller and the TPD2S300. Then the R_D resistors of the TPD2S300 are exposed again and connect the power adaptor's V_{BUS} to start the cycle over. This creates an infinite loop, never or very slowly charging the mobile device.

If the CC/PD Controller is configured for DRP and has started its DRP toggle before the TPD2S300 turns on, this DRP toggle is unable to guarantee that the power adaptor does not disconnect from the port. Therefore, it is recommended if the CC/PD controller is configured for DRP, that its dead battery resistors be exposed as well, and that they remain exposed until the TPD2S300 turns on. This is typically accomplished by powering the TPD2S300 at the same time as the CC/PD controller when powering the CC/PD controller in dead battery operation.

7.3.6 1.4-mm × 1.4-mm WCSP Package

The TPD2S300 comes in a small, 1.4-mm × 1.4-mm WCSP package, greatly reducing the size of implementing a similar protection solution discretely. Smart-phones and tablets need the smallest package size possible due to the space constraints the PCBs have in these devices.

7.4 Device Functional Modes

Table 1 describes all of the functional modes for the TPD2S300. The "X" in the below table are "do not care" conditions, meaning any value can be present within the absolute maximum ratings of the datasheet and maintain that functional mode.

Table 1. Device Mode Table

Device Mode Table		Inputs			Outputs		
MODE		VPWR	VM	C_CCx	$\overline{FLT}$	CC FETs	Dead Battery Resistors
Normal Operating Conditions	Unpowered	<UVLO	X	X	High-Z	OFF	ON
	Powered on	>UVLO	≥VPWR	<OVP	High-Z	ON	OFF
Fault Conditions	CC overvoltage condition	>UVLO	≥VPWR	>OVP	Low (Fault Asserted)	OFF	OFF

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD2S300 provides 2-channels of Short-to-V_{BUS} overvoltage protection for the CC1 and CC2 pins of the USB Type-C connector, and 2-channels of IEC ESD protection for the CC1 and CC2 pins of the USB Type-C connector. Care must be taken to insure that the TPD2S300 provides adequate system protection as well as insuring that proper system operation is maintained. The following application examples explain how to properly design the TPD2S300 into a USB Type-C system.

8.2 Typical Application

8.2.1 Smart-Phone Application

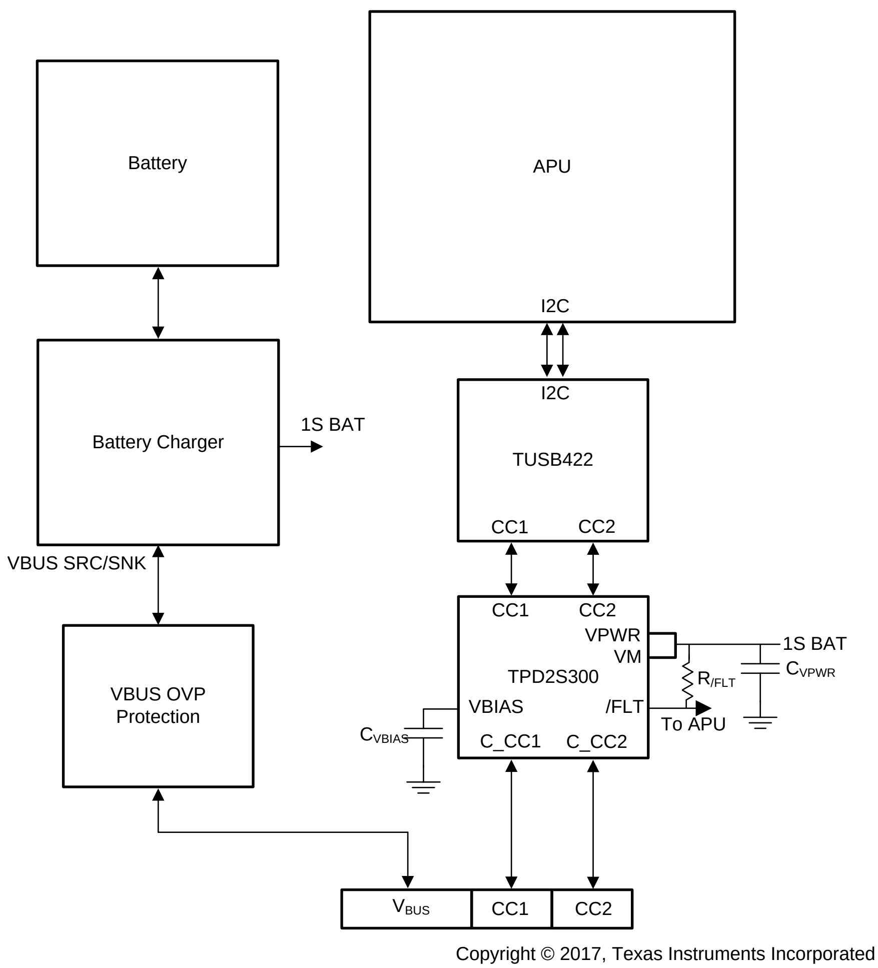


Figure 21. TPD2S300 Typical Application Diagram

Typical Application (continued)

8.2.1.1 Design Requirements

In this application example, we use the TPD2S300 to protect a USB Type-C port in a smart-phone application. In this application, the smart-phone needs USB2.0 support and 20-V, 2-A charging. Because 20 V is required, USB-PD needs to be used in this application to achieve this, as USB Type-C alone cannot support higher than 5 V. In order to add USB-PD operation in a smart-phone application, the TUSB422 is used. This device is a TCPCi that adds the USB Type C and USB-PD physical layer required to run USB PD over the USB Type-C connector. This device can be connected to the APU in the system through I^2C, and the APU can run the USB-PD code.

With USB-C with 20-V PD being used, a Short-to-V_{BUS} event can occur in the system. This short can affect both the CC and SBU pins. However, in this application, since only USB2.0 is required, the SBU pin is not used. Therefore, only CC Short-to-V_{BUS} protection is required to adequately protect the TUSB422 and the system. The CC pins also needs IEC61000-4-2 system level ESD protection. Additionally, with this application being a smart-phone, board space is crucial; a small protection device is required. Therefore, with these application requirements, the TPD2S300 is used, a single-chip solution which integrates all the protection requirements needed for the CC pins in this application.

Table 2 shows the TPD2S300 design parameters for this application.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BUS} nominal operating voltage	20 V
Short-to-V_{BUS} tolerance for the CC pins	24 V
VBIAS nominal capacitance	0.1 µF
Dead battery charging	40 W
TPD2S300 VPWR and VM power source	3.3-V LDO or 1S battery
Quiescent current required for protection device	≤ 20 µA
V_{CONN} requirement	V_{CONN} not required
Maximum ambient temperature requirement	85°C

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 VBIAS Capacitor Selection

As noted in the *Recommended Operating Conditions* table, a minimum of 35-VBUS rated capacitor is required for the VBIAS pin, and a 50-VBUS capacitor is recommended. The VBIAS capacitor is in parallel with the central IEC diode clamp integrated inside the TPD2S300. A forward biased hiding diode connects the VBIAS pin to the C_CCx pins. Therefore, when a Short-to-V_{BUS} event occurs at 20 V, 20-V_{BUS} minus a forward biased diode drop is exposed to the VBIAS pin. Additionally, during the Short-to-V_{BUS} event, ringing can occur almost double the settling voltage of 20 V, allowing a potential 40 V to be exposed to the C_CCx pins. However, the internal IEC clamps limits the voltage exposed to the C_CCx pins to around 30 V. Therefore, at least 35-VBUS capacitor is required to insure the VBIAS capacitor does not get destroyed during Short-to-V_{BUS} events.

A 50-V, X7R capacitor is recommended, however. This is to further improve the derating performance of the capacitors. When the voltage across a real capacitor is increased, its capacitance value derates. The more the capacitor derates, the greater than 2x ringing can occur in the Short-to-V_{BUS} RLC circuit. 50-V X7R capacitors have great derating performance, allowing for the best Short-to-V_{BUS} performance of the TPD2S300.

Additionally, the VBIAS capacitor helps pass IEC 61000-4-2 ESD strikes. The more capacitance present, the better the IEC performance. So the less the VBIAS capacitor derates, the better the IEC performance. Table 3 shows the real capacitors recommended to achieve the best performance with the TPD2S300.

Table 3. Design Parameters

CAPACITOR SIZE	PART NUMBER
0402	CC0402KRX7R9BB104
0603	GRM188R71H104KA93D

8.2.1.2.2 Dead Battery Operation

For this application, we want to support 40-W dead battery operation; when the smart-phone is out of battery, we still want to charge the laptop at 20 V and 2 A. This means that the USB PD Controller must receive power in dead battery mode. This means a dead battery LDO must be present in the system to power the TUSB422 and the APU controlling TUSB422 during dead battery. Or, the system PMIC must be able to provide the 1S battery to the APU and TUSB422 during dead battery conditions.

The TPD2S300s OVP FETs remain OFF when it is unpowered in order to insure in a dead battery situation proper protection is still provided to the PD controller or TCPCi in the system, in this case the TUSB422. However, when the OVP FETs are OFF, this isolates the TUSB422's dead battery resistors from the USB Type-C ports CC pins. A USB Type-C power adaptor must see the R_D pull-down dead battery resistors on the CC pins or it does not turn on V_{BUS} to provide power. Since the TUSB422's dead battery resistors are isolated from the USB Type-C connector's CC pins, the TPD2S300 integrates dead battery resistors on its C_CCx pins. The TPD2S300 exposes these pins when it is unpowered.

Once the power adaptor sees the TPD2S300's dead battery resistors, it applies 5 V on the V_{BUS} pin. This provides power to the dead battery LDO or PMIC, allowing power to be applied to the APU and TUSB422 to turn them ON, and allowing the battery to begin to charge. However, this application requires 40-W charging in dead battery mode, so V_{BUS} at 20 V and 2 A is required. USB PD negotiation is required to accomplish this, so the APU through the TUSB422 needs to be able to communicate on the CC pins. This means the TPD2S300 needs to be turned on in dead battery mode as well so the TUSB422 can be exposed to the CC lines. To accomplish this, it is critical that the TPD2S300 is powered by the same dead battery LDO or battery voltage as the APU and TUSB422 during dead battery. This way, the TPD2S300 is turned ON simultaneously with TUSB422.

It is critical that the TUSB422's dead battery resistors are also active on its CC pins for dead battery operation. Once the TPD2S300 receives power, removes its dead battery resistors and turns on its OVP FETs, R_D pull-down resistors must be present on the CC line in order to guarantee the power adaptor stays connected. If RD is not present and the voltage on CC increases into the SRC.Open range, the power adaptor can interpret this as a port disconnect and remove V_{BUS}.

Once this process has occured, the APU through the TUSB422 can start negotiating with the power adaptor through USB PD for higher power levels, allowing for 40W operation in dead battery mode.

For more information on the TPD2S300 dead battery operation, see the *CC Dead Battery Resistors Integrated for Handling Dead Battery Use Case in Mobile Devices* section in the description section of the datasheet. Also, see Figure 22 for a waveform of the CC line when the TPD2300 is turning on and exposing R_D dead battery resistors to the USB Type-C connector.

8.2.1.2.3 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines. The specification from section 5.8.6 of the *USB PD Specification* is given in Table 4.

Table 4. USB PD cReceiver Specification

NAME	DESCRIPTION	MIN	MAX	UNIT	COMMENT
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system shall have capacitance within this range when not transmitting on the line

Therefore, the capacitance on the CC lines must stay in between 200 pF and 600 pF when USB PD is being used. Therefore, the combination of capacitances added to the system by the TUSB422, the TPD2S300, and any external capacitor must fall within these limits. Table 5 shows that with TUSB422 + TPD2S300, no external capacitor is required to meet the USB-PD specification.

Table 5. CC Line Capacitor Calculation

CC Capacitance	MIN	MAX	UNIT	COMMENT
CC line target capacitance	200	600	pF	From the *USB PD Specification* section (cReceiver, section 5.8.6)
TUSB422 capacitance	200	450	pF	From the TUSB422 Datasheet
TPD2S300 capacitance	30	120	pF	From the *Electrical Characteristics* table
TUSB422 + TPD2S300	230	570	pF	Meets USB PD cReceiver Specification

8.2.1.2.4 FLT Pin Operation

A FLT pin is provided on the TPD2S300 to give the APU the ability to be notified that a Short-to-V_{BUS} event occured. Once a Short-to-V_{BUS} occurs on the C_CCx pins, the FLT pin is asserted in 1 µs (typical) so the PD controller can be notified quickly. If V_{BUS} is being shorted to CC, it is recommended to respond to the event by forcing a detach in the USB PD controller to remove V_{BUS} from the port. Although the USB Type-C port using the TPD2S300 is not damaged, as the TPD2S300 provides protection from these events, the other device connected through the USB Type-C Cable or any active circuitry in the cable can be damaged. Although shutting the V_{BUS} off through a detach does not guarantee it stops the other device or cable from being damaged, it can mitigate any high current paths from causing further damage after the initial damage takes place. Additionally, even if the active cable or other device does have proper protection, the Short-to-V_{BUS} event may corrupt a configuration in an active cable or in the other PD controller, so it is best to detach and reconfigure the port. Therefore, in this application it is recommended that the APU monitor the FLT pin for Short-to-V_{BUS} faults.

8.2.1.2.5 V_{CONN} Operation

In our current application example, V_{CONN} is not required. Therefore, a 3.3-V source or 1S battery can be connected to the VPWR and VM pins of the TPD2S300 and provide adaqute resistance in order to support CC analog and USB PD operation over the CC lines. In fact, the CC OVP FETs resistance specifications are set to optimize the FET size and therefore the TPD2S300 size and still allow proper CC analog and USB PD operation. See the *Electrical Characteristics* table for the specific resistances of the CC OVP FETs.

8.2.1.2.6 Low Quiescent Current

Smart-Phone applications require low quiescent current to meet long battery life specifications to provide the best experience to end-users. The TPD2S300 is designed to have very low quiescent current in order to meet these requirements. The lower the voltage kept on the C_CCx lines, and the lower the voltage kept on the VPWR and VM pins, the lower the quiescent current is on the TPD2S300. If an LDO is used that keeps VPWR and VM limited to 3.3 V, then the maximum quiescent current on VPWR is 7 µA, and the maximum current on VM is 1 µA. If the 1S battery is connected to the VPWR and VM pins, such that the maximum voltage applied to VPWR and VM is 4.5 V, then the maximum quiescent current is going to be 12 µA for VPWR, and VM has 1 µA maximum. Therefore, our application can achieve a very low total quiescent current for protection with the TPD2S300, between 8 µA and 13 µA, depending on how the TPD2S300 is powered. For all details on quiescent current values, see the *Electrical Characteristics* table.

8.2.1.3 Application Curves

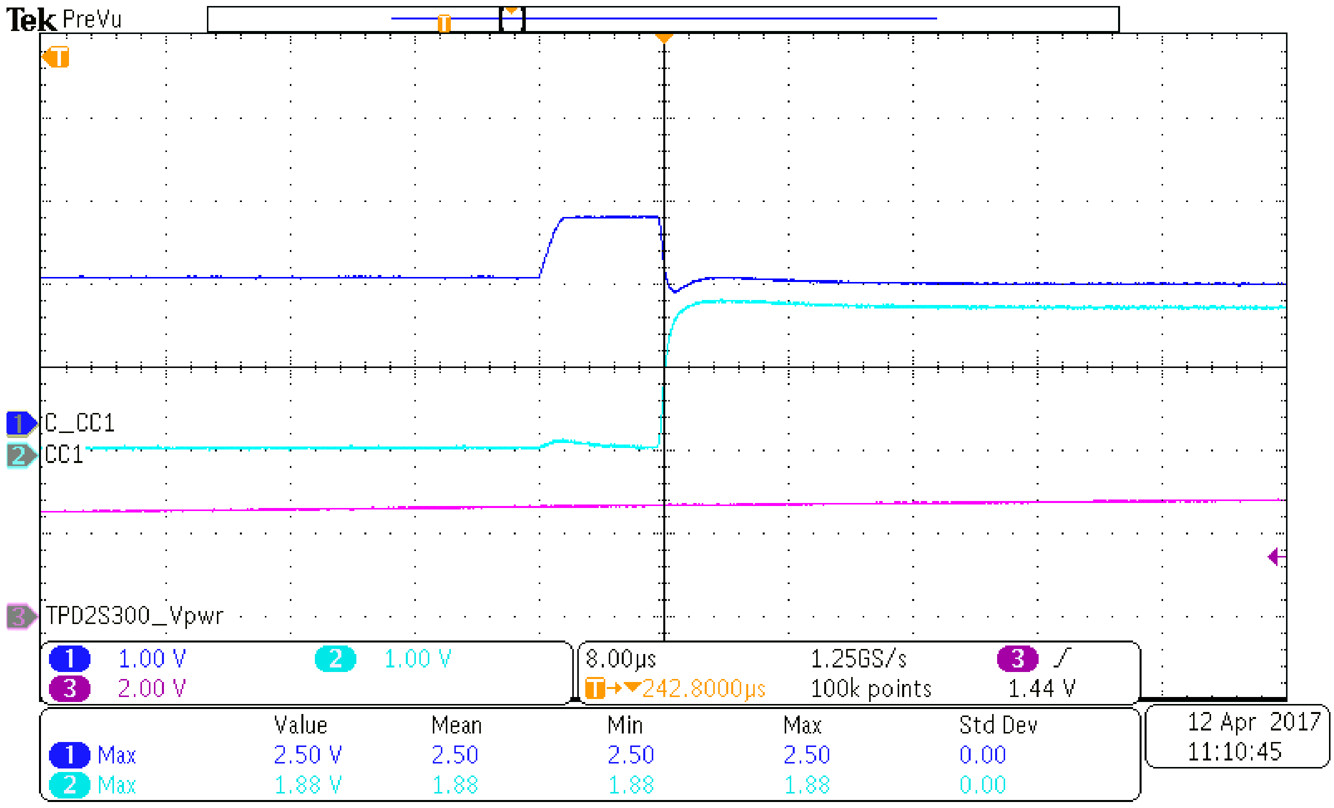


Figure 22. TPD2S300 Turning On in Dead Battery Mode With 5.1-kΩ on CC1

8.2.2 Laptop Application

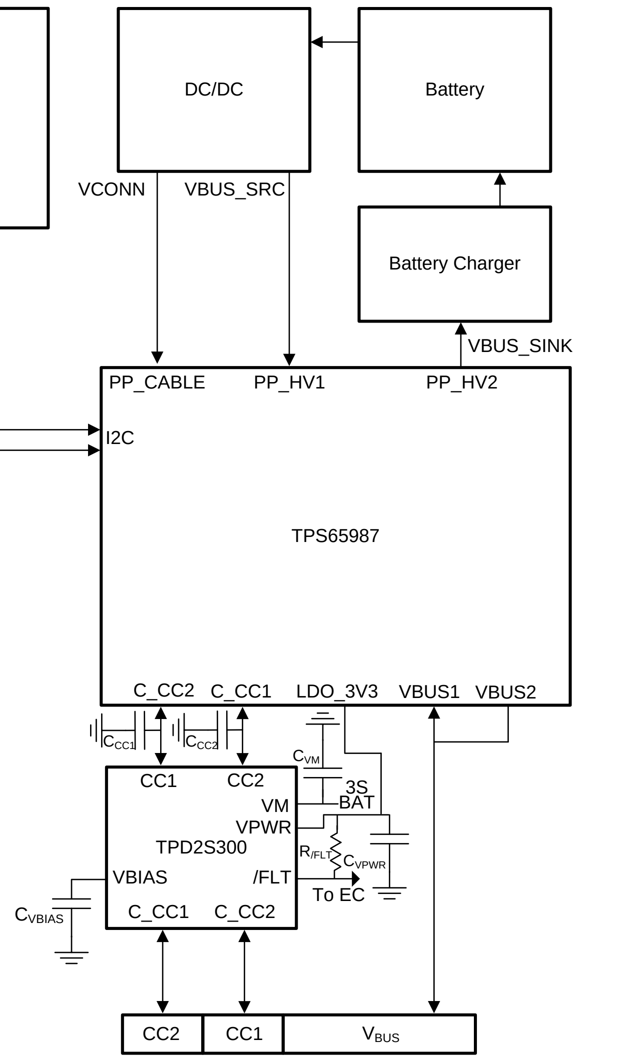


Figure 23. TPD2S300 Typical Application Diagram

8.2.2.1 Design Requirements

In this application example, we use the TPD2S300 to protect a USB Type-C port in a laptop application. In this application, the laptop needs USB3.0 support and 20-V, 5-A charging. Because 20 V is required, USB-PD needs to be used in this application to achieve this, as USB Type-C alone cannot support higher than 5 V. In order to add USB-PD operation in a laptop application, the TPS65987 is used. This device is a full-featured USB Type-C and USB PD controller that integrates all the analog and power paths needed to support 20-V, 5-A charging and USB3.0.

With USB-C with 20-V PD being used, a Short-to-V_{BUS} event can occur in the system. This short can affect both the CC and SBU pins. However, in this application, since only USB3.0 is required, the SBU pin is not used. Therefore, only CC Short-to-V_{BUS} protection is required to adequately protect TPS65987 and the system. The CC pins also need IEC61000-4-2 system level ESD protection. Additionally, with this application being a laptop, board space is crucial; a small protection device is required. Therefore, with these application requirements, the TPD2S300 is used, a single-chip solution which integrates all the protection requirements needed for the CC pins in this application.

Table 2 shows the TPD2S300 design parameters for this application.

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BUS} nominal operating voltage	20 V
Short-to-V_{BUS} tolerance for the CC pins	24 V
VBIAS nominal capacitance	0.1 µF
Dead battery charging	100 W
TPD2S300 VPWR power source	3.3-V LDO from TPS65987
TPD2S300 VM power source	3S or 4S Battery
V_{CONN} requirement	1-W V_{CONN} required
Maximum ambient temperature requirement	85°C

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 VBIAS Capacitor Selection

This VBIAS capacitor requirements for this application are identical to the Smart-Phone application; see the *VBIAS Capacitor Selection* section for more details.

8.2.2.2.2 Dead Battery Operation

For this application, we want to support 100-W dead battery operation; when the laptop is out of battery, we still want to charge the laptop at 20 V and 5 A. This means that the USB PD Controller must receive power in dead battery mode. The TPS65987 has its own built in LDO in order to supply the TPS65987 power from V_{BUS} in a dead battery condition. The TPS65987 can also provide power to its flash during this condition through its LDO_3V3 pin.

The TPD2S300s OVP FETs remain OFF when it is unpowered in order to insure in a dead battery situation proper protection is still provided to the PD controller in the system, in this case the TPS65987. However, when the OVP FETs are OFF, this isolates the TPS65987's dead battery resistors from the USB Type-C ports CC pins. A USB Type-C power adaptor must see the R_D pull-down dead battery resistors on the CC pins or it does not turn ON V_{BUS} to provide power. Since the TPS65987s dead battery resistors are isolated from the USB Type-C connector's CC pins, the TPD2S300 integrates dead battery resistors on its C_CCx pins, and exposes them when the device is unpowered.

Once the power adaptor sees the TPD2S300's dead battery resistors, it applies 5 V on the V_{BUS} pin. This provides power to the TPS65987, turning the PD controller on, and allowing the battery to begin to charge. However, this application requires 100-W charging in dead battery mode, so V_{BUS} at 20 V and 5 A is required. USB PD negotiation is required to accomplish this, so the TPS65987 needs to be able to communicate on the CC pins. This means the TPD2S300 needs to be turned on in dead battery mode as well so the TPD65987's PD controller can be exposed to the CC lines. To accomplish this, it is critical that the TPD2S300 is powered by the TPS65987's internal LDO, the LDO_3V3 pin. This way, when the TPS65987 receives power on V_{BUS}, the TPD2S300 is turned on simultaneously. Additionally, for low resistance VCONN support, the VM pin needs to be connected to the 3S battery, so TPD2S300 needs to be able to receive this voltage in the dead battery condition as well.

It is critical that the TPS65987's dead battery resistors are present; once the TPD2S300 receives power, removes its dead battery resistors and turns on its OVP FETs, R_D pull-down resistors must be present on the CC line in order to guarantee the power adaptor stays connected. If RD is not present and the voltage on CC increases to Src.Open, the power adaptor can interpret this as a disconnect and remove V_{BUS}.

Also, it is important that the TPS65987's dead battery resistors are present so it properly boots up in dead battery operation with the correct voltages on its CC pins.

Once this process has occurred, the TPS65987 can start negotiating with the power adaptor through USB PD for higher power levels, allowing 100-W operation in dead battery mode.

For more information on the TPD2S300 dead battery operation, see the *CC Dead Battery Resistors Integrated for Handling Dead Battery Use Case in Mobile Devices* section in the description section of the datasheet. Also, see Figure 22 for a waveform of the CC line when the TPD2S300 is turning on and exposing the TPS65987's dead battery resistors to the USB Type-C connector.

8.2.2.2.3 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines. The specification from section 5.8.6 of the *USB PD Specification* is given in Table 4.

Table 7. USB PD cReceiver Specification

NAME	DESCRIPTION	MIN	MAX	UNIT	COMMENT
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system shall have capacitance within this range when not transmitting on the line

Therefore, the capacitance on the CC lines must stay in between 200 pF and 600 pF when USB PD is being used. Therefore, the combination of capacitances added to the system by the TPS65987, the TPD2S300, and any external capacitor must fall within these limits. Table 5 shows the analysis involved in choosing the correct external CC capacitor for this system, and shows that an external CC capacitor is required.

Table 8. CC Line Capacitor Calculation

CC Capacitance	MIN	MAX	UNIT	COMMENT
CC line target capacitance	200	600	pF	From the *USB PD Specification* section (cReceiver, section 5.8.6)
TPS65987 capacitance	70	120	pF	From the TPS65987 Datasheet
TPD2S300 capacitance	30	120	pF	From the *Electrical Characteristics* table
Proposed capacitor GRM033R71E221KA01D	110	330	pF	CAP, CERM, 220 pF, 25 V, ±10%, X7R, 0201 (For min and max, assume ±50% capacitance change with temperature and voltage derating to be overly conservative)
TPS65987 + TPD2S300 + GRM033R71E221KA01D	210	570	pF	Meets USB PD cReceiver Specification

8.2.2.2.4 $\overline{\text{FLT}}$ Pin Operation

This $\overline{\text{FLT}}$ pin recommendation for this application are identical to the Smart-Phone application; see the *$\overline{\text{FLT}}$ Pin Operation* section for more details.

8.2.2.2.5 V_{CONN} Operation

In our current application example, 1-W V_{CONN} is required. With a 5-V source on the TPS65987's PP_CABLE pin, this means 200 mA of current is required. Therefore, it is ideal to put the TPD2S300 in low-resistance mode, which is easy to do in this application because of the presence of a 3S battery in the laptop. Tie the VM pin to the 3S battery voltage. With the VM pin tied to the 3S battery, the worst case resistance of TPD2S300 with 4.87 V on CCx is 608 mΩ. This way with 200 mA flowing through the TPD2S300, voltage drop is much lower across the TPD2S300 and it is easier to achieve the VCONN voltage requirements given in the USB Type-C Specification.

8.2.2.3 Application Curves

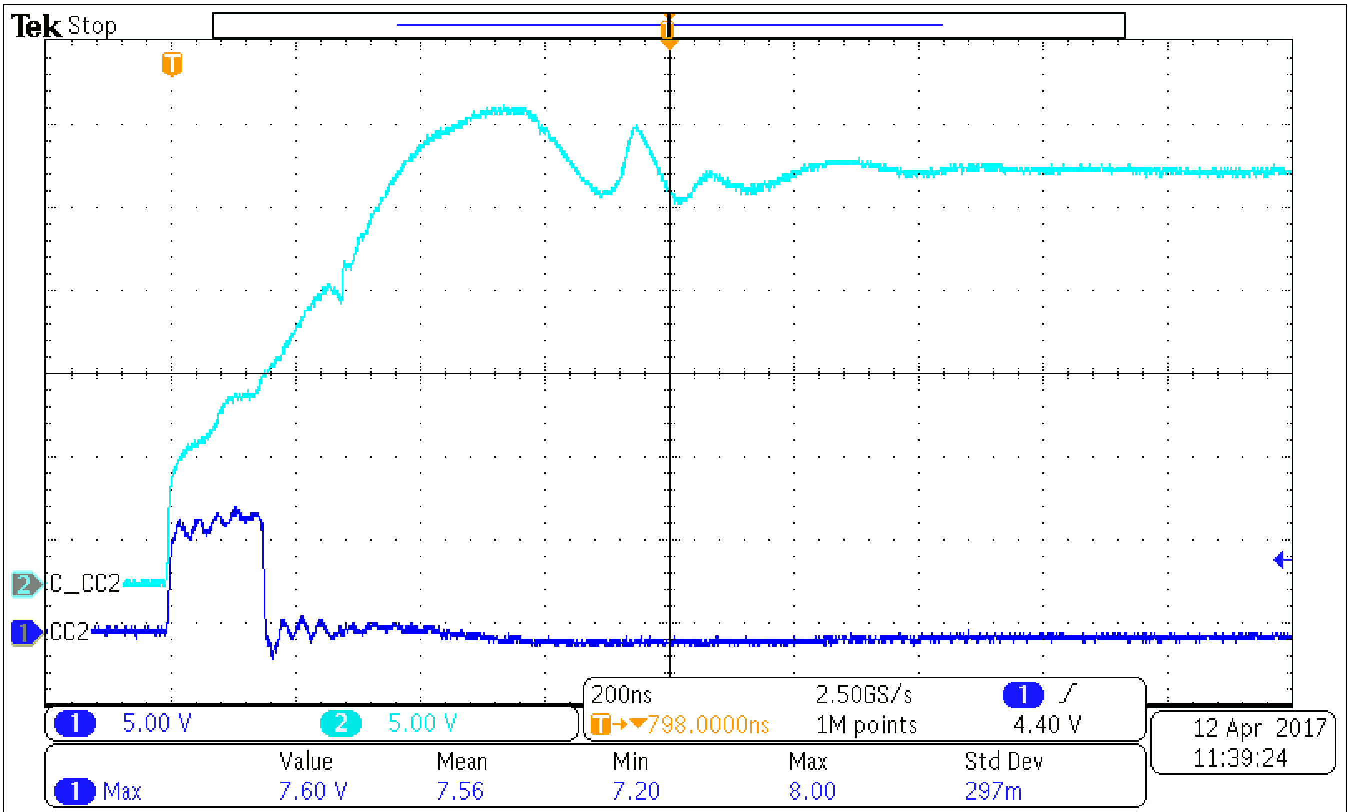


Figure 24. TPD2S300 Protecting the TPS65982 During a Short-to-V_{BUS} Event

8.2.3 Power Adaptor Application

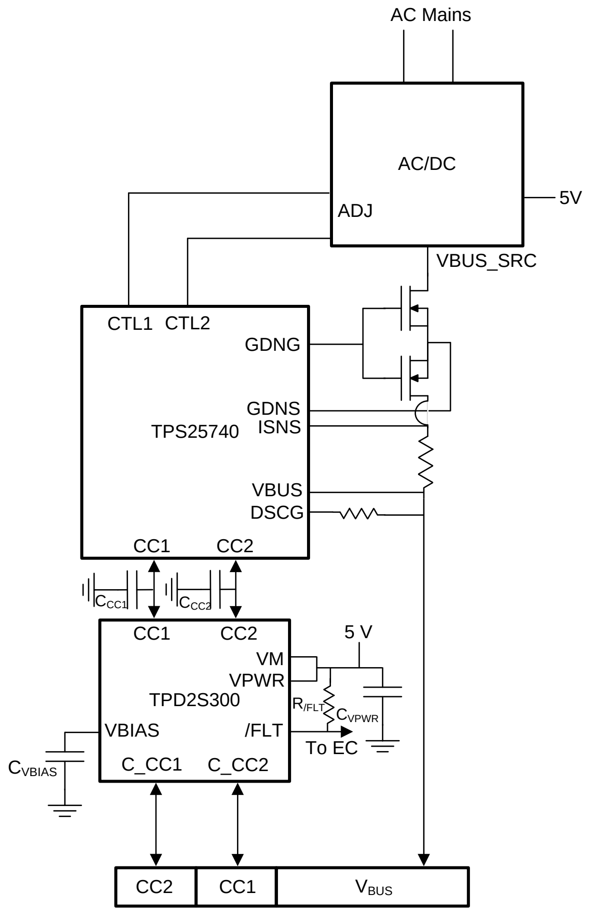


Figure 25. TPD2S300 Typical Application Diagram

8.2.3.1 Design Requirements

In this application example, we use the TPD2S300 to protect a USB Type-C port in a power adaptor application. In this application, the power adaptor needs to supply 20 V, 3 A to the device it is charging. Because 20 V is required, USB-PD needs to be used in this application to achieve this, as USB Type-C alone cannot support higher than 5 V. In order to add USB-PD operation in a power adaptor application, the TPS25740 is used. This device is a USB Type-C and USB PD Source Controller.

With USB-C with 20-V PD being used, a Short-to-V_{BUS} event can occur in the system. This short can affect both the CC and SBU pins. However, in this application, since only USB Type-C and PD charging is required, the SBU pin is not used. Therefore, only CC Short-to-V_{BUS} protection is required to adequately protect the TPS25740 and the system. The CC pins also need IEC61000-4-2 system level ESD protection. Additionally, with this application being a power adaptor, board space is crucial; a small protection device is required. Therefore, with these application requirements, the TPD2S300 is used, a single-chip solution which integrates all the protection requirements needed for the CC pins in this application.

Table 2 shows the TPD2S300 design parameters for this application.

Table 9. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BUS} nominal operating voltage	20 V
Short-to-V_{BUS} tolerance for the CC pins	24 V
VBIAS nominal capacitance	0.1 µF

Table 9. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Dead battery charging	No dead battery mode; source only device
TPD2S300 VPWR and VM power source	5-V source
V_{CONN} requirement	V_{CONN} not required
Maximum ambient temperature requirement	85°C

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 VBIAS Capacitor Selection

This VBIAS capacitor requirements for this application are identical to the Smart-Phone application; please see the *VBIAS Capacitor Selection* section for more details.

8.2.3.2.2 Dead Battery Operation

This application is source mode only. Therefore, dead battery operation is not required, and R_D resistors must not be exposed on the CC lines. However, because when the TPD2S300 is unpowered it exposes its dead battery resistors, when the wall adaptor is not plugged into the wall, it has RDs present on its CC lines. If it is plugged into a laptop at this point, then the laptop senses a connection and output 5-V V_{BUS}. Therefore, the power switch that sources V_{BUS} in the wall adaptor must be able to block this 5-V V_{BUS} from entering the system when it is unplugged from the wall. If this is maintained, there is not any issue. Once, the wall adaptor is plugged into the wall, it turns ON the TPD2S300. This removes the TPD2S300's RD dead battery resistor, and then the laptop stops sourcing V_{BUS}. Once the laptop starts its DRP toggle, it exposes its RD, which causes a connection with the wall adaptor to occur, and the wall adaptor outputs V_{BUS}, and then PD is negotiated like normal.

8.2.3.2.3 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines. The specification from section 5.8.6 of the *USB PD Specification* is given in Table 10.

Table 10. USB PD cReceiver Specification

NAME	DESCRIPTION	MIN	MAX	UNIT	COMMENT
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system shall have capacitance within this range when not transmitting on the line

Therefore, the capacitance on the CC lines must stay in between 200 pF and 600 pF when USB PD is being used. Therefore, the combination of capacitances added to the system by the TPS25740, the TPD2S300, and any external capacitor must fall within these limits. Table 11 shows the analysis involved in choosing the correct external CC capacitor for this system, and shows that an external CC capacitor is required.

Table 11. CC Line Capacitor Calculation

CC Capacitance	MIN	MAX	UNIT	COMMENT
CC line target capacitance	200	600	pF	From the *USB PD Specification* section (cReceiver, section 5.8.6)
TPS25740 capacitance	~0	10	pF	From the TPS25740 Datasheet
TPD2S300 capacitance	30	120	pF	From the *Electrical Characteristics* table
Proposed capacitor GRM033R71E331KA01D	198	462	pF	CAP, CERM, 330 pF, 25 V, ±10%, X7R, 0201 (For min and max, assume ±40% capacitance change with temperature and voltage derating to be overly conservative)
TPS25740 + TPD2S300 + GRM033R71E331KA01D	228	592	pF	Meets USB PD cReceiver specification

8.2.3.2.4 $\overline{FLT}$ Pin Operation

The $\overline{FLT}$ pin recommendation for this application are identical to the Smart-Phone application; see the *$\overline{FLT}$ Pin Operation* section for more details.

8.2.3.2.5 V_{CONN} Operation

In our current application example, V_{CONN} is not required. Therefore, a 3.3-V source or 5-V source can be connected to the VPWR and VM pins of the TPD2S300 to provide adequate resistance in order to support CC analog and USB PD operation over the CC lines. In fact, the CC OVP FETs resistance specifications are set to optimize the FET size and therefore the TPD2S300 size and still allow proper CC analog and USB PD operation. See the *Electrical Characteristics* table for the specific resistances of the CC OVP FETs.

8.2.3.3 Application Curves

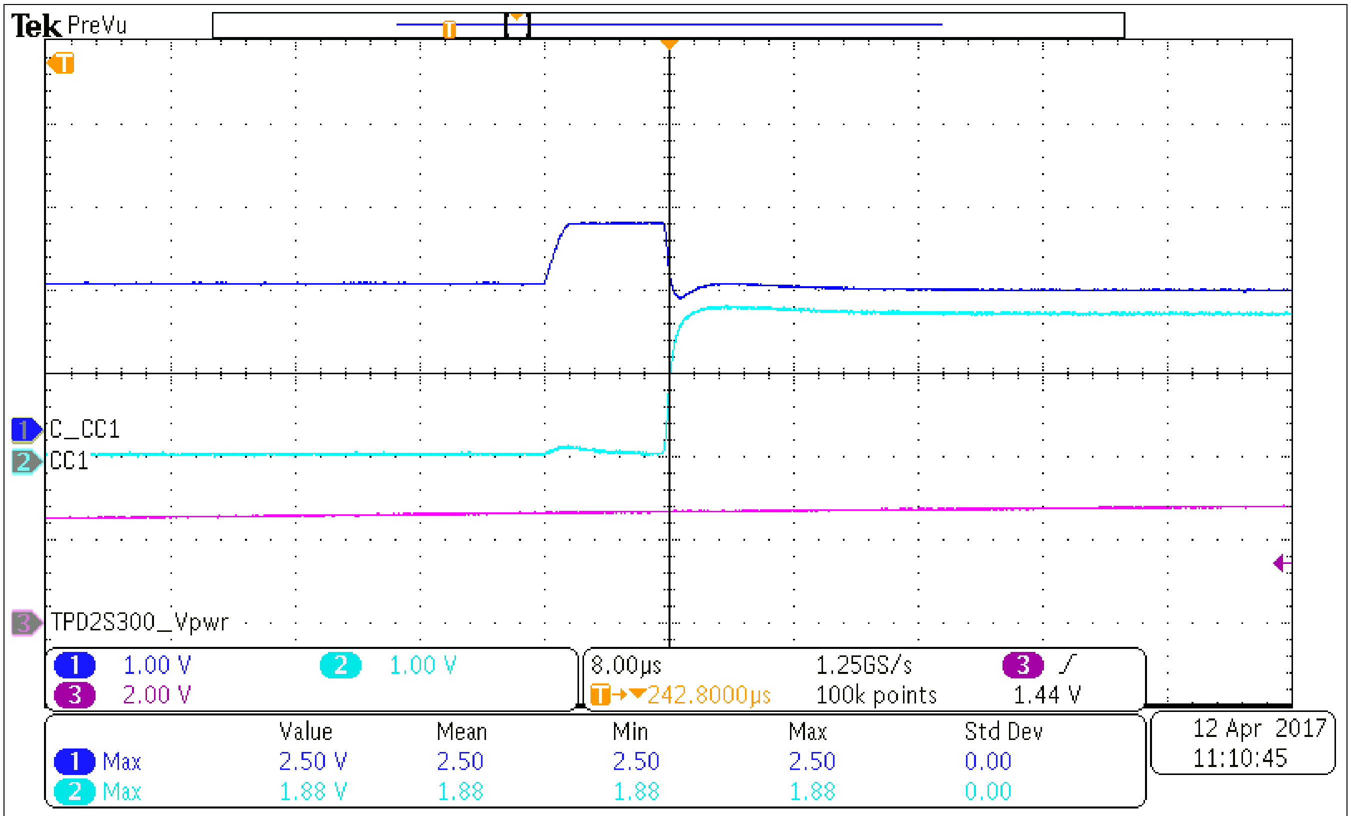


Figure 26. TPD2S300 Turning On in Dead Battery Mode With 5.1-kΩ on CC1

9 Power Supply Recommendations

The VPWR pin provides power to all the circuitry in the TPD2S300. It is recommended a 1-µF decoupling capacitor is placed as close as possible to the VPWR pin. If USB PD is desired to be operated in dead battery conditions, it is critical that the TPD2S300 share the same power supply as the PD controller in dead battery boot-up (such as sharing the same dead battery LDO). See the *CC Dead Battery Resistors Integrated for Handling Dead Battery Use Case in Mobile Devices* section for more details.

The VM pin is used to control the resistance of the CC OVP FETs. If only CC analog and PD communications are needed over the CC lines, short this pin to VPWR, and no extra capacitor is needed. However, if wanting to use V_{CONN} on CC, and the lower resistance operation of the TPD2S300 is needed, then VM needs to be connected to its own independent voltage source that is ≥ 9 V and ≤ 22 V. This is usually the 3S or 4S battery in the system. If connected to its own independent voltage source, then VM with need its own 1-µF decoupling capacitor; it is recommended to place this capacitor as close as possible to the VM pin.

10 Layout

10.1 Layout Guidelines

Proper routing and placement is important to maintain the signal integrity the CC line signals. The following guidelines apply to the TPD2S300:

- Place the bypass capacitors as close as possible to the V_{PWR} and V_M pins, and ESD protection capacitor as close as possible to the V_{BIAS} pin. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to-V_{BUS} and ESD strikes.

Standard ESD recommendations apply to the C_CC1 and C_CC2 pins:

- The optimum placement for the device is as close to the connector as possible:
  – EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  – The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TPD2S300 and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TPD2S300 and the connector by using rounded corners with the largest radii possible.
  – Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

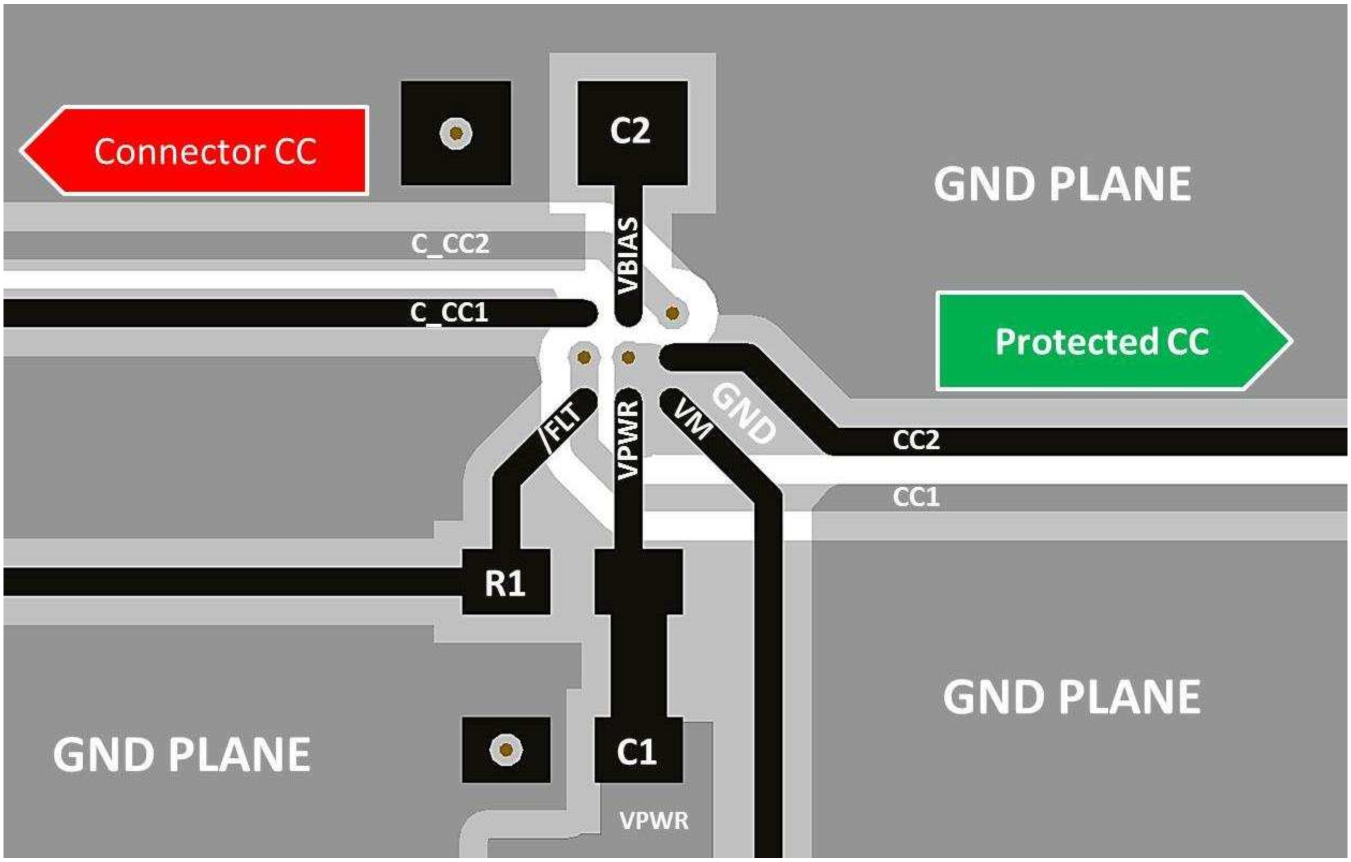


Figure 27. TPD2S300 Typical Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

TPD2S300YFF Evaluation Module

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2S300YFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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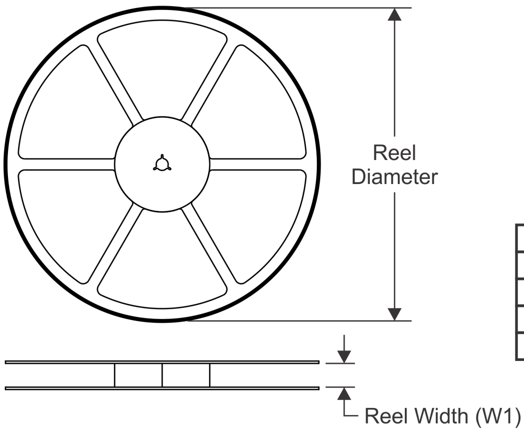
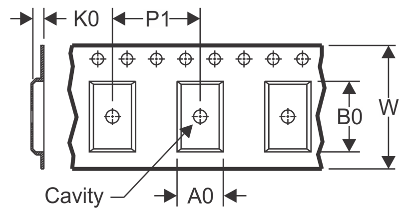
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

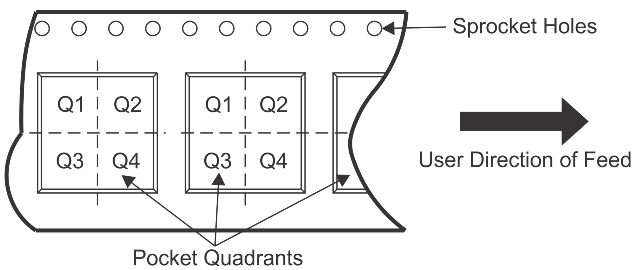


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

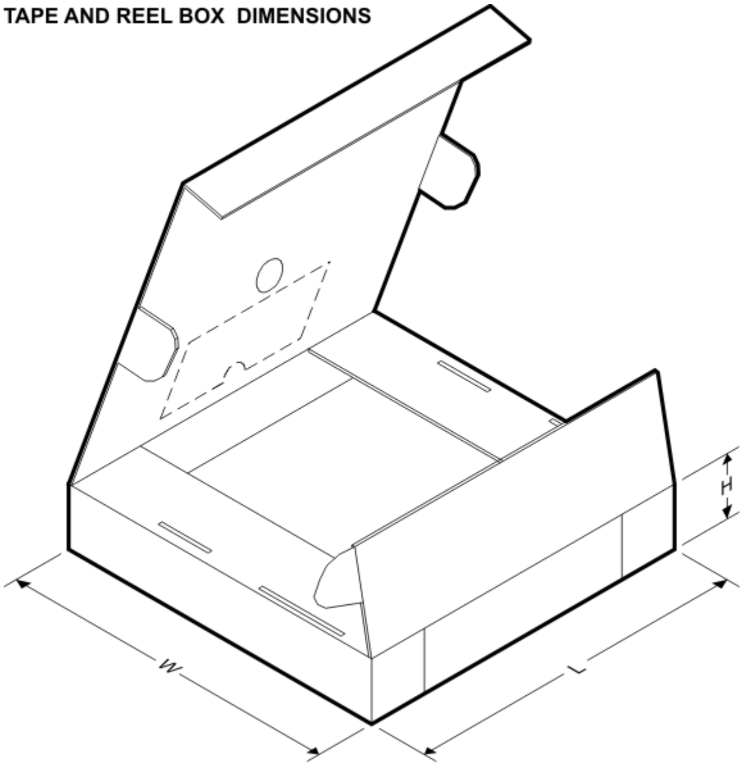
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

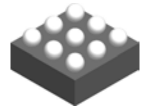
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2S300YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1

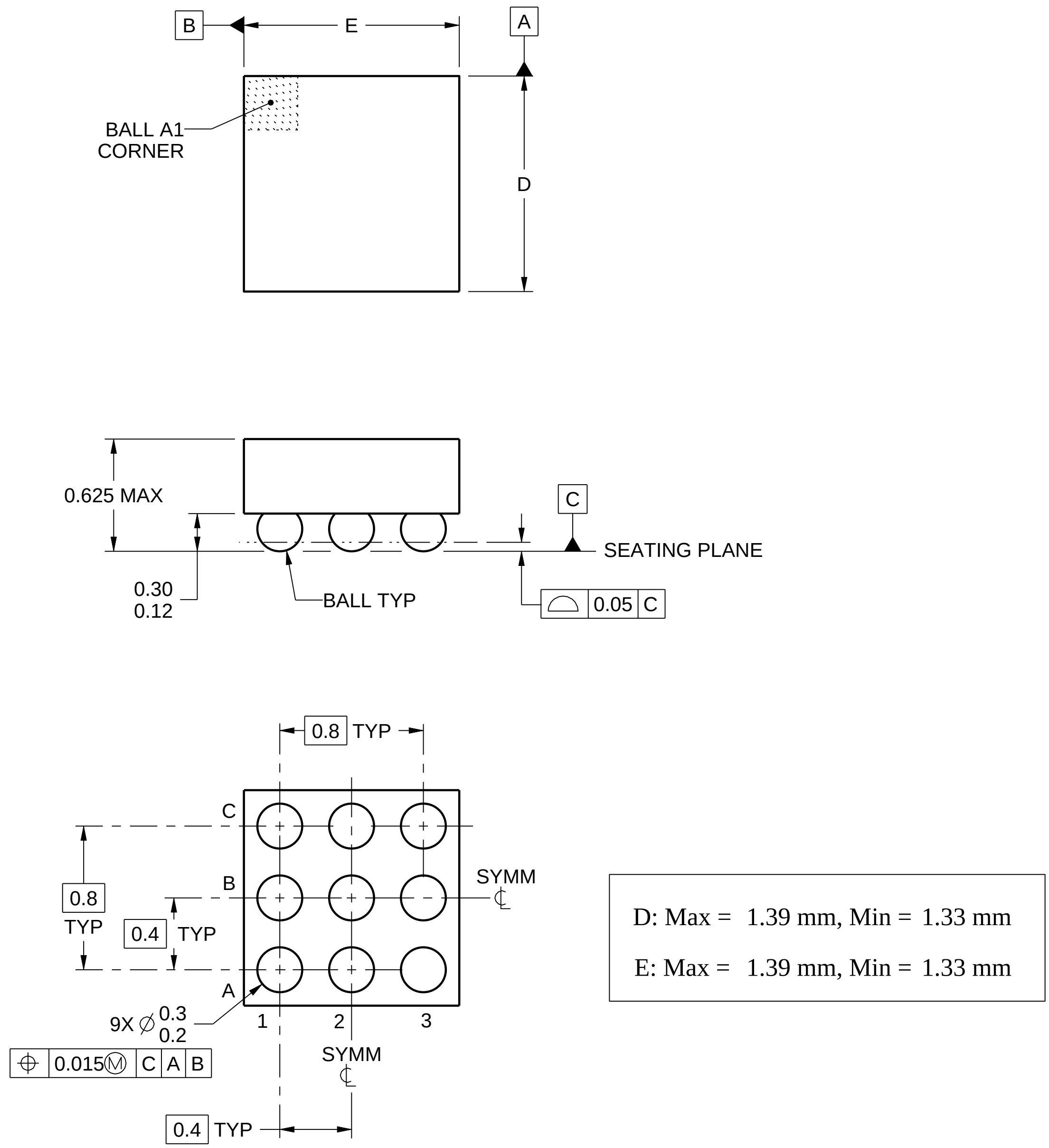
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2S300YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0





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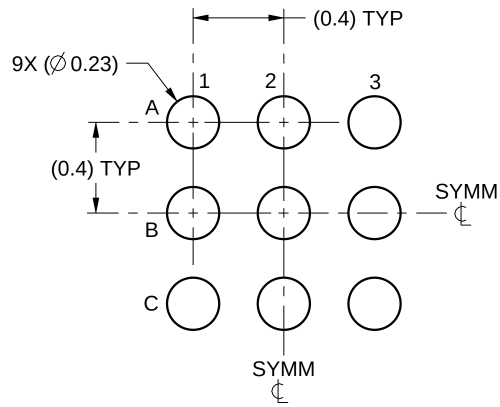
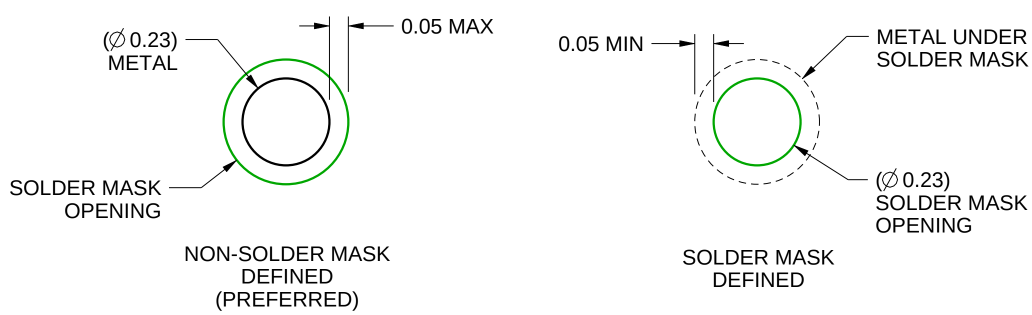
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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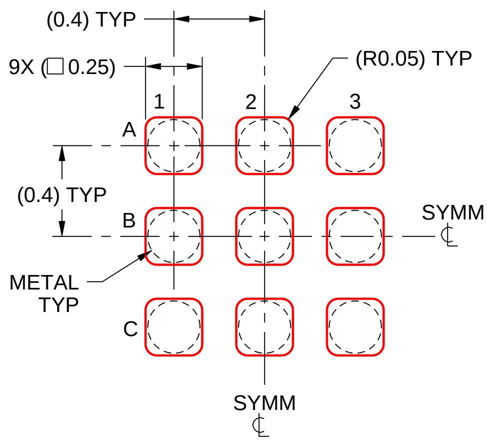
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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