

## Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
- 20	0.101 at V <sub>GS</sub> = - 4.5 V	- 4.5 <sup>a</sup>	4.9 nC
	0.141 at V <sub>GS</sub> = - 2.5 V	- 4.5 <sup>a</sup>	
	0.192 at V <sub>GS</sub> = - 1.8 V	- 2	

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- New Thermally Enhanced PowerPAK<sup>®</sup> SC-70 Package
  - Small Footprint Area
  - Low On-Resistance
- Typical ESD Protection 4000 V

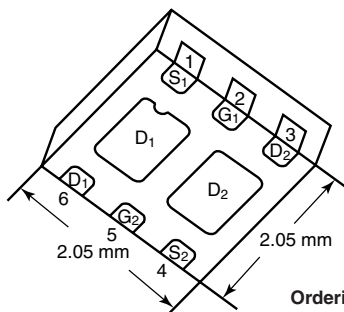


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

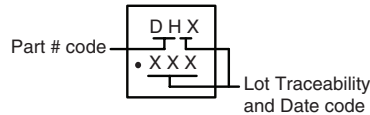
### APPLICATIONS

- Load Switch, PA Switch and Battery Switch for Portable Devices

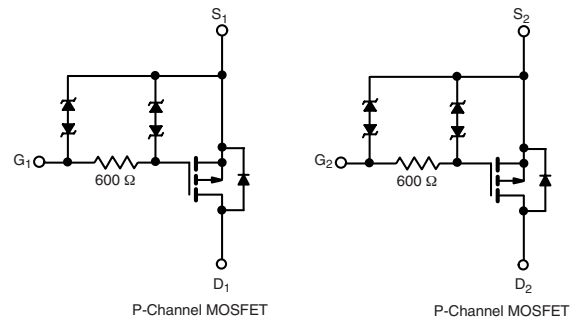
PowerPAK SC-70-6 Dual



Marking Code



Ordering Information: SiA911EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	- 20	V
Gate-Source Voltage	V <sub>GS</sub>	± 8	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	- 4.5 <sup>a</sup>
		T <sub>C</sub> = 70 °C	- 4.5 <sup>a</sup>
		T <sub>A</sub> = 25 °C	- 3.6 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	- 2.9 <sup>b, c</sup>
Pulsed Drain Current	I <sub>DM</sub>	- 10	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	- 1.6 <sup>b, c</sup>
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	7.8
		T <sub>C</sub> = 70 °C	5
		T <sub>A</sub> = 25 °C	1.9 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	1.2 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 s	R <sub>thJA</sub>	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	12.5	16	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 110 °C/W.

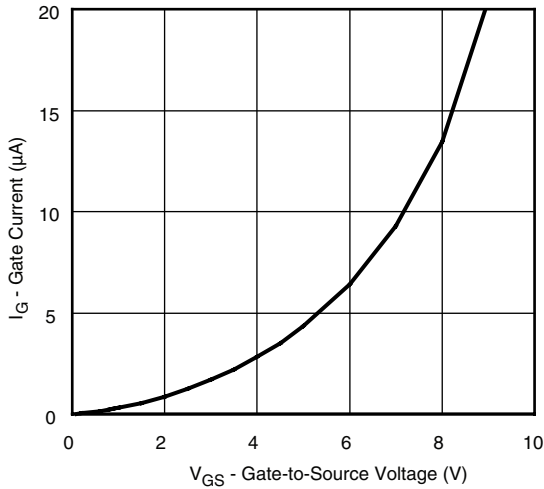
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-21		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-1	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 100$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-10			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -2.7\text{ A}$		0.083	0.101	$\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -2.3\text{ A}$		0.115	0.141	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.153	0.192	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\text{ V}, I_D = -2.7\text{ A}$		7		S
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -10\text{ V}, V_{GS} = -8\text{ V}, I_D = -3.6\text{ A}$		7.1	11	nC
				4.2	6.5	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -3.6\text{ A}$		0.7		nC
Gate-Drain Charge	$Q_{gd}$			1.2		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		600		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 3.5\text{ }\Omega$ $I_D \cong -2.9\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		92	140	ns
Rise Time	$t_r$			200	300	
Turn-Off Delay Time	$t_{d(off)}$			700	1100	
Fall Time	$t_f$			400	600	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 3.5\text{ }\Omega$ $I_D \cong -2.9\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$		32	50	ns
Rise Time	$t_r$			70	105	
Turn-Off Delay Time	$t_{d(off)}$			990	1500	
Fall Time	$t_f$			410	615	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			-4.5	A
Pulse Diode Forward Current	$I_{SM}$				-10	
Body Diode Voltage	$V_{SD}$	$I_S = -2.9\text{ A}, V_{GS} = 0\text{ V}$		-0.9	-1.2	V

## Notes:

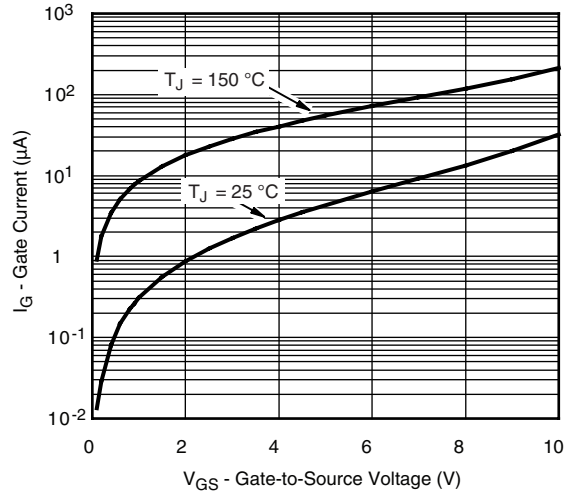
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

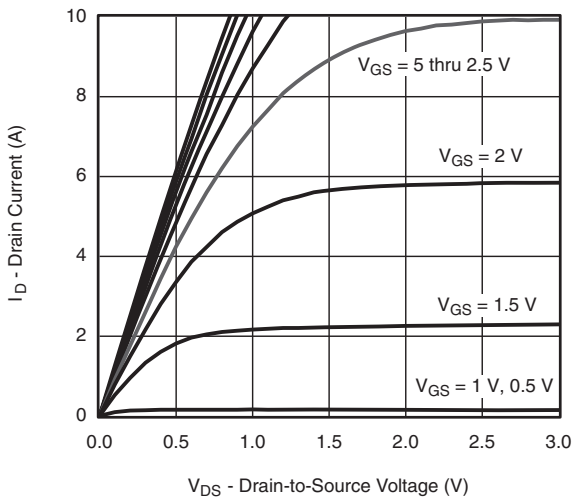
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



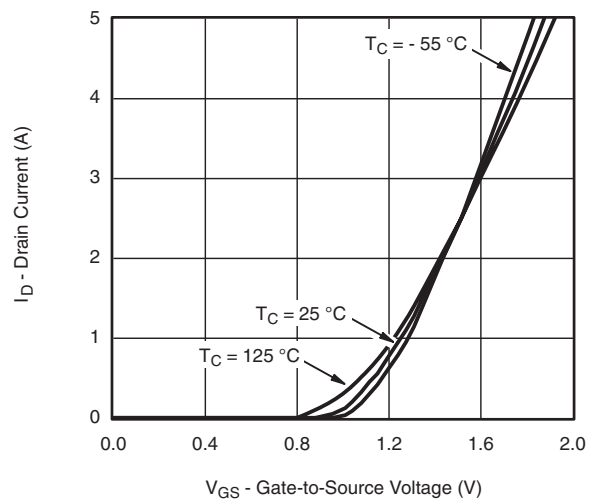
**Gate Current vs. Gate-to-Source Voltage**



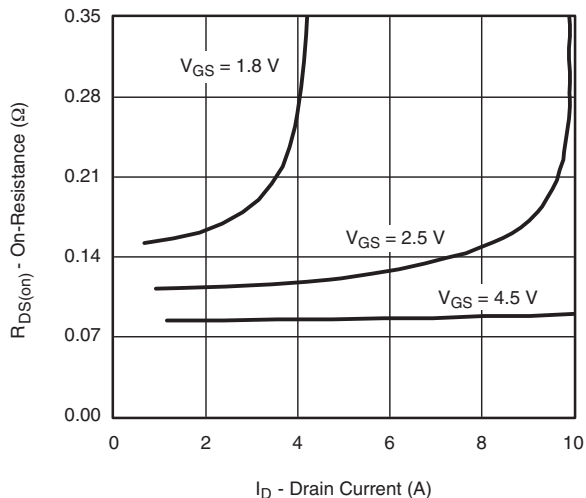
**Gate Current vs. Gate-to-Source Voltage**



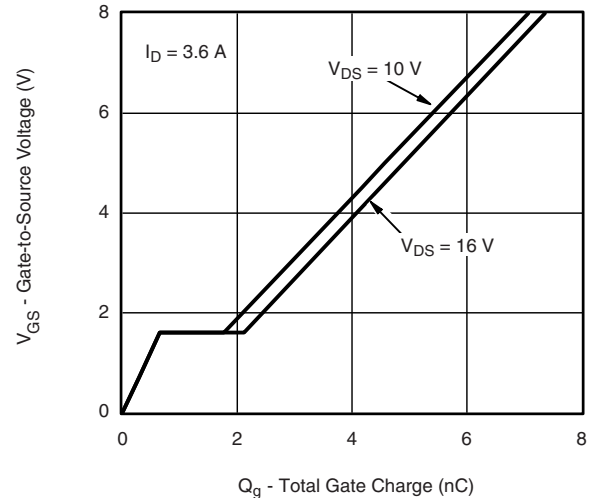
**Output Characteristics**



**Transfer Characteristics**

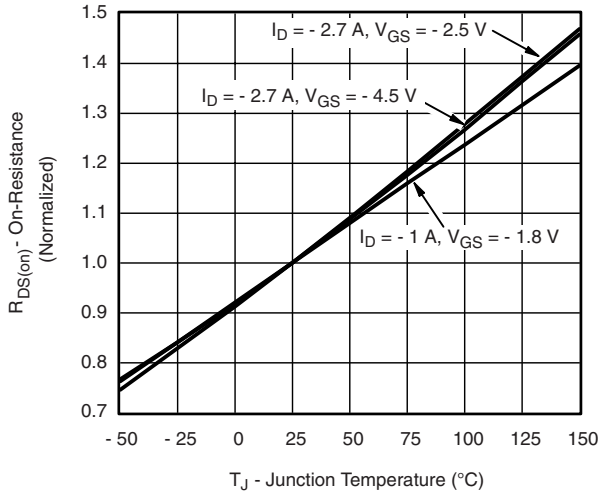


**On-Resistance vs. Drain Current and Gate Voltage**

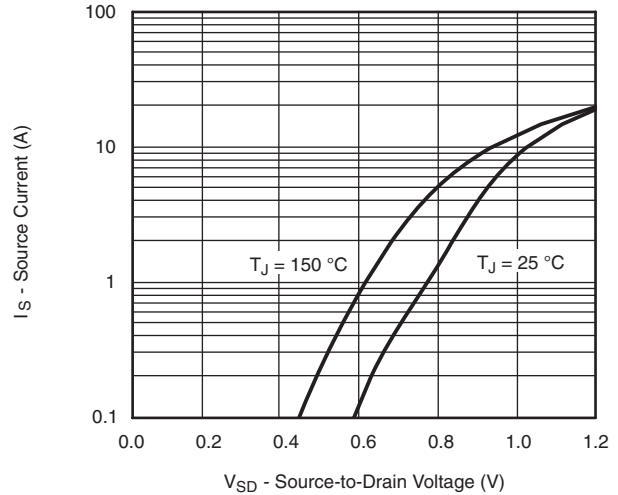


**Gate Charge**

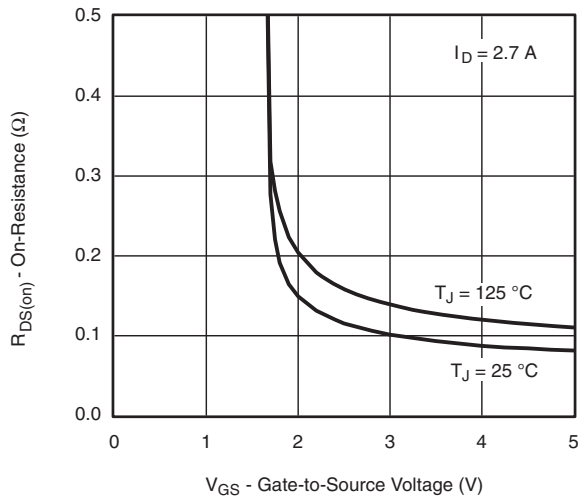
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



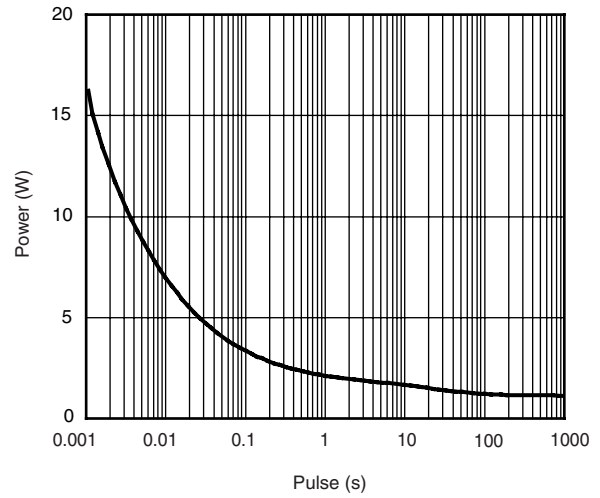
**On-Resistance vs. Junction Temperature**



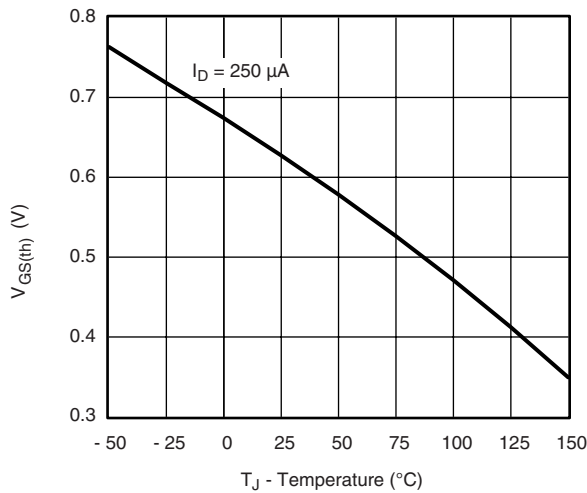
**Source-Drain Diode Forward Voltage**



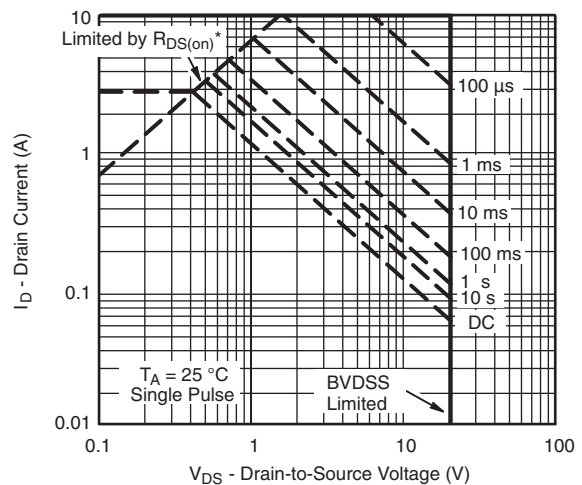
**On-Resistance vs. Gate-to-Source Voltage**



**Single Pulse Power, Junction-to-Ambient**



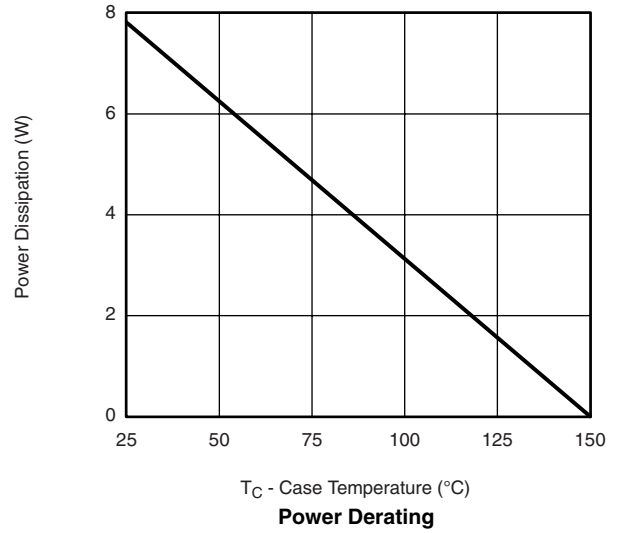
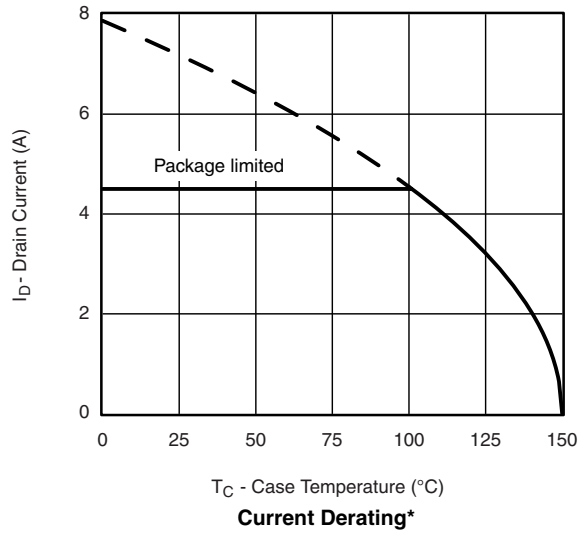
**Threshold Voltage**



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

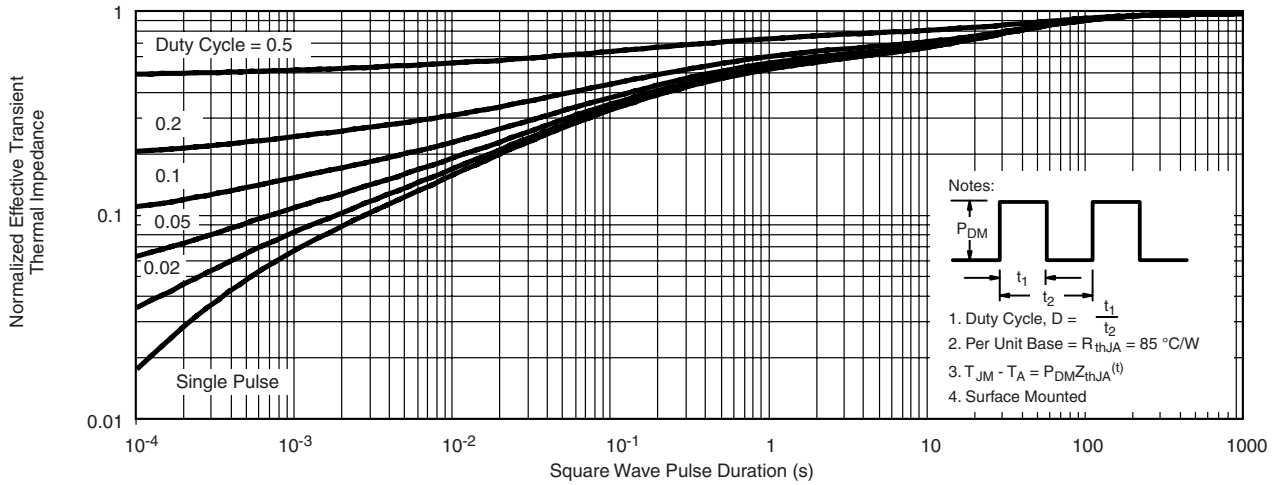
**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

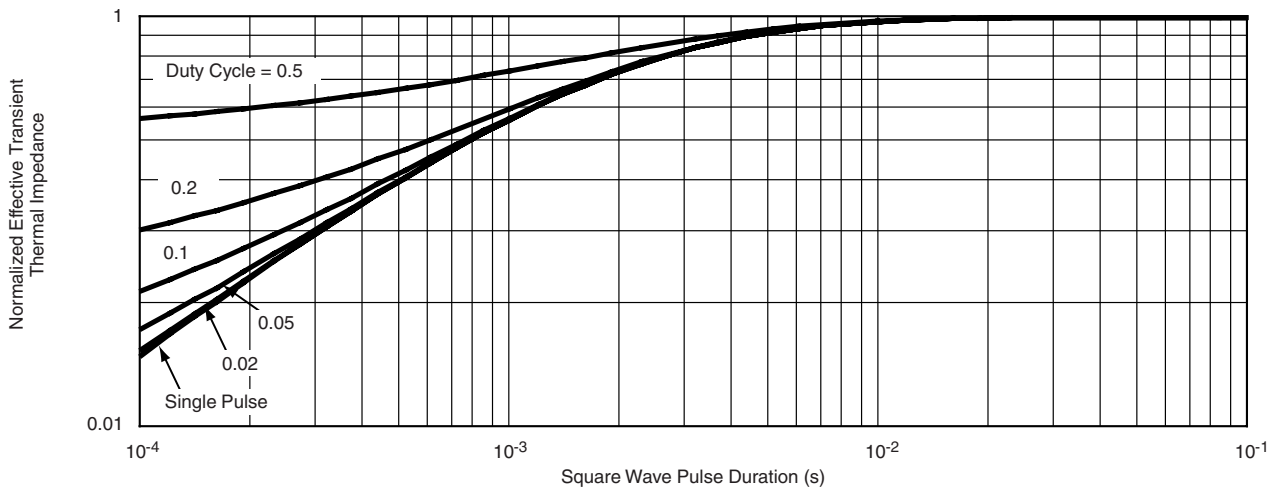


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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