

**Reference Design:**

**HFRD-31.0**

Rev. 2; 11/08

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## **REFERENCE DESIGN**

**20Gbps, Quad-SFP Active Copper Cable Assembly**

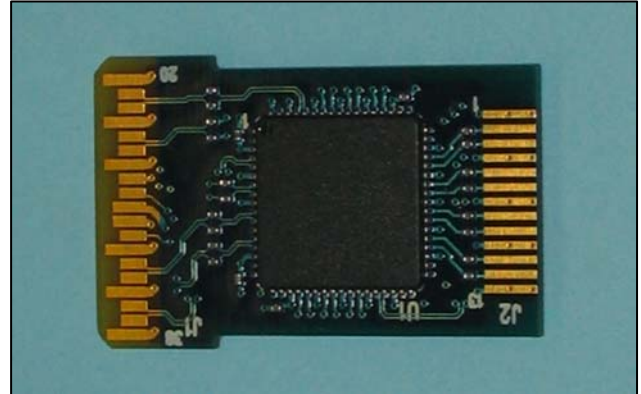
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# 20Gbps, Quad-SFP Active Copper Cable Assembly

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## 1 Overview

High Frequency Reference Design 31.0 (HFRD-31.0) is an active cable transmitter and receiver intended to be integrated within a Quad-SFP (QSFP) cable assembly. This reference design is capable of rates up to 5Gbps on each of its four links. It provides adjustable equalization for different cable lengths and reduces the impact of near-end crosstalk (NEXT) by regenerating the received signal before encountering interfering signals. This regeneration step significantly increases the signal-to-noise ratio thereby improving bit-error margins and allowing longer cable spans. To support the testing and evaluation of the active cable assembly, a host adapter board (HFRD-32.0) is available to supply power and I<sup>2</sup>C serial communication support, and to translate the QSFP high-speed signal connections to SMA connectors.

HFRD-31.0 presents a two-chip solution. One device is a micro-controller, necessary to provide a compliant QSFP software interface. The other device is the MAX3983 Signal Conditioner an eight-channel equalizer that supports four transmit channels and four receive channels.

HFRD-31.0 reduces the risk associated with experimenting with active cable assemblies by supplying complete documentation, performance evaluation and a fully assembled circuit board.

### 1.1 Features

- Schematics
- Bill of Materials
- Gerber plot files available
- Single 3.3V supply
- Adjustable transmitter pre-emphasis
- Regenerates weak signals before launching into the host-side receiver.
- PC board fits into QSFP shell

## 2 Obtaining Additional Information

Limited quantities of the Quad-SFP Active Copper Cable Assembly (HFRD-31.0) are available. For more information about this reference design or to obtain a board, please email your request to: <https://support.maxim-ic.com/>.

### 3 High-Speed Copper Links

High-speed copper links operating over several meters of cable require compensation to correct for inter-symbol interference (ISI) induced jitter. The loss mechanism of simple copper cable reduces higher frequency content more severely than lower frequency content. This disproportionate attenuation requires attention to several signal characteristics to achieve acceptable performance: transition time, swing, crosstalk (cable dress and construction), and signal-to-noise ratio (SNR), to name a few.

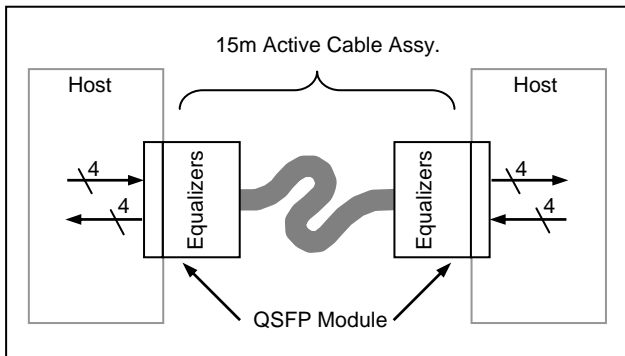


Figure 1. The QSFP active cable assembly relies on the MAX3983 equalizer to achieve a 15m span over copper cable.

Transition time and amplitude conflict with crosstalk and SNR. Attempts to improve an individual channel's performance by increasing swing and reducing transition time generate more interference for adjacent, low-level receive channels. The proximity of the transmit lines with the receive lines makes crosstalk unavoidable; however, it is possible to improve the SNR at the receiver by regenerating the signal before it accumulates more noise.

With only a transmitter that provides compensation for the cable, the signal at the end of the line might have a 100mV of eye opening. In isolation, this is not bad, but in proximity with four outbound transmitters, this eye opening will suffer from crosstalk. Furthermore, the receiver output requirements of the QSFP interface demand the higher output of an active receiver.

### 4 QSFP Requirements

The specification released by the QSFP Multi-Source Agreement committee requires that all status, monitor, and control functions be accessed through a serial communication link. For example, a receiver loss of signal (LOS) and transmit laser fault are now reported only through a register, which is read using I<sup>2</sup>C, instead of the dedicated pins of an SFP interface. In addition, all modules must report various measurements such as received power, temperature, and supply voltage. A micro-controller is needed for these latter measurements.

### 5 Implementation

The MAX3983 provides four transmitters capable of compensating the majority of the 15m span, as well as four receivers to complete the job of compensation and signal regeneration. The result is an end-to-end physical link that is low in crosstalk and low in jitter, and that produces an output swing well above the QSFP minimum. The Atmel® ATMEGA48PV-10MU was chosen because it includes a built-in thermometer and sufficient flash memory, EEPROM, and RAM to support this application. It is housed in a very small, 5mm by 5mm, leadless quad package (QFN). Because of space constraints, the micro controller and the MAX3983 are mounted on opposite sides of the board. See Figure 2.



Figure 2. Front and back of HFRD31.0.

Atmel is a registered trademark of Atmel Corporation.

## 5.1 Cable Transmitter and Receiver

The MAX3983 provides both transmit and receive functions as well as signal detectors. Figure 3 shows the functional block diagram for the MAX3983. Four levels of pre-emphasis are available at the cable transmitter, TX\_OUT, to compensate for different length cables. See Figure 4. Two levels of

pre-emphasis are available at the host-side output, RX\_OUT, to overcome circuit-board and connector losses between the module and the host receiver. See Figure 5. All inputs have fixed equalization. The cable-receive input, RX\_IN, compensates for approximately 5 meters of 24AWG cable. The host-side receive input, TX\_IN, compensates for approximately 10 inches of FR4 at 5Gbps.

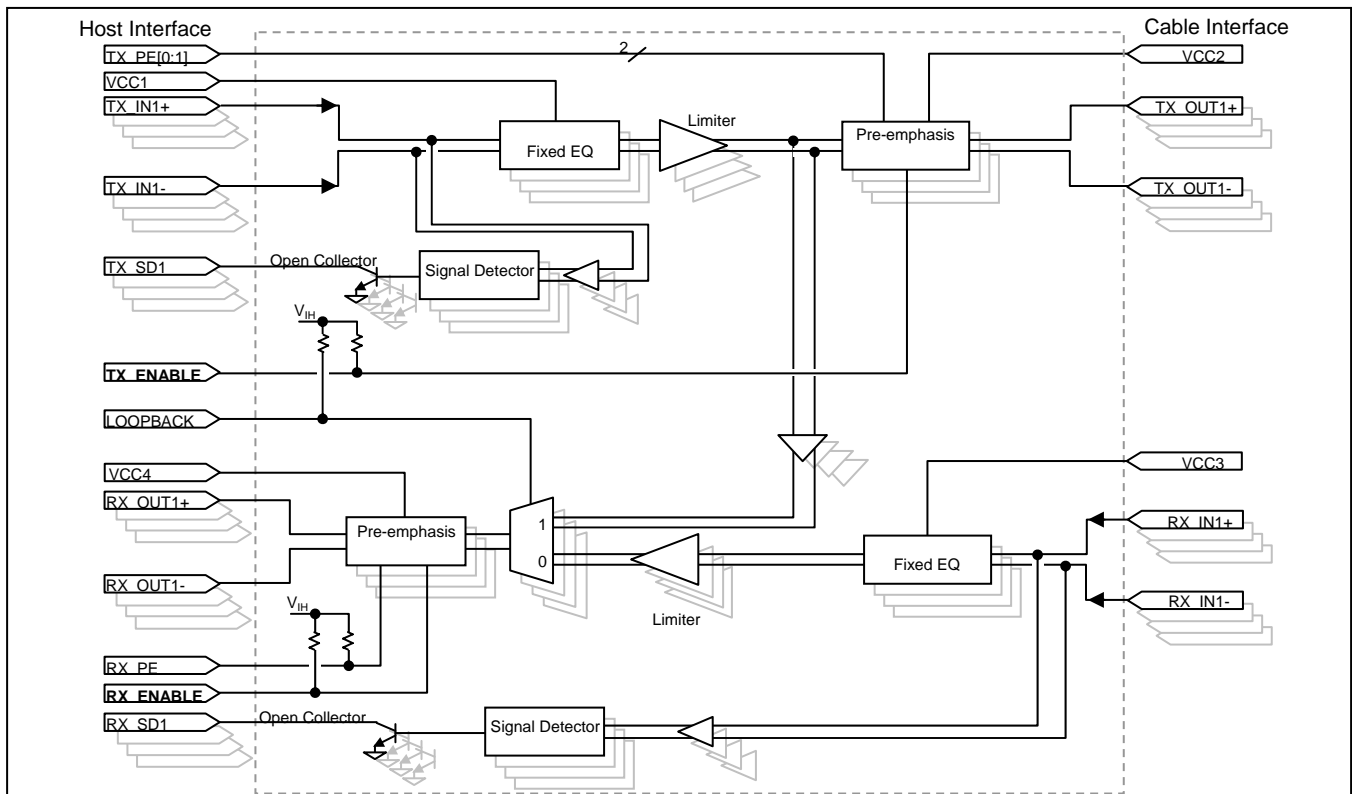


Figure 3. The MAX3983 supports eight differential channels, four outbound and four inbound.

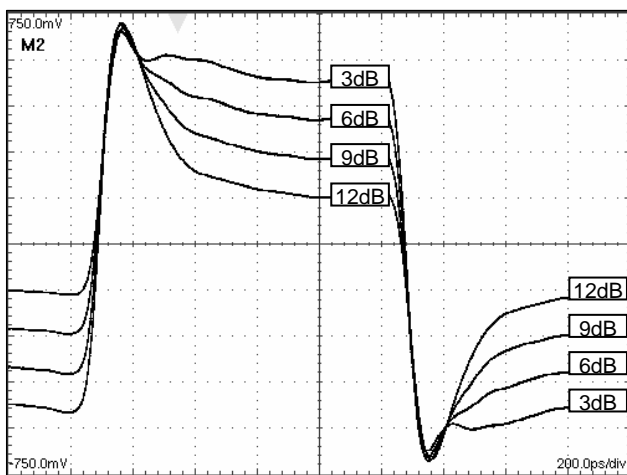


Figure 4. The TX\_OUT pre-emphasis levels.

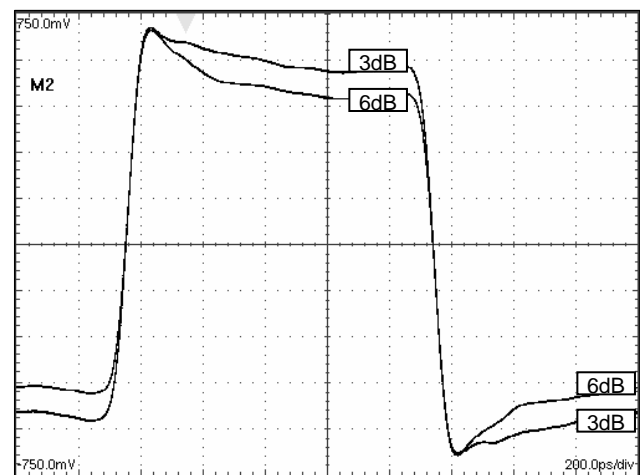


Figure 5. The RX\_OUT pre-emphasis levels.

## 5.2 Construction

The recommended cable is Amphenol's 28 American Wire Gauge (AWG), eight-pair, SpectraStrip® SkewClear®. Other gauge wire can be used, but the loss characteristic will vary with gauge. For example, the expected loss for 28AWG is approximately 50% more than that experienced with 24AWG. Another way to compare the two is by distance. The 24AWG cable will reach approximately 50% farther than the 28AWG.

The multiconductor cable from Amphenol has eight differential wire pairs. Each pair is wrapped in a thin metalized polyester foil with an accompanying bare (drain) wire to serve as a signal shield. The wrapping for each pair is labeled every few inches to aid in identification during assembly. If more space were available within the module shell, it would be easy to strip away more of the cable jacketing and merely twist, weave, and dress the individual pairs in an arbitrary fashion. Amphenol's SpectraStrip wire arrangement greatly simplifies the wiring task. Although some small variations have been encountered, the individual differential wire pairs appear as illustrated in Figure 6. This is not the case with all cable vendors.

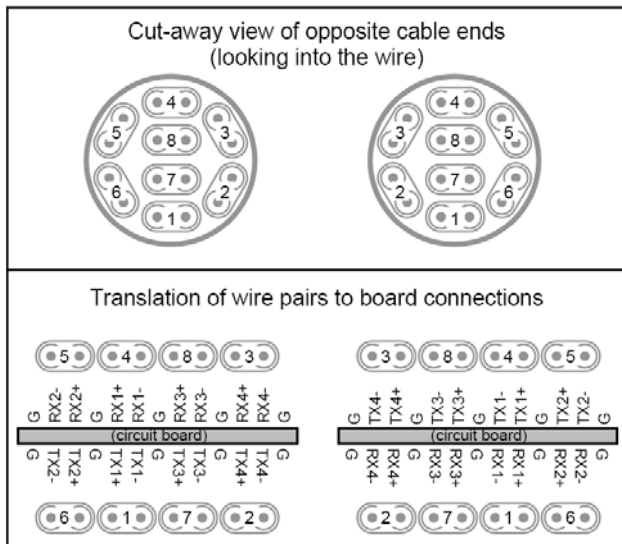


Figure 6. Wire arrangement within the cable bundle and each pair's assignment relative to the board.

In Figure 6, note that the view on the left is a mirror image of the view on the right (i.e., flipped about the vertical axis). The lower portion of Figure 6 shows how the signal pairs are translated from the cable bundle to the circuit boards.

The wire order within the cable bundle is shown in Figure 7. A careful study of how the wires transition from the bundle to the board, minimizes dress problems. The other end of the cable (not shown) is dressed as neatly as the one in the figure.

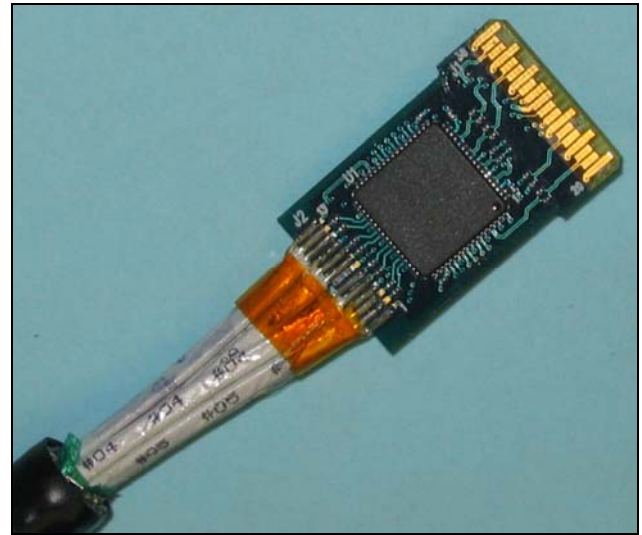


Figure 7. HFRD-31.0 with 28AWG cable. Careful planning results in a neat and space-efficient wire dress.

Finally, the wires within the module shell must be immobilized so that the solder connections to the circuit board do not break. It is recommended that a generous supply of nonconductive silicon adhesive be introduced around the cable-to-board termination to fill the remaining space and secure the connections.

*SpectraStrip and SkewClear are register trademarks of Amphenol Corporation.*

### 5.3 Heat Dissipation

A QSFP module is allowed to dissipate as much as 3.5W. This reference design dissipates between 1.5W and 1.6W. The MAX3983 is packaged with a large pad on the bottom for cooling. The pad is soldered to the ground plane which offers sufficient cooling in most applications. This board is only slightly larger than the device itself and offers no immediate access to a cooling environment. For this reference design, the cable's drain wires provide modest heat conduction. Additional heat control must be integrated into the module's shell design by direct thermal contact with the top of the MAX3983 package.

## 6 Control Interface

The QSFP standard stipulates the memory locations associated with all of the common and optional module functions. The standard also allows vendor-specific controls. HFRD-31.0 reports status and allows monitoring of functions that are relevant to a copper cable implementation. For example, LOS is reported, but other optical functions such as laser fault and received optical power are not reported. Likewise, there are nonoptical functions that are not included in the common QSFP controls such as transmitter pre-emphasis. Table 1 lists the memory location and bit assignments for the various functions that are vendor-specific and unique to HFRD-31.0.

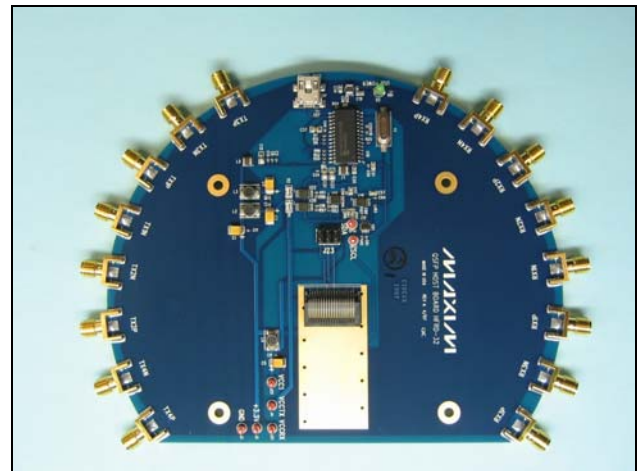
In addition to the control bits for pre-emphasis and output disable, four bytes are used to store gain and offset calibration constants for the temperature and voltage monitors. QSFP allows monitoring for only one of the three supplies. HFRD-31.0 monitors the VCC\_TX pin. One more byte is used to hold the power-on settings. This byte is copied to byte 226 (page 3) when power is applied. Access to these and the other QSFP functions is provided through an I<sup>2</sup>C interface. A supporting reference design, HFRD-32.0, provides this I<sup>2</sup>C interface and the appropriate connections for lab equipment. See Figure 8.

*Microsoft Windows is a registered mark of Microsoft Corporation.*

**Table 1. HFRD-31.0 Vendor-Specific Controls**

Byte	Page	Bit	Description
226	3	5-7	Not used
		4	TX_DISABLE. Set to 1 to disable all transmitter outputs
		3	TX_PE1. Adds to level set by bit 2. Set to 1 to add 6dB of pre-emphasis. Set to 0 to add 0dB.
		2	TX_PE0. Set to 1 for 6dB. Set to 0 for 3dB of pre-emphasis.
		1	RX_DISABLE. Set to 1 to disable all receiver outputs
		0	RX_PE. Set to 1 for 6dB. Set to 0 for 3dB pre-emphasis
226	7		Power-On Defaults. Contains a copy of byte 226, page 3
227	7		Temp Monitor Calibration: Offset
228	7		Temp Monitor Calibration: Gain
229	7		Volt Monitor Calibration: Offset
230	7		Volt Monitor Calibration: Gain

This host adapter board and its associated graphic user interface (GUI) allow access through a Microsoft Windows®-based personal computer equipped with USB 2.0. Figures 9, 10, and 11 are examples of the GUI.



*Figure 8. The QSFP Host Adapter board (HFRD-32.0) includes a USB to I<sup>2</sup>C interface, host-side supply monitor, QSFP interface connector, and SMA connectors for all of the data signals.*



## 6.1 HFRD-32.0 QSFP Host Adapter Software: Monitor Page

**MAXIM Strategic Applications: QSFP Host Adapter**

**Communication**

Initialize  Module Found  Module NOT Found  OK  Warning

Module Found  
Vendor Part Number: HFRD-31.0

**Host Supplies**

**Receiver** 3.45 V 104 mA **Transmitter** 3.45 V 126 mA

**Monitor** | Interrupt Masks | Controls | Identification | Read/Write Byte | Options Available | HFRD-31.0 Settings

**Interrupt Flags: Channel Status**

**TX Fault**  TX1  TX2  TX3  TX4

**TX LOS**  TX1  TX2  TX3  TX4

**RX LOS**  RX1  RX2  RX3  RX4

**Flag Update Method**

Polling (2Hz rate)  
 Hardware Interrupt Line  
 Software Interrupt Bit

Indicates Flag is not asserted.  
 Indicates Flag is asserted.

History "ON" maintains flag history and does not clear flags. History "OFF" shows most recent flag status and clears with each update. "Clear" unconditionally clears flags. Use it to clear the history.

Items that are displayed as dim in intensity are not available or do not apply to the specific module. See "Options Available" page for vendor supplied features.

**History** OFF ON Clear

**Interrupt Flags: Channel Monitor**

**Alarms**

	High	Low
RX1 Power	<input type="radio"/>	<input type="radio"/>
RX2 Power	<input type="radio"/>	<input type="radio"/>
RX3 Power	<input type="radio"/>	<input type="radio"/>
RX4 Power	<input type="radio"/>	<input type="radio"/>
TX1 Bias	<input type="radio"/>	<input type="radio"/>
TX2 Bias	<input type="radio"/>	<input type="radio"/>
TX3 Bias	<input type="radio"/>	<input type="radio"/>
TX4 Bias	<input type="radio"/>	<input type="radio"/>
Mod VCC	<input type="radio"/>	<input type="radio"/>
Mod Temp	<input type="radio"/>	<input type="radio"/>

**Warnings**

	High	Low
RX1 Power	<input type="radio"/>	<input type="radio"/>
RX2 Power	<input type="radio"/>	<input type="radio"/>
RX3 Power	<input type="radio"/>	<input type="radio"/>
RX4 Power	<input type="radio"/>	<input type="radio"/>
TX1 Bias	<input type="radio"/>	<input type="radio"/>
TX2 Bias	<input type="radio"/>	<input type="radio"/>
TX3 Bias	<input type="radio"/>	<input type="radio"/>
TX4 Bias	<input type="radio"/>	<input type="radio"/>
Mod VCC	<input checked="" type="radio"/>	<input type="radio"/>
Mod Temp	<input type="radio"/>	<input type="radio"/>

**Measurements**

RX1 OMA	0.0 uW
RX2 OMA	0.0 uW
RX3 OMA	0.0 uW
RX4 OMA	0.0 uW
TX1 Bias	0.000 mA
TX2 Bias	0.000 mA
TX3 Bias	0.000 mA
TX4 Bias	0.000 mA
Mod VCC	3.34 V
Mod Temp	61 C

**History** OFF ON Clear

**History** OFF ON Clear

Figure 9. A typical status display from HFRD-32.0 QSFP Host Adapter.

## 6.2 HFRD-32.0 QSFP Host Adapter Software: HFRD-31.0 Specific Controls

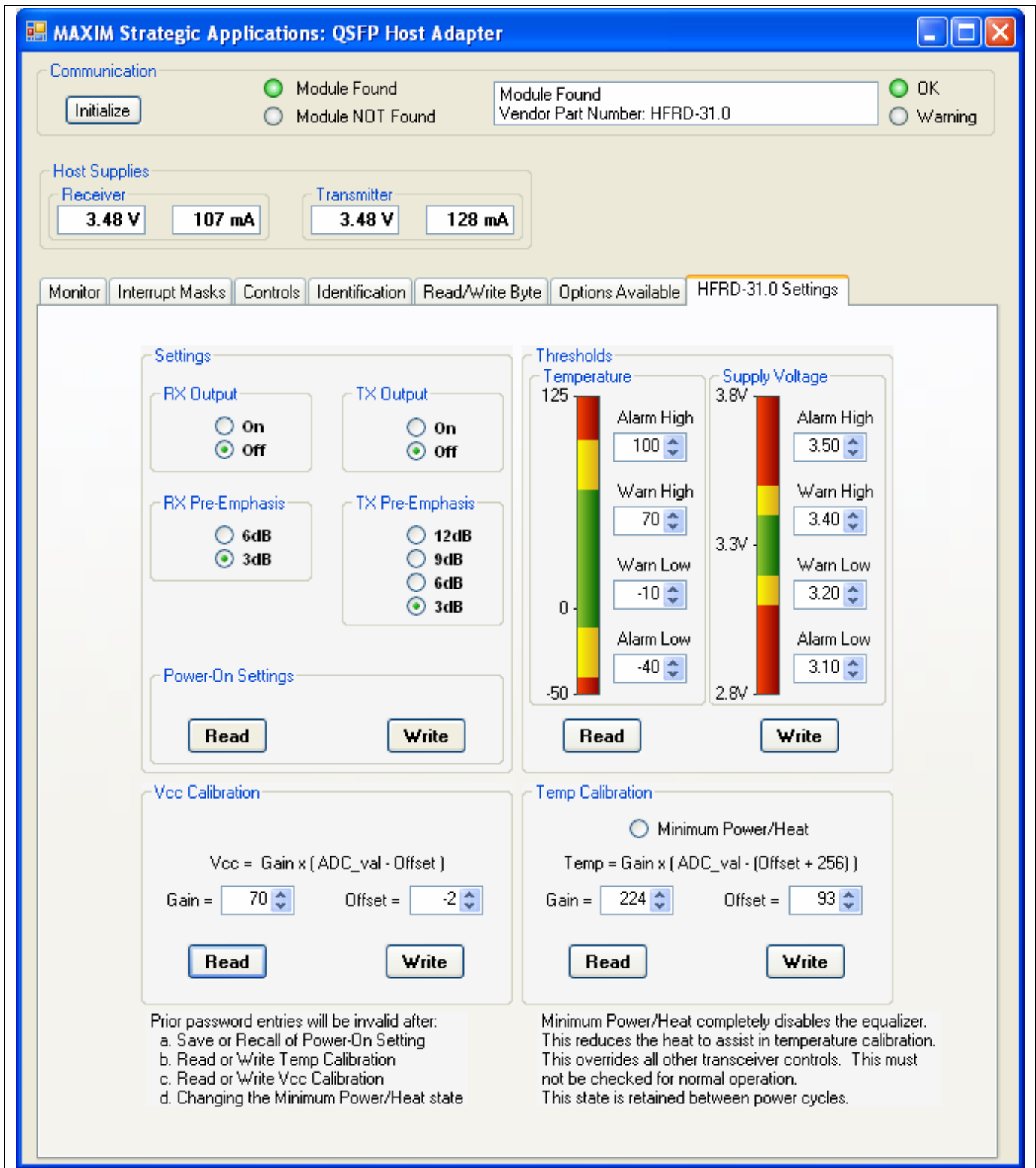


Figure 10. HFRD-32.0 displays the vendor-specific controls for HFRD-31.0. This menu is present only when the host adapter detects HFRD-31.0.



### 6.3 HFRD-32.0 QSFP Host Adapter Software: Bit-Level and Byte-Level Read/Write

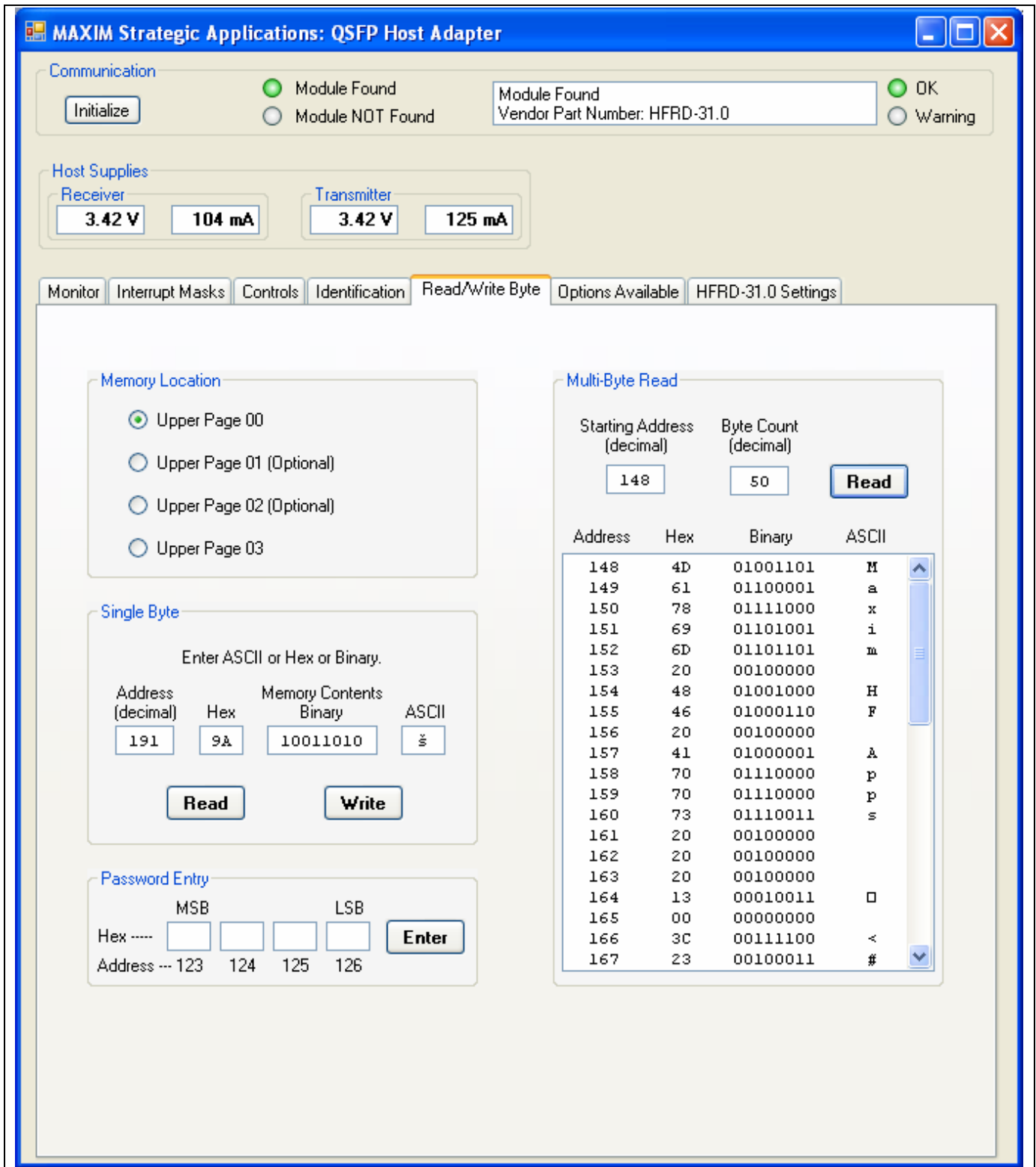


Figure 11. HFRD32.0 gives bit-level and byte-level access to all QSFP memory locations and contents.

## 7 Evaluation

### 7.1 Test Apparatus

The test apparatus is shown in Figure 12. The Agilent ParBERT™ pattern generator provided the data to fill the channels and introduced the aggressor signals. The Agilent 70843B supplied the “victim” signal. The HFRD-32.0 host adapter board provided the interface between the lab equipment and the cable assembly. The Tektronix CSA8000 oscilloscope produced the eye diagrams.

### 7.2 Results

Table 2 is a collection of eye diagrams for various data rates, cable lengths, pre-emphasis settings, and two wire gauges. These images capture the entire signal path shown in Figure 12: QSFP connectors;

approximately 5 inches 6mil, FR-4 microstrip, SMA connectors; and aggressor signals of 1V<sub>P-P</sub>. The eye diagrams also reveal some residual pre-emphasis from the receiver output. The minimum setting of 3dB, was used and some emphasis remains for a slightly longer distance to the host receiver.

Table 3 shows the difference in transmitter pre-emphasis for the single configuration of a 10m, 28AWG cable. It is important to note that the optimal jitter setting for 4.25Gbps and 5.0Gbps is different than at the lower rates. These lower rates benefit from the higher peaking because more time is required for the peaked transitions to settle before the next transition. When operating at 5.0Gbps, the 9dB of peaking (right side of table) actually degrades the signal. A choice of 6dB (left side of table) is a reasonable compromise if the operating range includes 4.25Gbps or greater.

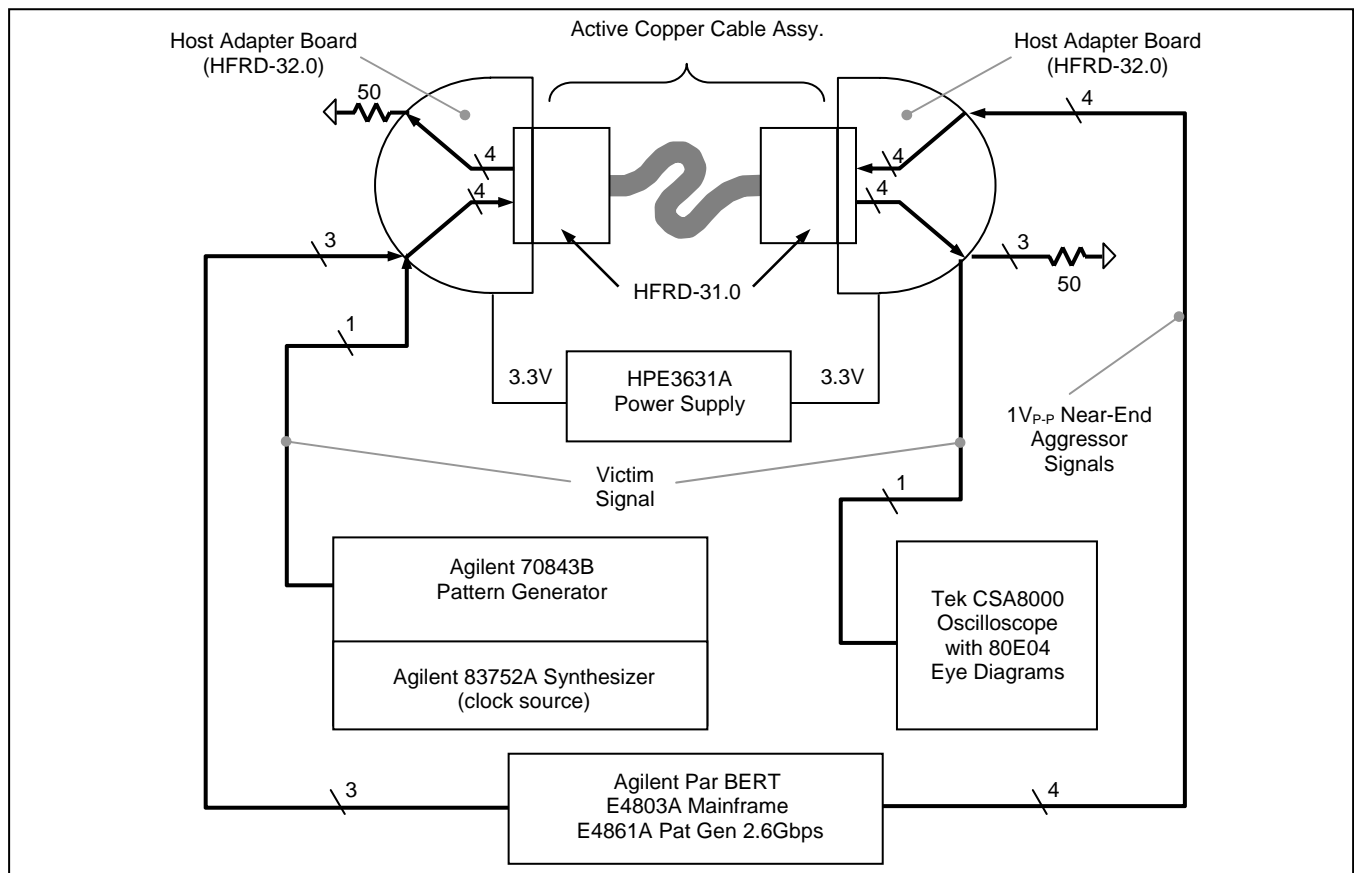
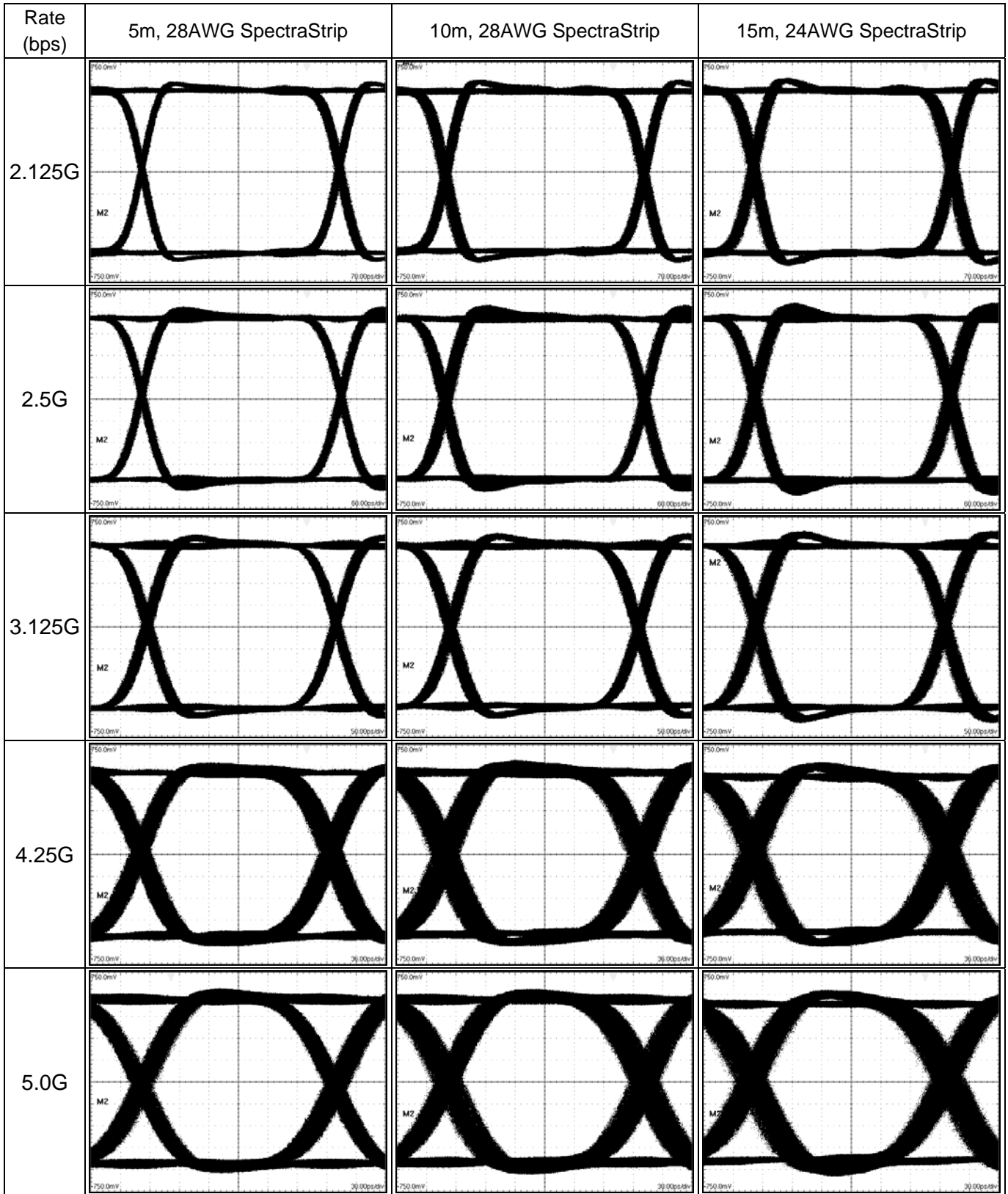


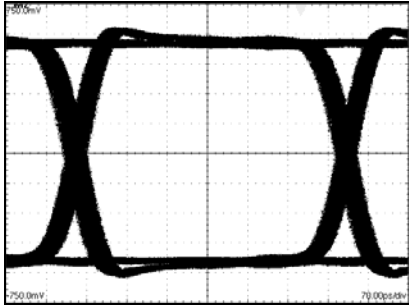
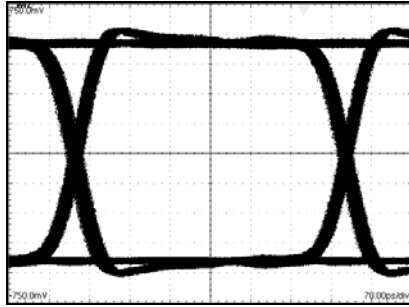
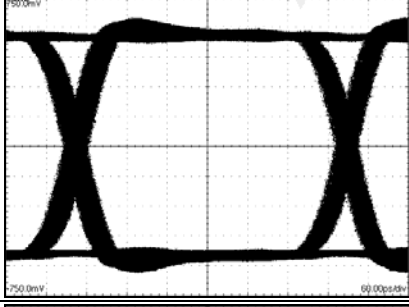
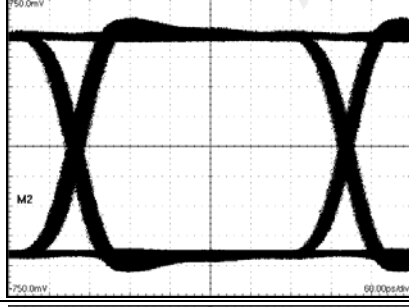
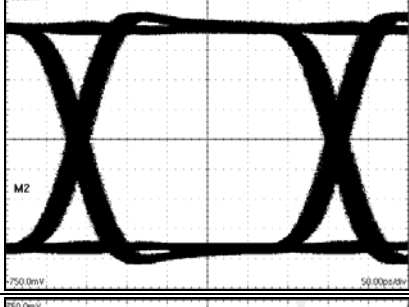
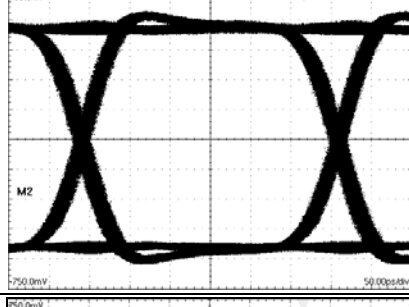
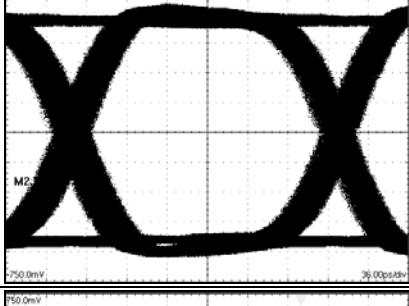
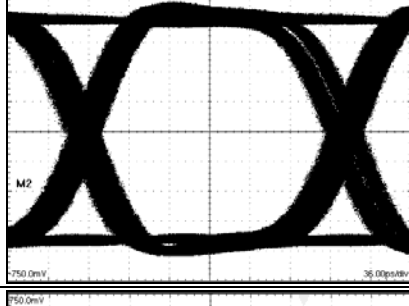
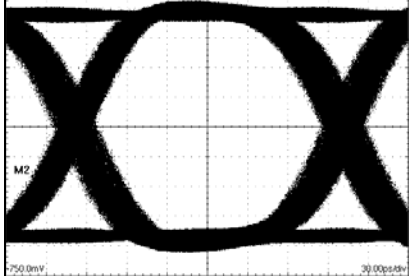
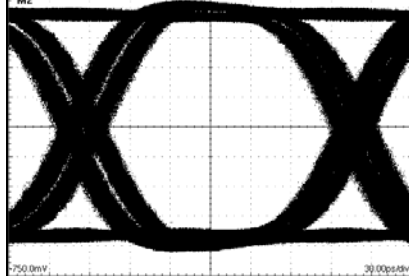
Figure 12. Test apparatus fills all channels to evaluate performance in the presence of interfering aggressor signals.

ParBERT is a trademark of the Agilent Technologies Inc

**Table 2. End-to-End Performance for Various Cables and Bit rate**



**Table 3. Comparison of 6dB and 9dB Compensation on 10m, 28AWG SpectraStrip**

Rate(bps)	6dB Transmitter Pre-Emphasis	9dB Transmitter Pre-Emphasis
2.125G		
2.5G		
3.125G		
4.25G		
5.0G		

# 8 Supporting Documentation

## 8.1 HFRD-31.0 Schematic, Sheet 1 of 2

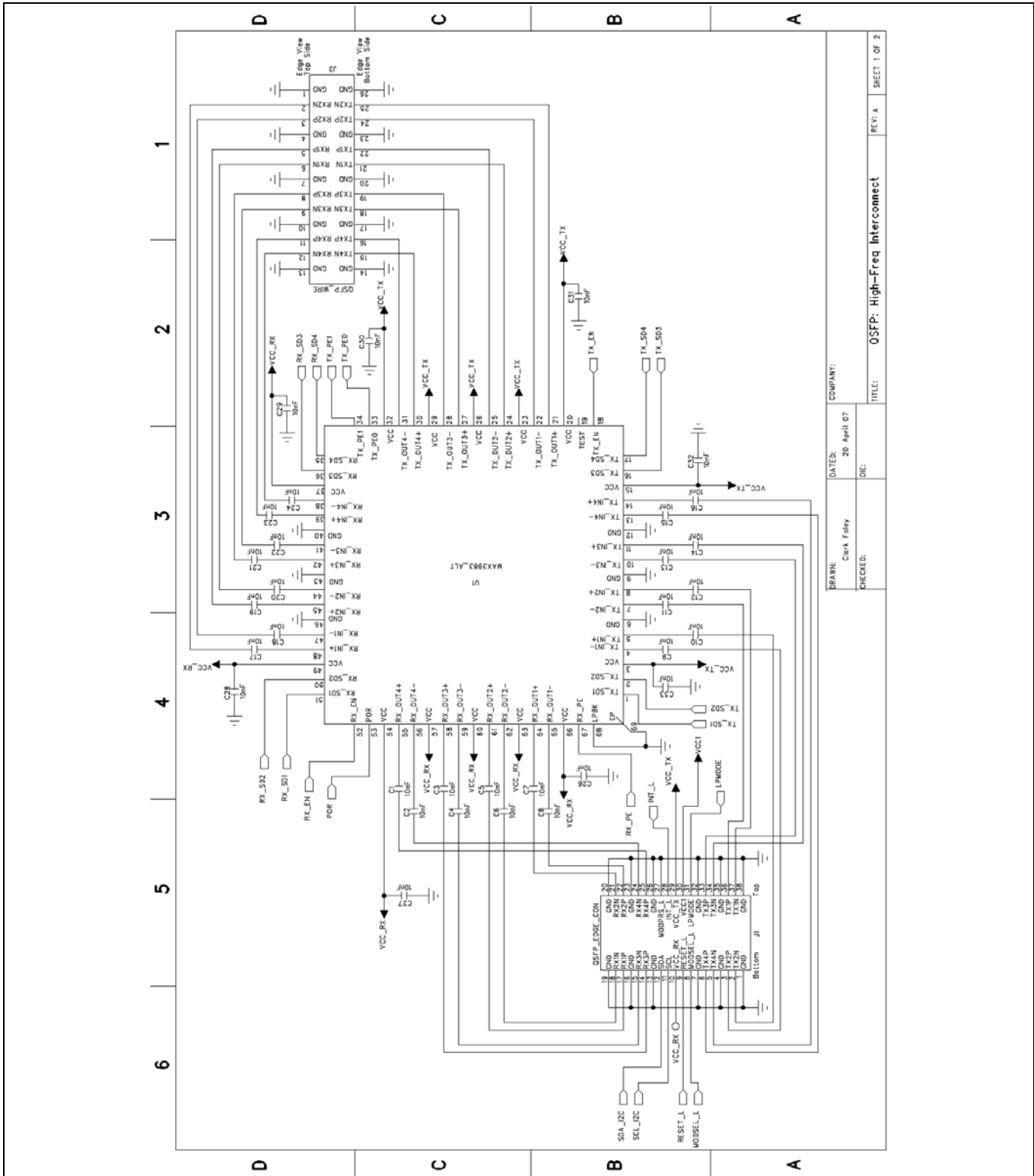


Figure 13. Schematic for HFRD-31.0 High-speed data and equalizer. The cable is wired to J2.

## 8.2 HFRD-31.0 Schematic, Sheet 2 of 2

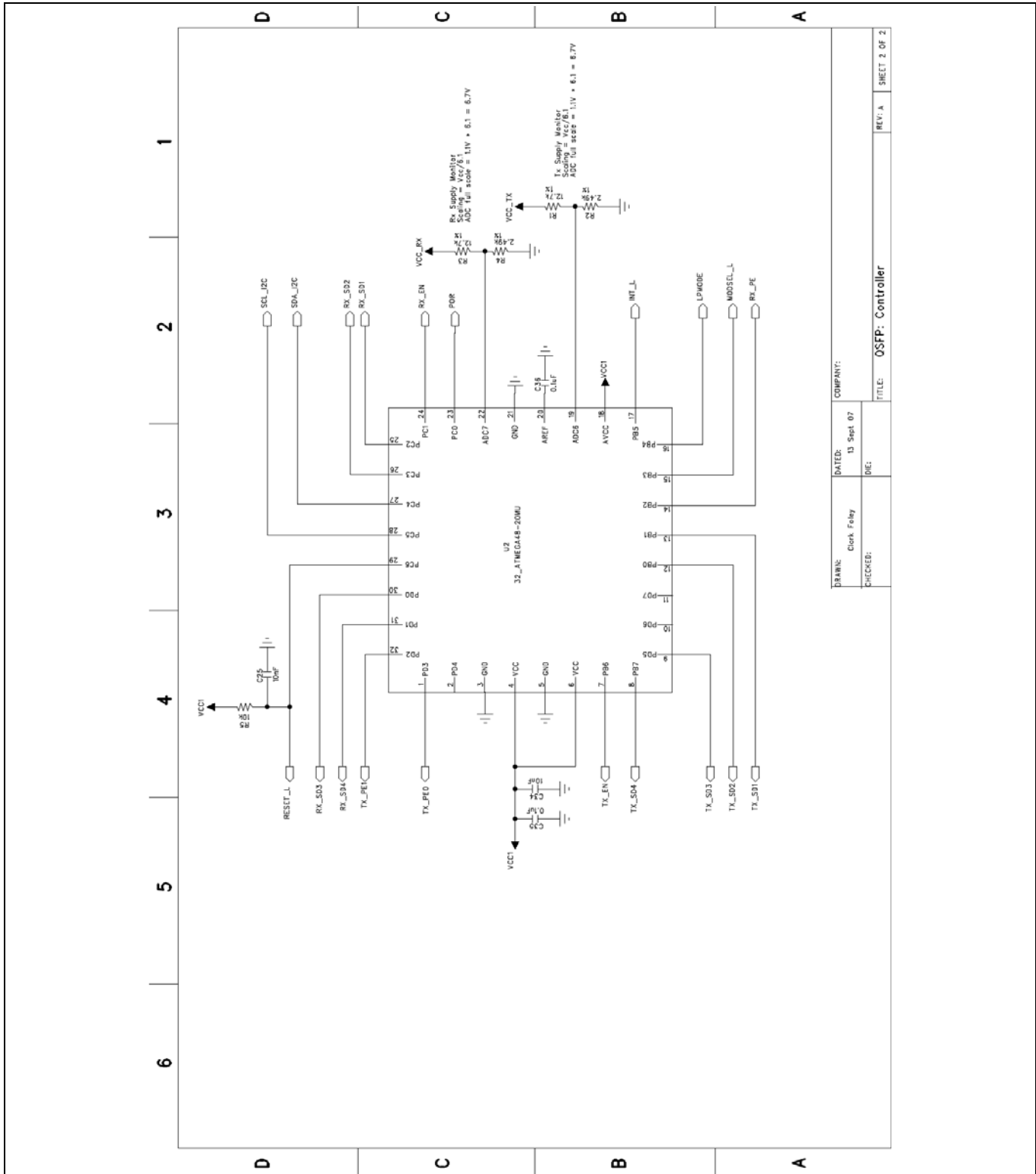


Figure 14. Schematic for HFRD-31.0, showing the micro-controller.



### 8.3 Artwork, HFRD-31.0

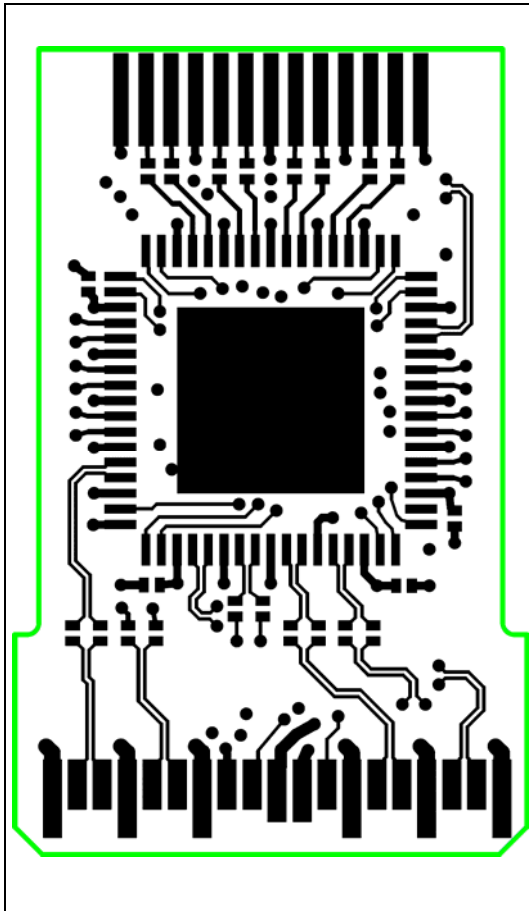


Figure 15. Layer 1 (top)

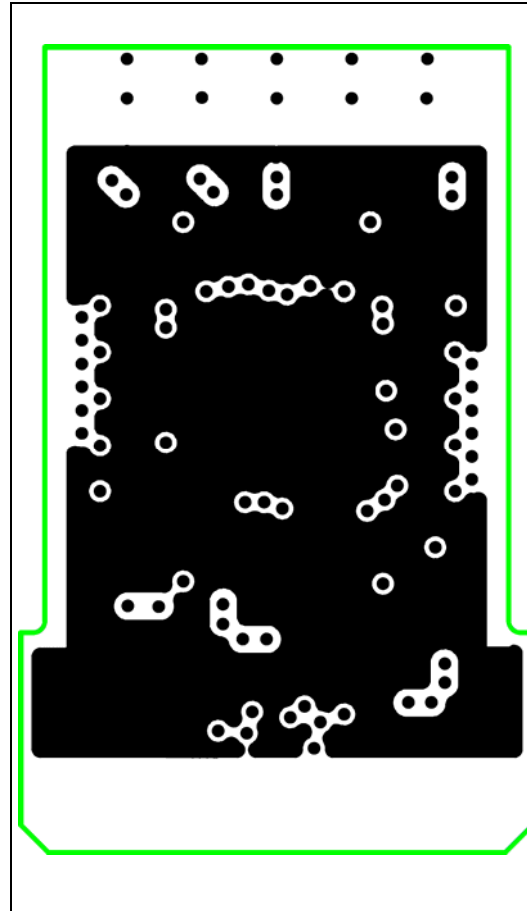


Figure 16. Layer 2, ground reference for top layer and layer 3 transmission lines.

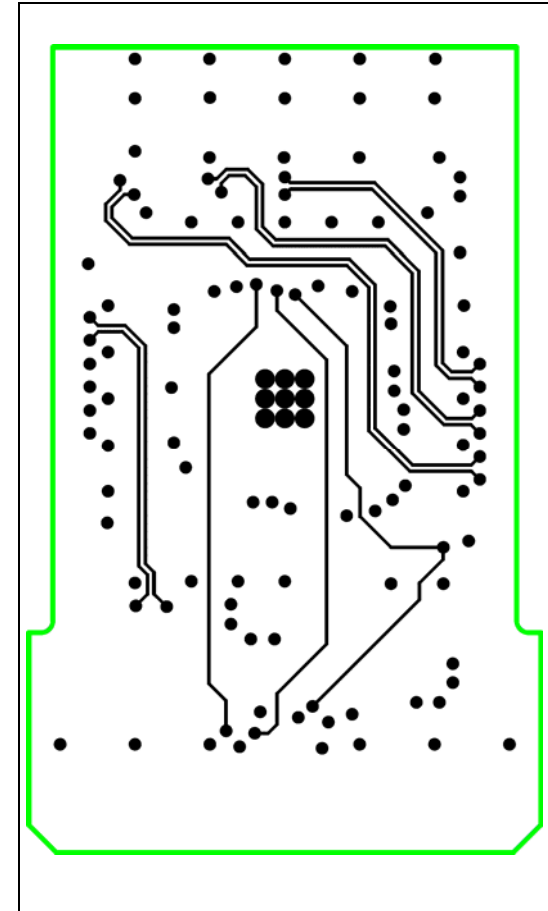


Figure 17. Layer 3, includes differential data lines referenced to layer 2. Layer 4 is relatively far away.

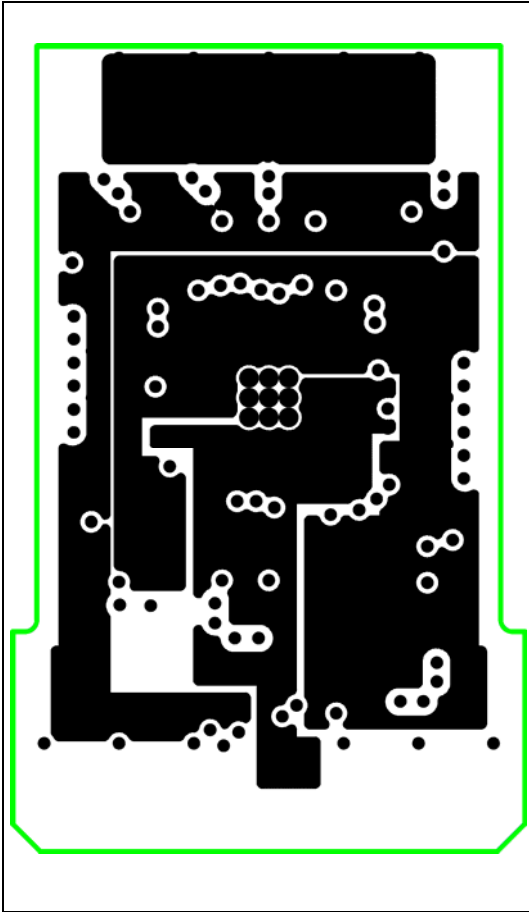


Figure 18. Layer 4, supply routing and ground patch to tie layer 5 and 2 together.

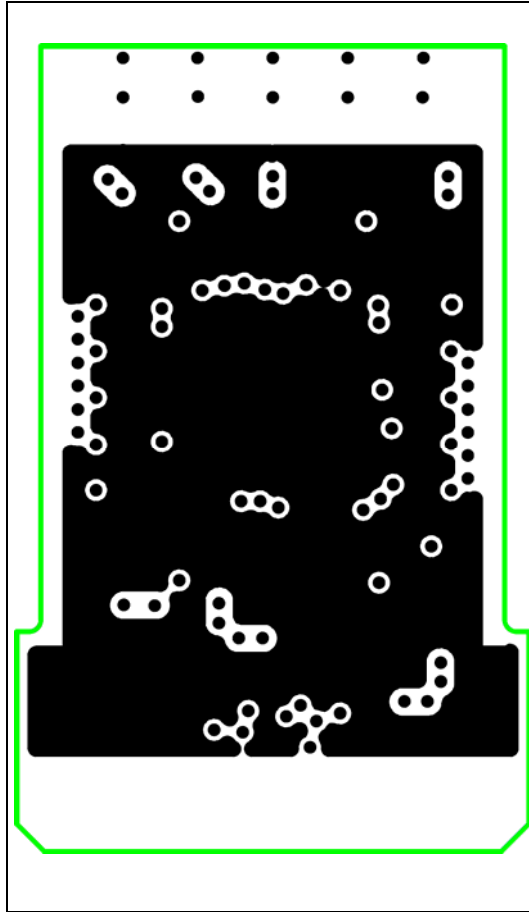


Figure 19. Layer 5, ground reference for bottom layer transmission lines.

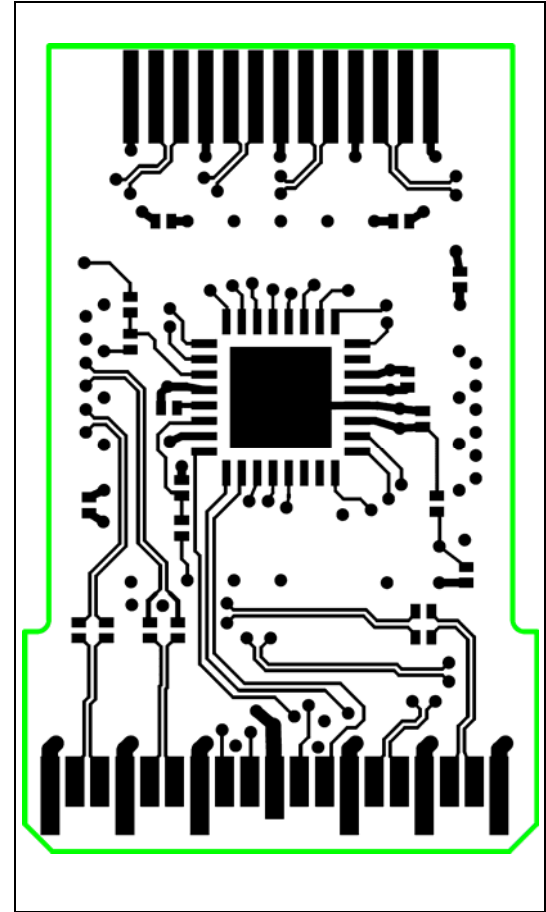


Figure 20. Layer 6 as viewed looking through the top layer.

## 8.4 Component Placement, Front Side of HFRD-31.0

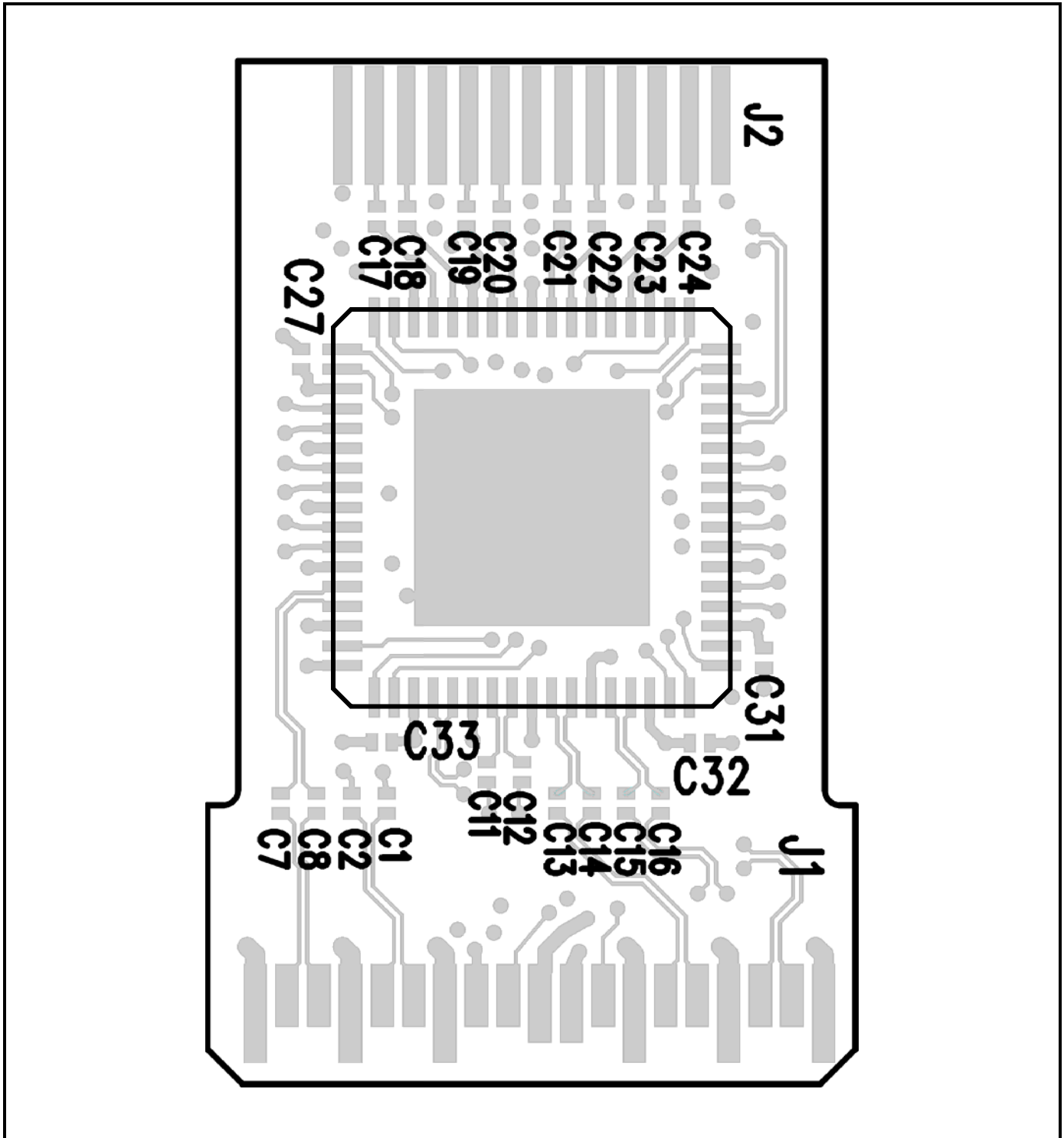


Figure 21. Top (front) layer. The receiver input portion of the cable is soldered to pins 1 through 13 of J2 at the top. J1 is the QSFP interface at the bottom.

## 8.5 Component Placement, Back Side of HFRD-31.0

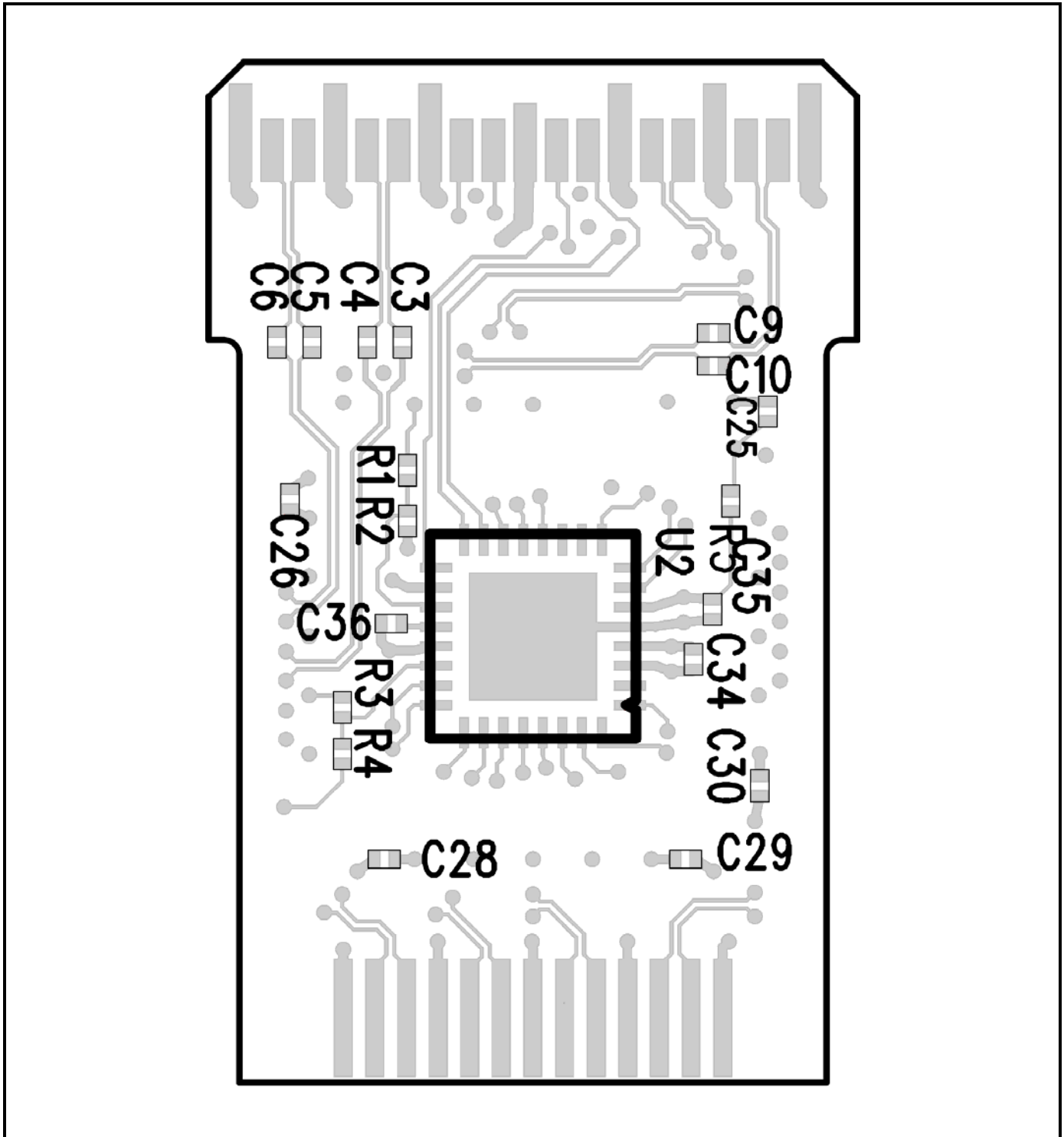
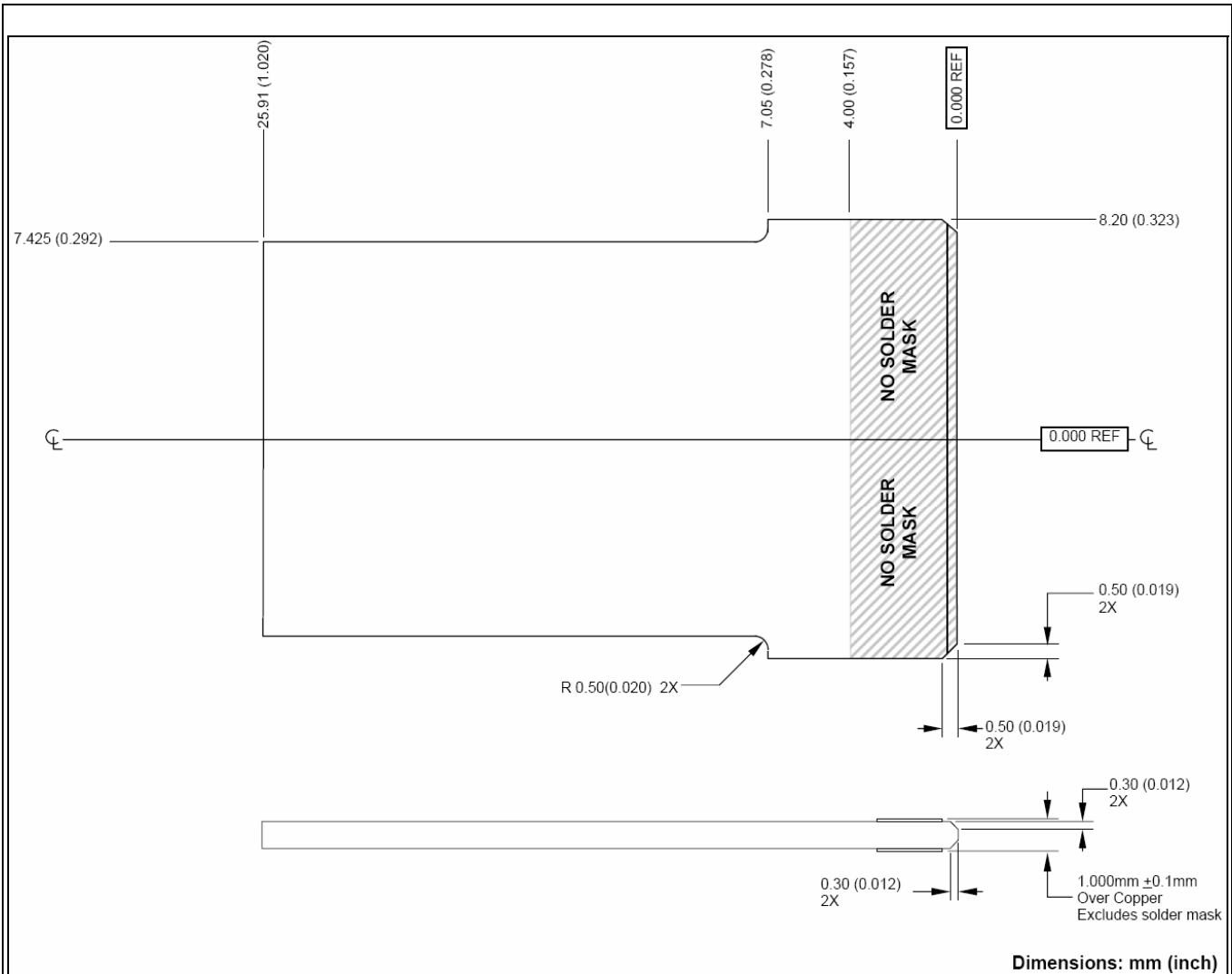


Figure 22. Bottom layer viewed from the bottom. The transmitter output portion of the cable is soldered to pins 14 through 26 at the bottom. The QSPF interface is at the top.

## 8.6 Mechanical Dimensions, HFRD-31.0



### 6-Layer Stack up

HF S	1oz Cu + Au ply/prepreg	2.0mil 4.0mil	(Diff 100ohm: W=4mil S=4mil / Single 50ohm: W=6mil)
GND	0.5oz Cu core	0.7mil 3.0mil	
HF S	0.5oz Cu ply/prepreg	0.7mil 18.6mil	(Diff 100ohm: W=4mil S=4mil / Single 50ohm: W=6mil)
Power	0.5oz Cu core	0.7mil 3.0mil	
GND	0.5oz Cu ply/prepreg	0.7mil 4.0mil	
HF S	1oz Cu + Au	2.0mil	(Diff 100ohm: W=4mil S=4mil, Single 50ohm: W=6mil)

Target is 1.0mm  $\pm$ 0.1mm (39.4mil  $\pm$ 4mil)

Figure 23. Dimensioned drawing and FR-4 board stackup (loss tangent = 0.02).

## 8.7 Bill of Materials

Qty	Reference	Value	Tolerance	Manufacturer	Description
1	U2			ATMEL	ATMEL ATMEGA48PV-10MU microcontroller
2	C35-36	0.1uF	10%		CERAMIC CAPACITOR (0201)
34	C1-34	10nF	10%		CERAMIC CAPACITOR (0201)
1	U1			Maxim	MAX3983UGK Equalizer/Signal Conditioner
1	J1				QSFP Edge Connector. Etched pattern on board.
1	J2				QSFP WIRE LANDING, BOARD FEATURE
1	R5	10k	5%		RESISTOR (0201)
2	R1 R3	12.7k	1%		RESISTOR (0201)
2	R2 R4	2.49k	1%		RESISTOR (0201)

## 8.8 Additional Materials Not Included

### Wire

8-pair, 24AWG shielded and balanced 100ohm cable, Amphenol SpectraStrip SkewClear, part number 166-2499-998.

8-pair, 28AWG shielded and balanced 100ohm cable, Amphenol SpectraStrip SkewClear, part number 166-2899-997.