2.8-W/Ch Stereo Class-D Audio Amplifier with SmartGain™ Dynamic Range Compression and AGC

FEATURES

- **Filter-Free Class-D Architecture**
- **3 SmartGain™ functions**
  - **AGC DRC Function**
  - **AGC Limiter Function**
  - **AGC Noise Gate Function**
- **1.7 W/Ch Into 8 Ω at 5 V (10% THD+N)**
- **750 mW/Ch Into 8 Ω at 3.6 V (10% THD+N)**
- **2.8 W/Ch Into 4 Ω at 5 V (10% THD+N)**
- **1.5 W/Ch Into 4 Ω at 3.6 V (10% THD+N)**
- **Power Supply Range: 2.5 V to 5.5 V**
- **Low Supply Current: 3.5 mA**
- **Low Shutdown Current: 0.2 µA**
- **High PSRR: 75 dB at 217 Hz**
- **Fast Start-up Time: 5 ms**
- **Short-Circuit and Thermal Protection**
- **Space-Saving Package**
  - **4 mm × 4 mm QFN (RTJ)**

APPLICATIONS

- **Wireless or Cellular Handsets and PDAs**
- **Portable Navigation Devices**
- **Portable DVD Player**
- **Notebook PCs**
- **Portable Radio**
- **Portable Games**
- **Educational Toys**
- **USB Speakers**

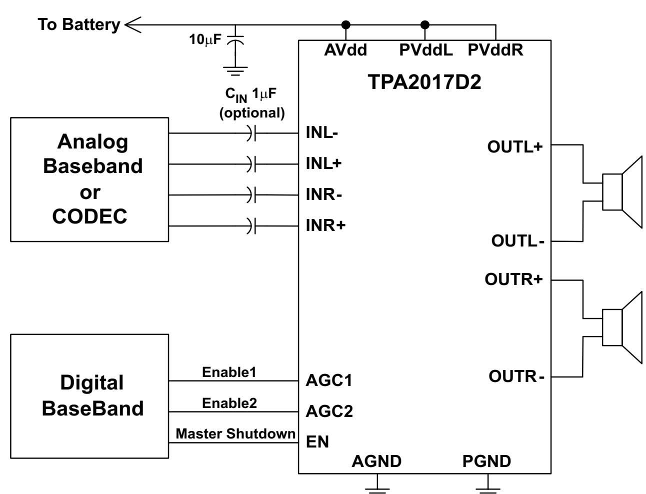
DESCRIPTION

The TPA2017D2 (sometimes referred to as TPA2017) is a stereo, filter-free Class-D audio power amplifier with SmartGain™ dynamic range compression (DRC), automatic gain control (AGC), and noise gate. It is available in a 4 mm x 4mm QFN package.

SmartGain™ functions are configured to automatically prevent distortion of the audio signal and enhance quiet passages that are normally not heard. SmartGain™ is a combined AGC DRC and Limiter that protects the speaker from damage at high power levels and compress the dynamic range of voice or music to fit within the dynamic range of the speaker. SmartGain™ DRC, limiter, and noise gate functions can be enabled or disabled. The TPA2017D2 (TPA2017) is capable of driving 1.7 W/Ch at 4 V or 750mW/Ch at 3.6 V into 8 Ω load or 2.8 W/Ch at 5 V or 1.5 W/Ch at 3.6 V into 4 Ω. The device features an enable pin and also provides thermal and short circuit protection.

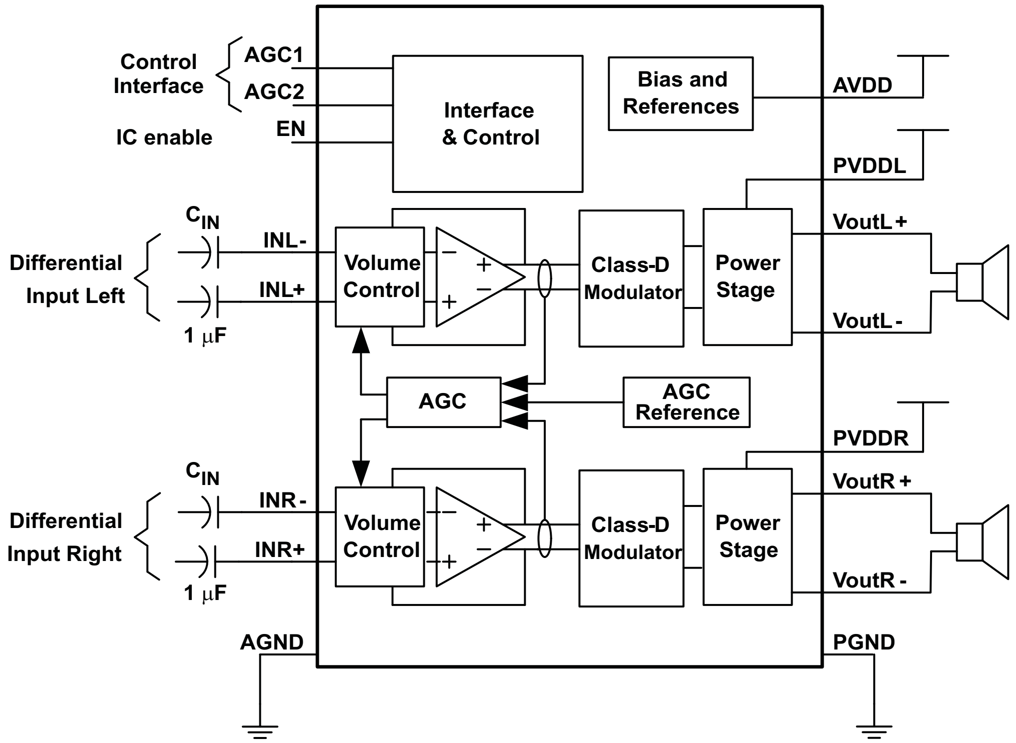
In addition to these features, a fast start-up time and small package size make the TPA2017D2 (TPA2017) an ideal choice for Notebook PCs, PDAs and other portable applications.

SIMPLIFIED APPLICATION DIAGRAM

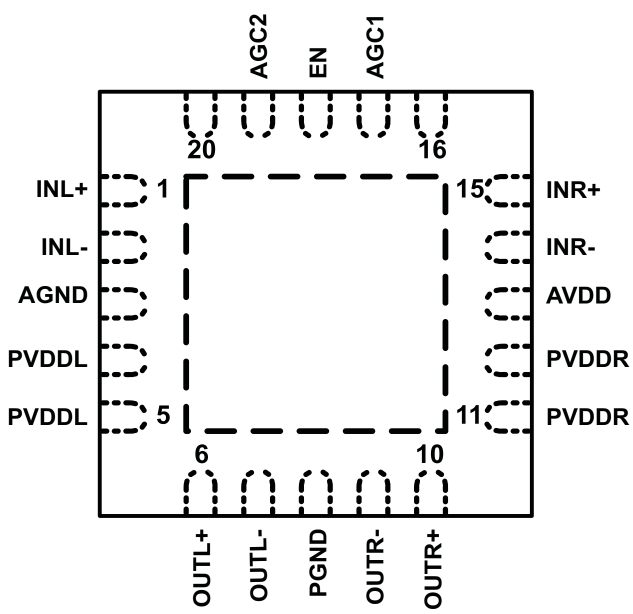


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



DEVICE PINOUT
RTJ (QFN) PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O/P	DESCRIPTION
NAME	QFN		
INR+	15	I	Right channel positive audio input
INR–	14	I	Right channel negative audio input
INL+	1	I	Left channel positive audio input
INL–	2	I	Left channel negative audio input
EN	18	I	Enable terminal (active high)
AGC2	19	I	AGC select function pin 2
AGC1	17	I	AGC select function pin 1
OUTR+	10	O	Right channel positive differential output
OUTR–	9	O	Right channel negative differential output
OUTL+	6	O	Left channel positive differential output
OUTL–	7	O	Left channel negative differential output
AVDD	13	P	Analog supply (must be the same as PVDDR and PVDDL)
AGND	3	P	Analog ground (all GND pins need to be connected)
PVDDR	11, 12	P	Right channel power supply (must be the same as AVDD and PVDDL)
PGND	8	P	Power ground (all GND pins need to be connected)
PVDDL	4, 5	P	Left channel power supply (must be the same as AVDD and PVDDR)

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted).

			VALUE / UNIT
V_{DD}	Supply voltage	AVDD, PVDDR, PVDDL	–0.3 V to 6 V
	Input voltage	INR+, INR–, INL+, INL–	–0.3 V to V_{DD}+0.3 V
		EN, AGC1, AGC2	–0.3 V to 6 V
	Continuous total power dissipation		See Dissipation Ratings Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
ESD	Electro-Static Discharge Tolerance, all pins	Human Body Model (HBM)	2 KV
		Charged Device Model (CDM)	500 V
R_{LOAD}	Minimum load resistance		3.6 Ω

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS TABLE(1)

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
20-pin QFN	5.2 W	41.6 mW/°C	3.12 W	2.7 W

(1) Dissipations ratings are for a 2-side, 2-plane PCB.

AVAILABLE OPTIONS[(1)]

T_A	PACKAGED DEVICES[(2)]	PART NUMBER	SYMBOL
–40°C to 85°C	20-pin, 4 mm × 4 mm QFN (RTJ)	TPA2017D2RTJR	–
		TPA2017D2RTJT	–

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com

(2) The RTJ packages are only available taped and reeled. The suffix R indicates a reel of 3000; the suffix T indicates a reel of 250.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage	AVDD, PVDDR, PVDDL	2.5	5.5	V
V_{IH}	High-level input voltage	EN, AGC1, AGC2	1.3		V
V_{IL}	Low-level input voltage	EN, AGC1, AGC2		0.6	V
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

at T_A = 25°C, V_{DD} = 3.6 V, EN = 1.3 V, and R_L = 8 Ω + 33 µH (unless otherwise noted).

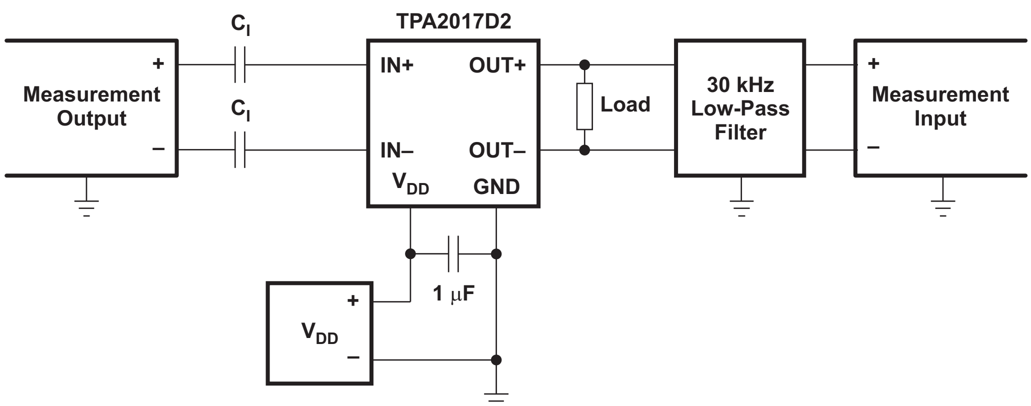
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		2.5	3.6	5.5	V
I_{SD}	Shutdown quiescent current	EN = 0.35 V, V_{DD} = 2.5 V		0.1	1	µA
		EN = 0.35 V, V_{DD} = 3.6 V		0.2	1	
		EN = 0.35 V, V_{DD} = 5.5 V		0.3	1	
I_{DD}	Supply current	V_{DD} = 2.5 V		3.5	4.9	mA
		V_{DD} = 3.6 V		3.7	5.1	
		V_{DD} = 5.5 V		4.5	5.5	
f_{SW}	Class D Switching Frequency		275	300	325	kHz
I_{IH}	High-level input current	V_{DD} = 5.5 V, EN = 5.8 V			1	µA
I_{IL}	Low-level input current	V_{DD} = 5.5 V, EN = –0.3 V	–1			µA
t_{START}	Start-up time	2.5 V ≤ V_{DD} ≤ 5.5 V no pop, C_{IN} ≤ 1 µF		5		ms
POR	Power on reset ON threshold			2	2.3	V
	Power on reset hysteresis			0.2		V
CMRR	Input common mode rejection	R_L = 8 Ω, V_{icm} = 0.5 V and V_{icm} = V_{DD} – 0.8 V, differential inputs shorted		–70		dB
V_{oo}	Output offset voltage	V_{DD} = 3.6 V, A_V = 6 dB, R_L = 8 Ω, inputs ac grounded	–10	0	10	mV
Z_O	Output Impedance in shutdown mode	EN = 0.35 V		2		kΩ
	Gain accuracy	Compression and limiter disabled, Gain = 0 to 30 dB	–0.75		0.75	dB
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 4.7 V		–80		dB

OPERATING CHARACTERISTICS

at T_A = 25°C, V_{DD} = 3.6V, EN = 1.3 V, R_L = 8 Ω +33 µH, and A_V = 6 dB (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
k_{SVR}	power-supply ripple rejection ratio	V_{DD} = 3.6 Vdc with ac of 200 mV_{PP} at 217 Hz		–68		dB
THD+N	Total harmonic distortion + noise	f_{aud_in} = 1 kHz; P_O = 550 mW; V_{DD} = 3.6 V		0.1%		
		f_{aud_in} = 1 kHz; P_O = 1 W; V_{DD} = 5 V		0.1%		
		f_{aud_in} = 1 kHz; P_O = 630 mW; V_{DD} = 3.6 V		1%		
		f_{aud_in} = 1 kHz; P_O = 1.4 W; V_{DD} = 5 V		1%		
N_r	Output integrated noise	Av = 6 dB		44		µV
		Av = 6 dB floor, A-weighted		33		µV
f	Frequency response	Av = 6 dB	20		20000	Hz
$P_{O(max)}$	Maximum output power	THD+N = 10%, V_{DD} = 5 V, R_L = 4 Ω		2.8		W
		THD+N = 10%, V_{DD} = 3.6 V, R_L = 4 Ω		1.5		W
		THD+N = 10%, V_{DD} = 5 V, R_L = 8 Ω		1.4		W
		THD+N = 10% , V_{DD} = 3.6 V, R_L = 8 Ω		630		mW
η	Efficiency	THD+N = 1%, V_{DD} = 3.6 V, R_L = 8 Ω, P_O= 0.63 W		90%		
		THD+N = 1%, V_{DD} = 5 V, R_L = 8 Ω, P_O = 1.4 W		90%		

TEST SET-UP FOR GRAPHS



(1) All measurements were taken with a 1-µF C_I (unless otherwise noted.)

(2) A 33-µH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.

(3) The 30-kHz low-pass filter is required, even if the analyzer has an internal low-pass filter. An RC low-pass filter (1 kΩ 4.7 nF) is used on each output for the data sheet graphs.

TYPICAL CHARACTERISTICS

with $C_{(DECOUPLE)}$ = 1 µF, C_I = 1 µF, AGC1 = AGC2 = 0 V.
All THD + N graphs are taken with outputs out of phase (unless otherwise noted).
All data is taken on left channel.

Table of Graphs

		FIGURE
Quiescent supply current	vs Supply voltage	Figure 1
Output Level	vs Input Level	Figure 2
Output power	vs Supply voltage	Figure 3
Total harmonic distortion + noise at 2.5 V	vs Frequency	Figure 4
Total harmonic distortion + noise at 3.6 V	vs Frequency	Figure 5
Total harmonic distortion + noise at 5 V	vs Frequency	Figure 6
Total harmonic distortion + noise	vs Output power at 8 Ω	Figure 7
Total harmonic distortion + noise	vs Output power at 4 Ω	Figure 8
Efficiency	vs Output power (per channel) at 8 Ω	Figure 9
Efficiency	vs Output power (per channel) at 4 Ω	Figure 10
Total power dissipation	vs Total output power at 8 Ω	Figure 11
Total power dissipation	vs Total output power at 4 Ω	Figure 12
Total supply current	vs Total output power at 8 Ω	Figure 13
Total supply current	vs Total output power at 4 Ω	Figure 14
Supply ripple rejection ratio	vs Frequency	Figure 15
Crosstalk	vs Frequency	Figure 16
Shutdown time		Figure 17
Startup time		Figure 18

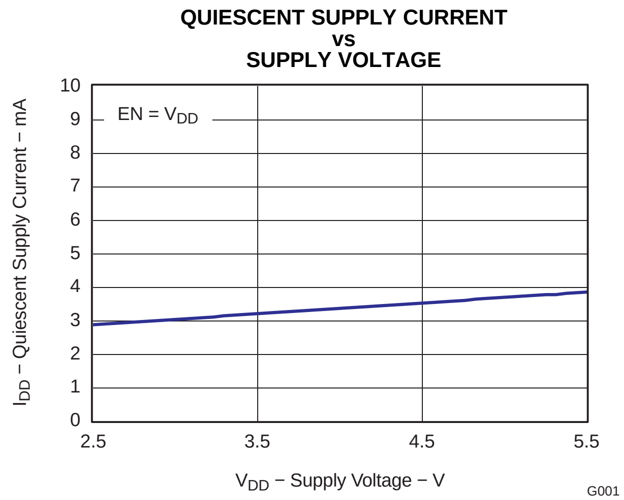


Figure 1.

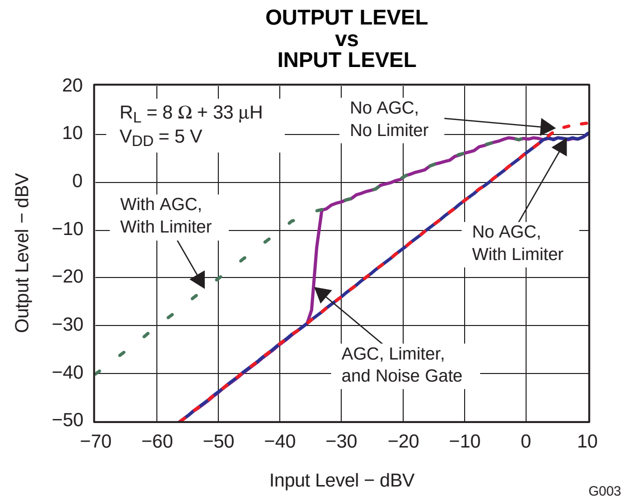


Figure 2.

OUTPUT POWER
vs
SUPPLY VOLTAGE

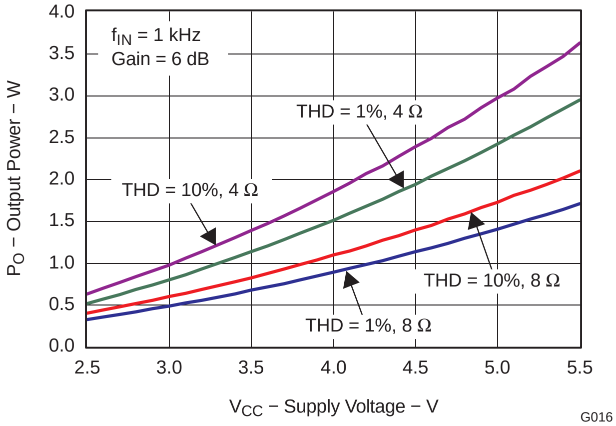


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

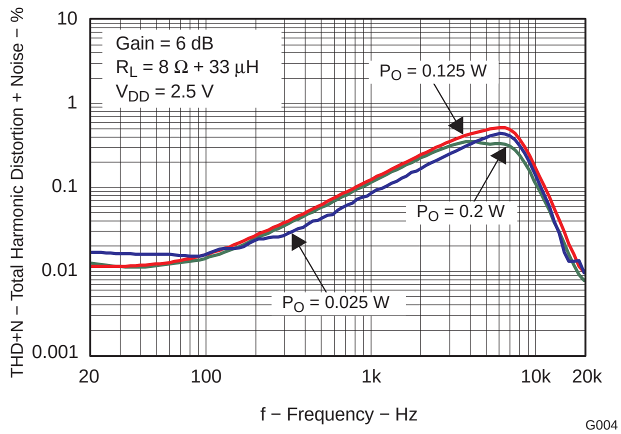


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

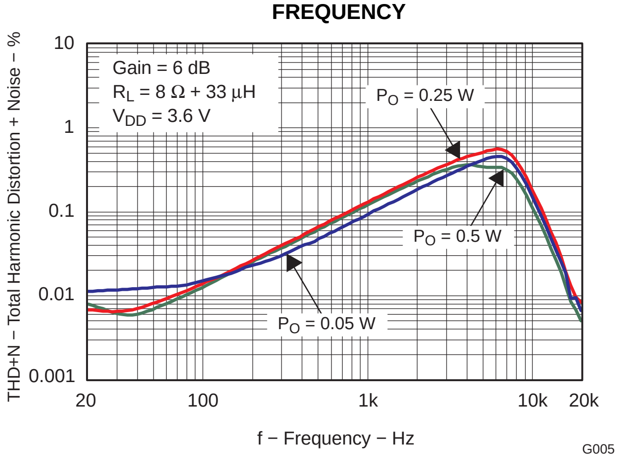


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

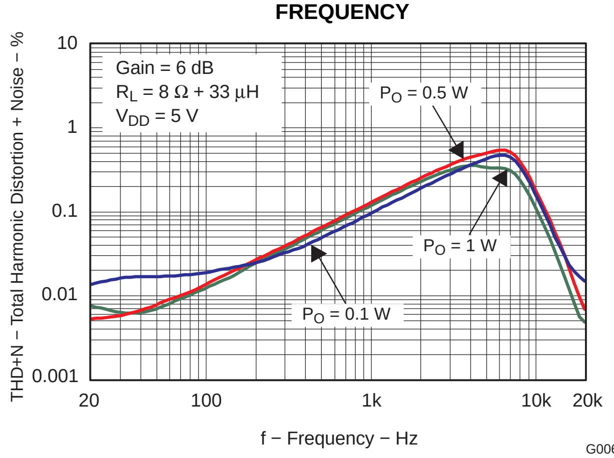


Figure 6.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

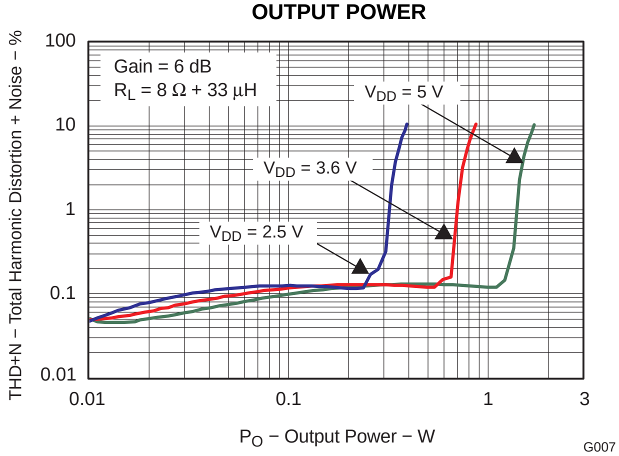


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

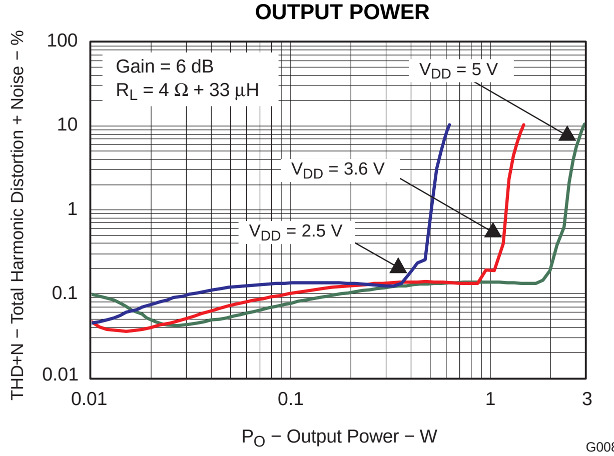


Figure 8.

EFFICIENCY vs OUTPUT POWER (PER CHANNEL)

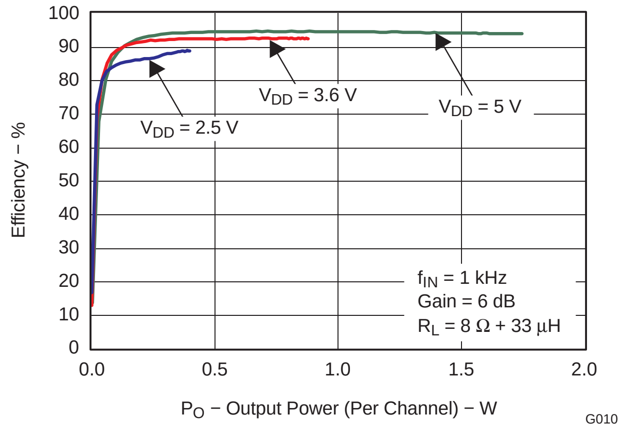


Figure 9.

EFFICIENCY vs OUTPUT POWER (PER CHANNEL)

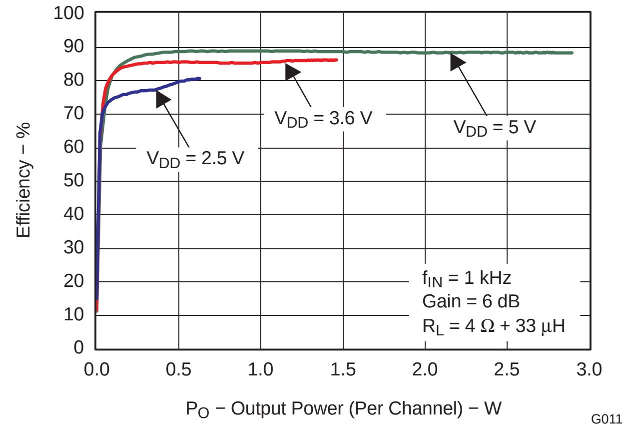


Figure 10.

TOTAL POWER DISSIPATION vs TOTAL OUTPUT POWER

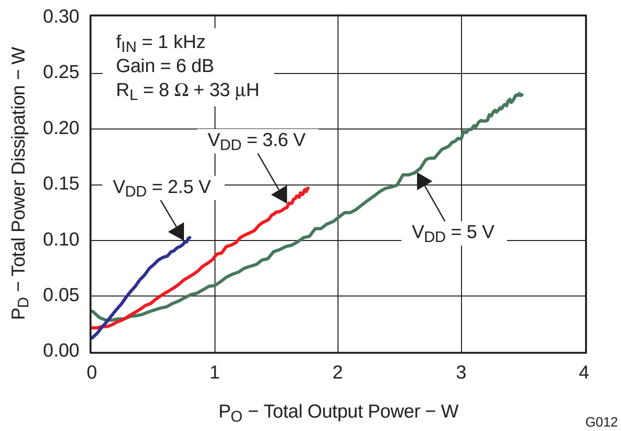


Figure 11.

TOTAL POWER DISSIPATION vs TOTAL OUTPUT POWER

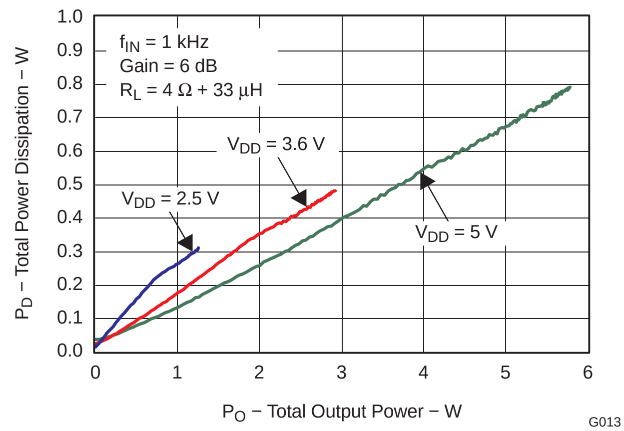


Figure 12.

TOTAL SUPPLY CURRENT vs TOTAL OUTPUT POWER

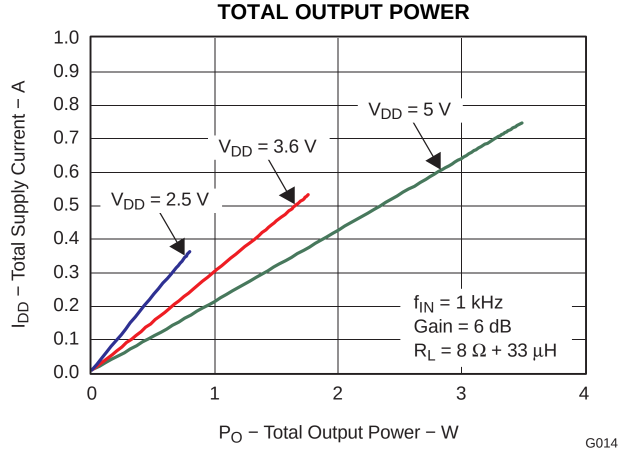


Figure 13.

TOTAL SUPPLY CURRENT vs TOTAL OUTPUT POWER

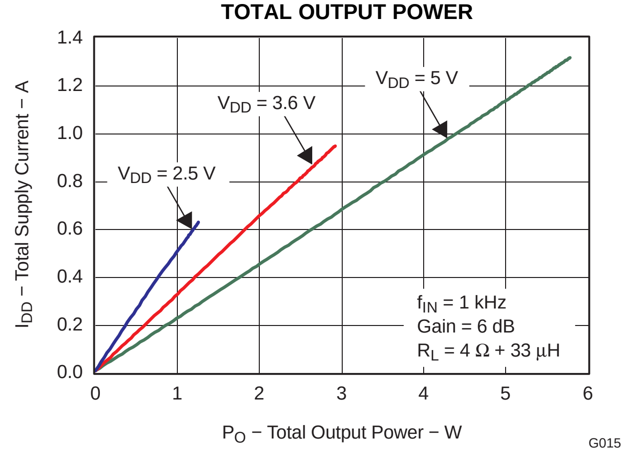


Figure 14.

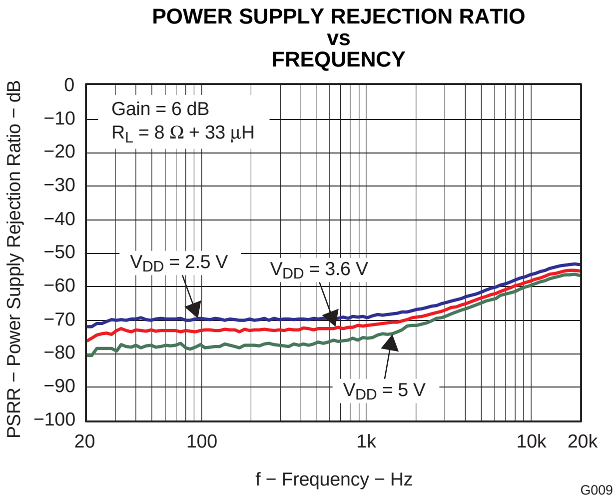


Figure 15.

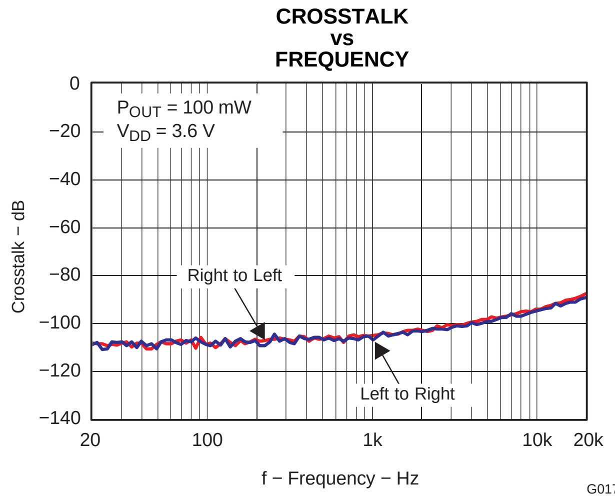


Figure 16.

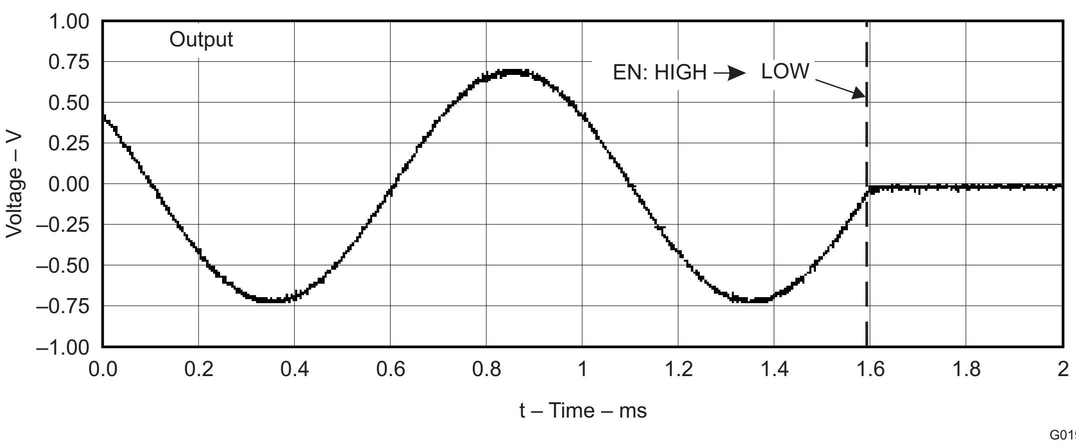


Figure 17. Shutdown Time

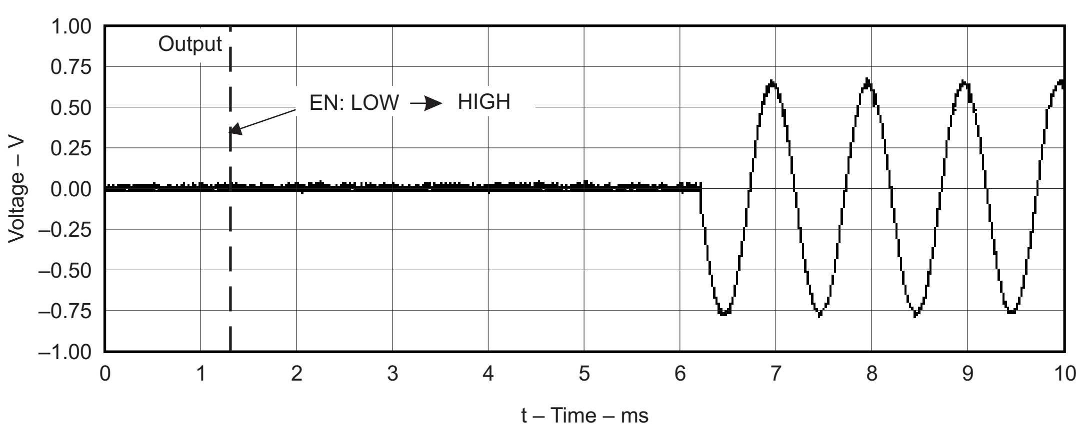


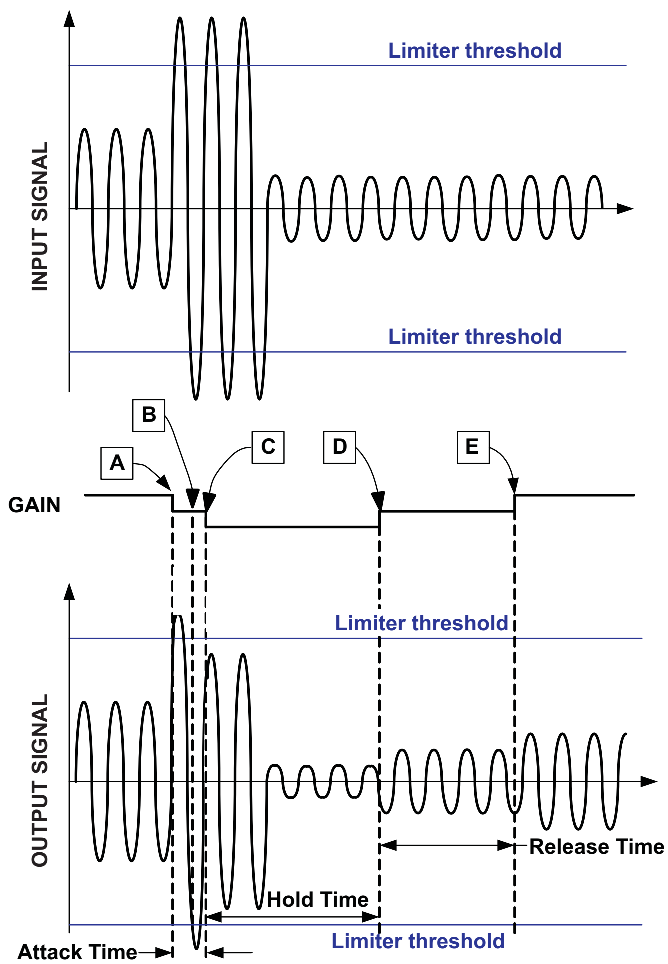
Figure 18. Startup Time

APPLICATION INFORMATION

AUTOMATIC GAIN CONTROL

The Automatic Gain Control (AGC) feature provides continuous automatic gain adjustment to the amplifier through an internal PGA. This feature enhances the perceived audio loudness and at the same time prevents speaker damage from occurring (Limiter function).

The AGC works by detecting the audio input envelope. The gain changes depending on the amplitude, the limiter level, the compression ratio, and the attack and release time. The gain changes constantly as the audio signal increases and/or decreases to create the compression effect. The gain step size for the AGC is 0.5 dB. If the audio signal has near-constant amplitude, the gain does not change. Figure 19 shows how the AGC works.



A. Gain decreases with no delay; attack time is reset. Release time and hold time are reset.

B. Signal amplitude above limiter level, but gain cannot change because attack time is not over.

C. Attack time ends; gain is allowed to decrease from this point forward by one step. Gain decreases because the amplitude remains above limiter threshold. All times are reset

D. Gain increases after release time finishes and signal amplitude remains below desired level. All times are reset after the gain increase.

E. Gain increases after release time is finished again because signal amplitude remains below desired level. All times are reset after the gain increase.

Figure 19. Input and Output Audio Signal vs Time

Since the number of gain steps is limited the compression region is limited as well. The following figure shows how the gain changes vs. the input signal amplitude in the compression region.

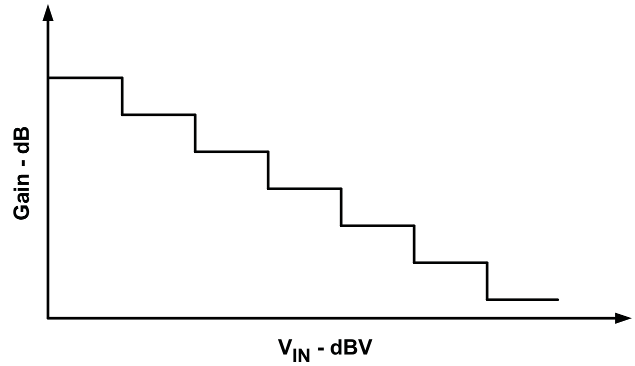


Figure 20. Input Signal Voltage vs Gain

Thus the AGC performs a mapping of the input signal vs. the output signal amplitude.

Pins AGC1 and AGC 2 are used to enable/disable the limiter, compression, and noise gate function. Table 1 shows each function.

Table 1. FUNCTION DEFINITION FOR AGC1 AND AGC2

AGC1	AGC2	Function
0	0	AGC Function disabled
0	1	AGC Limiter Function enabled
1	0	AGC, Limiter, and Compression Functions enabled
1	1	AGC, Limiter, Compression, and Noise Gate Functions enabled

The default values for the TPA2017D2 AGC function are given in Table 2. The default values can be changed at the factory during production. Refer to the TI representative for assistance with different default value requests.

Table 2. AGC DEFAULT VALUES

Attack Time	6.4 ms / step
Release Time	1.81 sec/step
Fixed Gain	6 dB
NoiseGate Threshold	20 mV
Output Limiter Level	9 dBV
Max Gain	30 dB
Compression Ratio	2:1

DECOUPLING CAPACITOR (C_S)

The TPA2017D2 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) 1-μF ceramic capacitor (typically) placed as close as possible to the device PVDD (L, R) lead works best. Placing this decoupling capacitor close to the TPA2017D2 is important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 4.7 μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

INPUT CAPACITORS (C_I)

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_C, determined in Equation 1.

$$f_C = \frac{1}{(2\pi \times R_I \times C_I)} \tag{1}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset. Equation 2 is used to solve for the input coupling capacitance. If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

$$C_I = \frac{1}{(2\pi \times R_I \times f_C)} \tag{2}$$

COMPONENT LOCATION

Place all the external components very close to the TPA2017D2. Placing the decoupling capacitor, C_S, close to the TPA2017D2 is important for the efficiency of the Class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the packages are shown in the dissipation rating table. Converting this to θ_{JA} for the WCSP package:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.01} = 100°\text{C/W} \tag{3}$$

Given θ_{JA} of 100°C/W, the maximum allowable junction temperature of 150°C, and the maximum internal dissipation of 0.4 W (0.2 W per channel) for 1.5 W per channel, 8-Ω load, 5-V supply, from Figure 9, the maximum ambient temperature can be calculated with the following equation.

$$T_A\text{Max} = T_J\text{Max} - \theta_{JA}P_{DMAX} = 150 - 100\ (0.4) = 110°\text{C} \tag{4}$$

Equation 4 shows that the calculated maximum ambient temperature is 110°C at maximum power dissipation with a 5-V supply and 8-Ω a load. The TPA2017D2 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 8-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

OPERATION WITH DACS AND CODECS

In using Class-D amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when mixing of the output frequencies of the CODEC/DAC mix with the switching frequencies of the audio amplifier input stage. The noise increase can be solved by placing a low-pass filter between the CODEC/DAC and audio amplifier. This filters off the high frequencies that cause the problem and allow proper performance. See the functional block diagram.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1 MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker. Figure 21 shows typical ferrite bead and LC output filters.

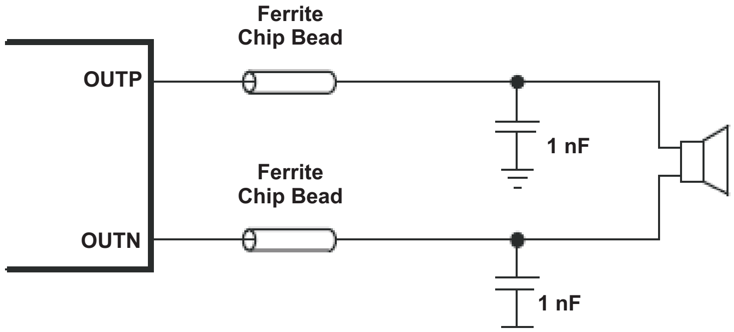


Figure 21. Typical Ferrite Bead Filter (Chip bead example: TDK: MPZ1608S221A)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA2017D2RTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA 2017D2	Samples
TPA2017D2RTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA 2017D2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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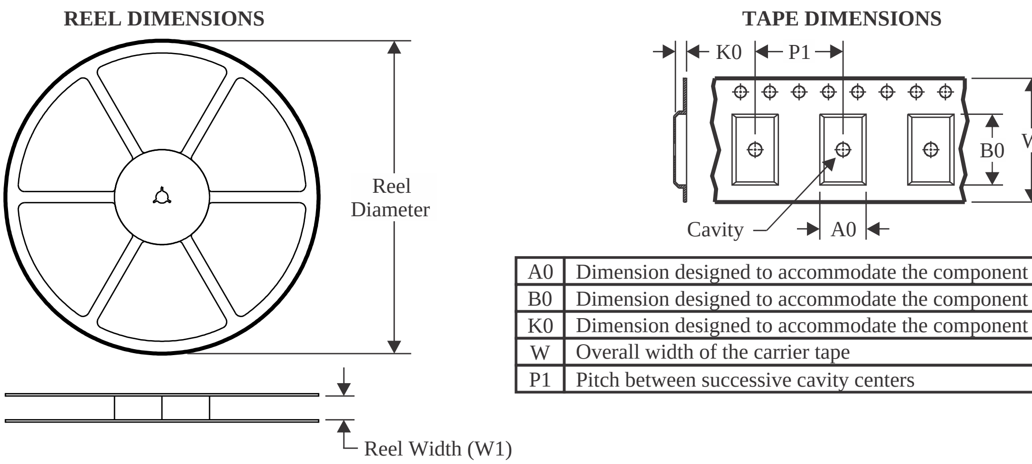
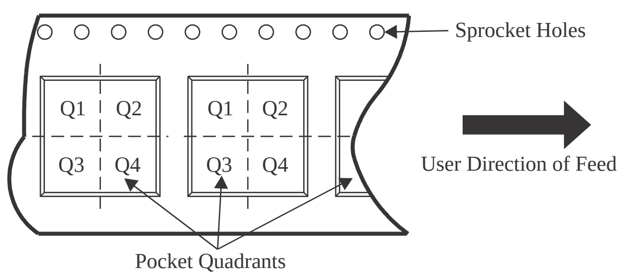
TAPE AND REEL INFORMATION



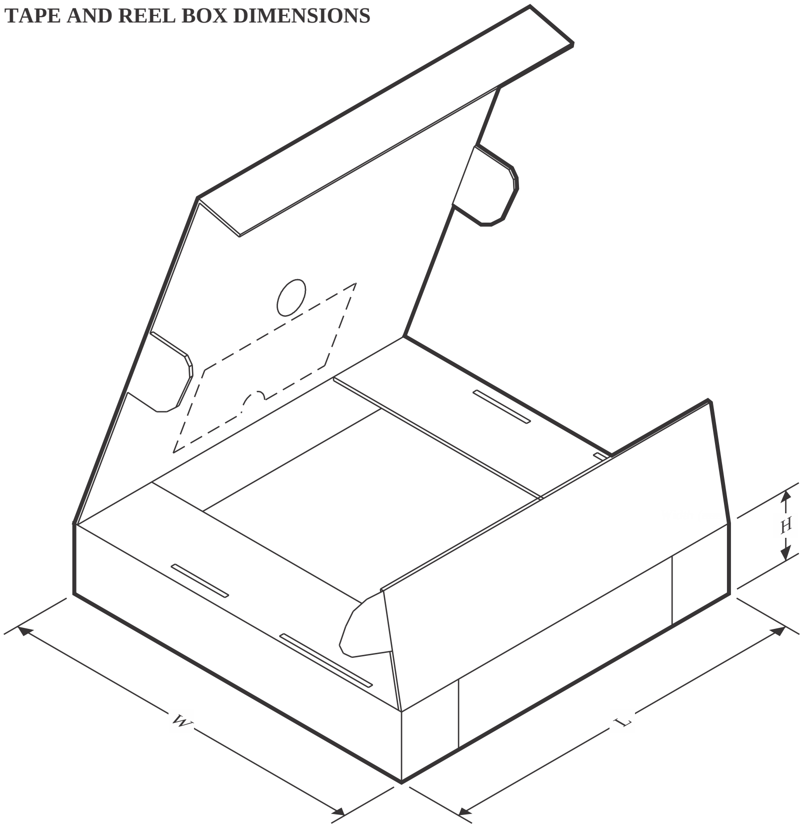
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2017D2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2017D2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2
TPA2017D2RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2017D2RTJT	QFN	RTJ	20	250	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2

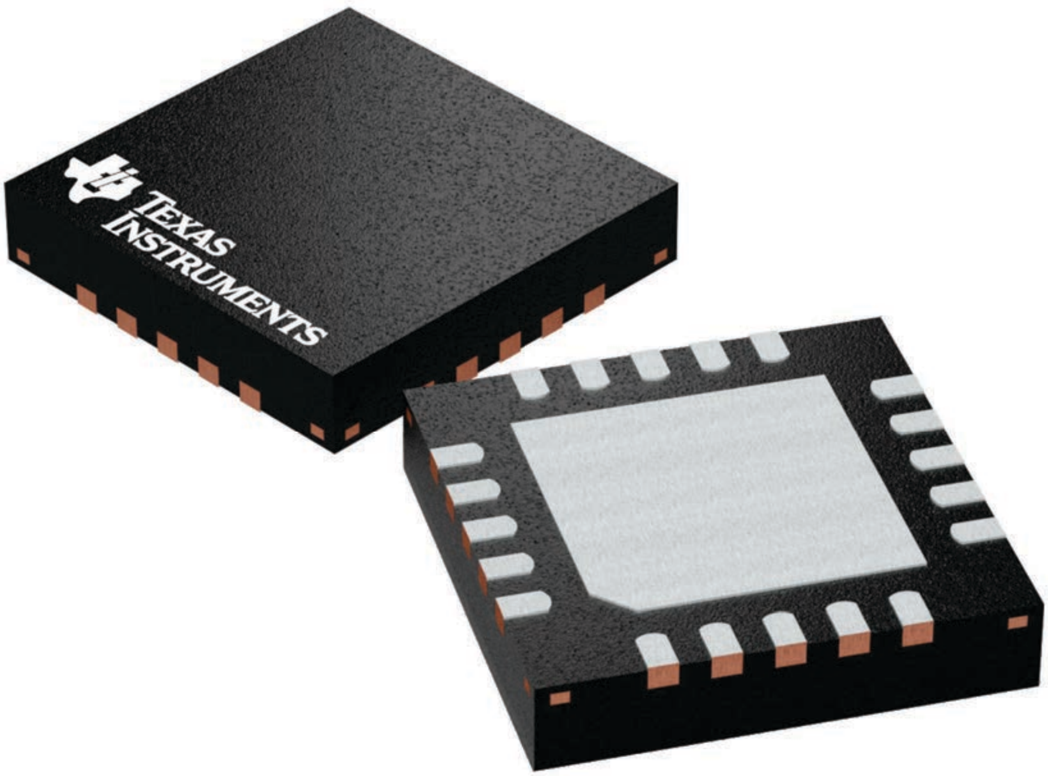
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2017D2RTJR	QFN	RTJ	20	3000	356.0	356.0	35.0
TPA2017D2RTJR	QFN	RTJ	20	3000	370.0	355.0	55.0
TPA2017D2RTJT	QFN	RTJ	20	250	210.0	185.0	35.0
TPA2017D2RTJT	QFN	RTJ	20	250	195.0	200.0	45.0

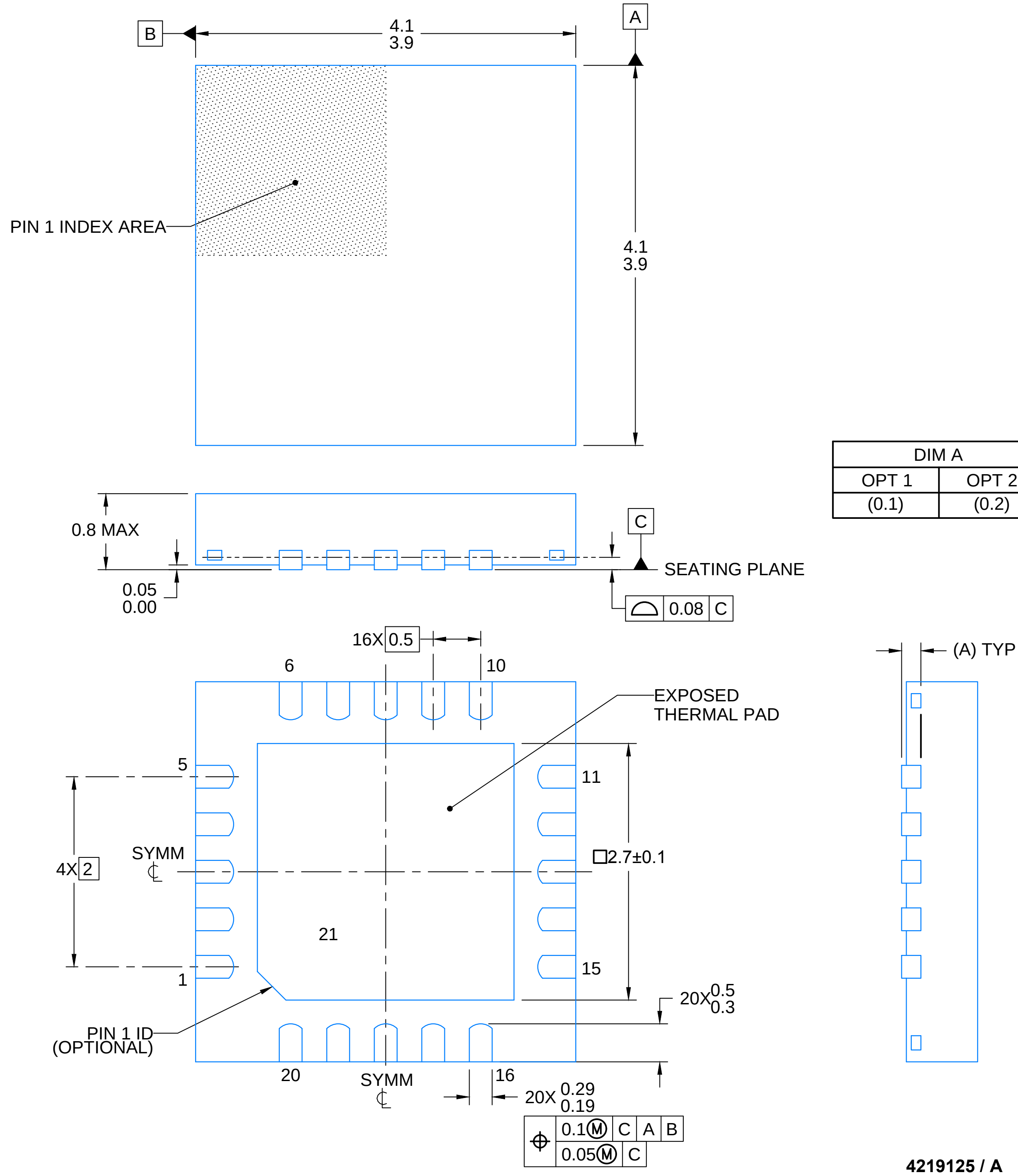
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



DATA BOOK
PACKAGE OUTLINE

LEADFRAME EXAMPLE
4222370

DRAFTSMAN: H. DENG	DATE: 09/12/2016		DIMENSIONS IN MILLIMETERS
DESIGNER: H. DENG	DATE: 09/12/2016	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
CHECKER: V. PAKU & T. LEQUANG	DATE: 09/12/2016		
ENGINEER: T. TANG	DATE: 09/12/2016	ePOD, RTJ0020D / WQFN, 20 PIN, 0.5 MM PITCH	
APPROVED: E. REY & D. CHIN	DATE: 10/06/2016		
RELEASED: WDM	DATE: 10/24/2016		
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016	SCALE 15X, SIZE A, 4219125	REV A, PAGE 1 OF 5

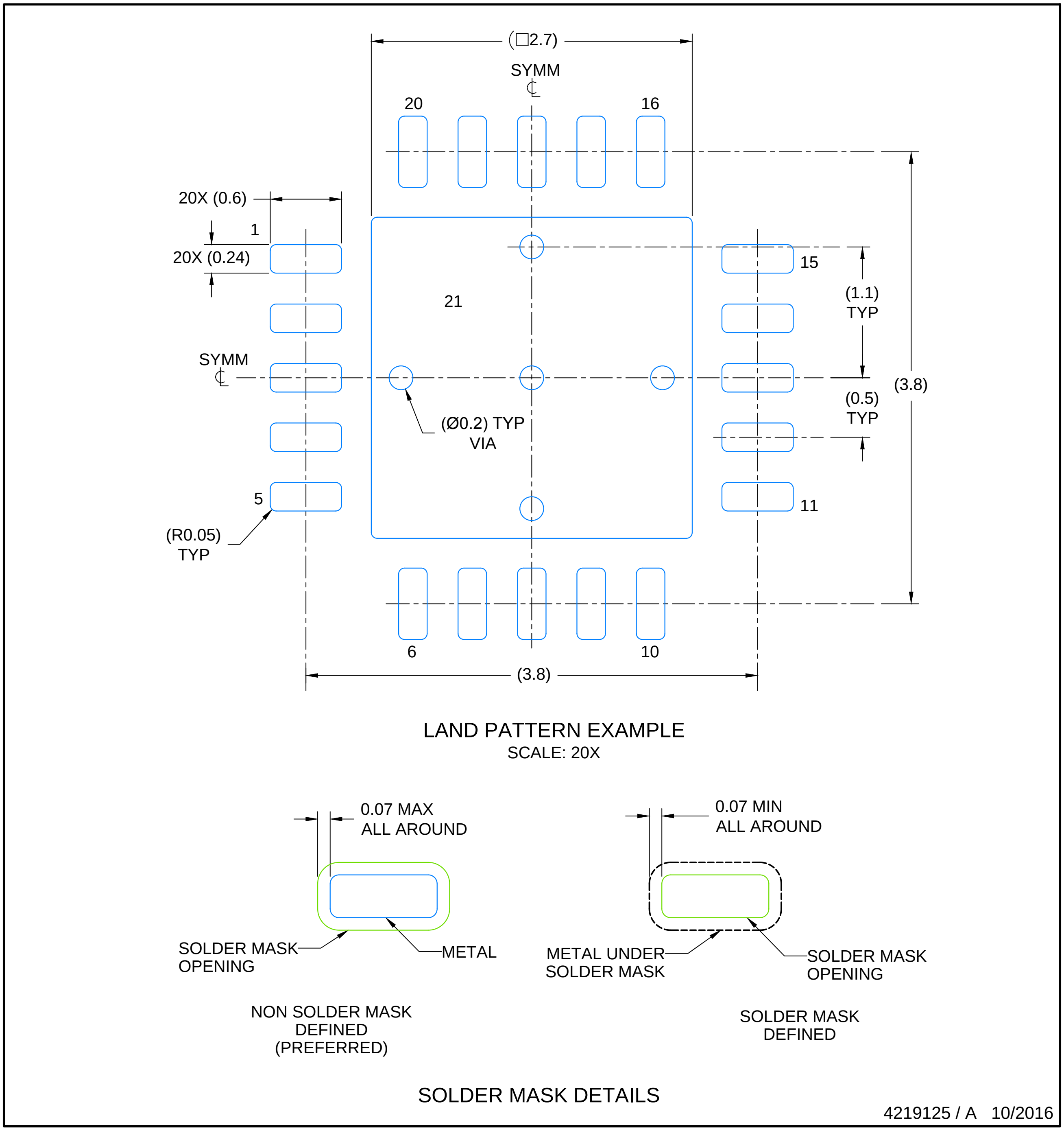


DIM A	
OPT 1	OPT 2
(0.1)	(0.2)

4219125 / A 10/2016

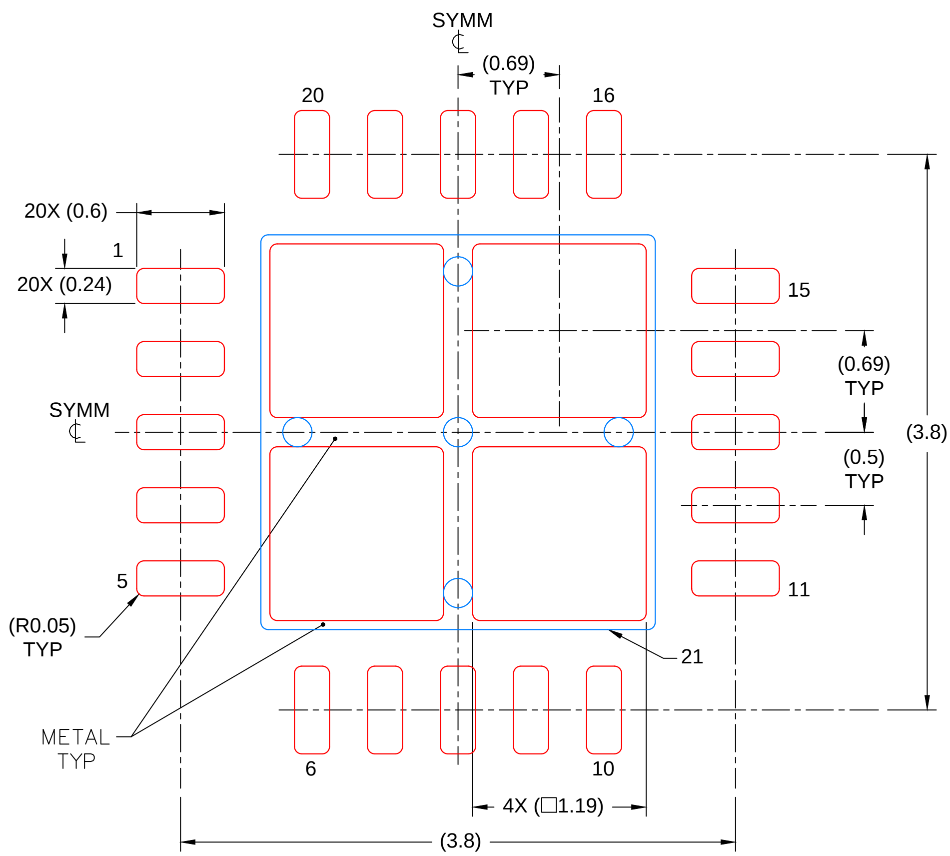
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219125 / A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2160736	10/24/2016	T. TANG / H. DENG

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