Keywords: elastic, store, buffer, T1, E1, rate, conversion

APPLICATION NOTE 3208

Elastic Store Operation

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Abstract: The elastic store inside of Maxim T1, E1, and J1 devices serves as a dual port buffer between the line side and the system side of the device. It allows the two sides to operate in different clock domains or even at different frequencies. The nature of the elastic store makes it difficult to understand how the device reacts under a given set of conditions. This application note presents many different examples and should remove most questions about how the elastic store operates under these varying conditions.

Introduction

The elastic store inside of Maxim T1, E1, and J1 devices serves as a dual port buffer between the line side and the system side of the device. It allows the two sides to operate in different clock domains or even at different frequencies. The nature of the elastic store makes it difficult to understand how the device reacts under a given set of conditions. This application note presents many different examples and should remove most questions about how the elastic store operates under these varying conditions.

Elastic Store Operation

The elastic store is a dual port buffer that has a depth of 512 bits. Since the bit length of a frame varies between T1 and E1, the amount of buffer bits that are used depends on the mode of operation. There are four basic modes of operation:

- T1 Mode: 193-bit frame
- E1 Mode: 256-bit frame
- T1 to E1 Rate Conversion Mode: 193-bit frames on the line (network) side and 256-bit frames on the system (backplane) side
- Interleave Bus Operation Mode: 193-bit or 256-bit frames on the line (network) side and 256-bit frames on the system (backplane) side with a high speed gapped system clock

To clarify the operation of the elastic store, the following series of diagrams was created. Each example was based on the receive elastic store in E1 mode with 256 bit frames. The write pointer, indicated by the white dot, is clocked by RCLK and writes data into the elastic store. The read pointer, indicated by the black dot, is clocked by RSYSCLK and reads data out of the elastic store (if the transmit elastic store were used in the examples, the write pointer would be clocked by TSYSCLK and the read pointer would be clocked by TCLK). **Figure 1** illustrates the condition where the write pointer and read pointer are "ideally" centered at exactly one frame apart.

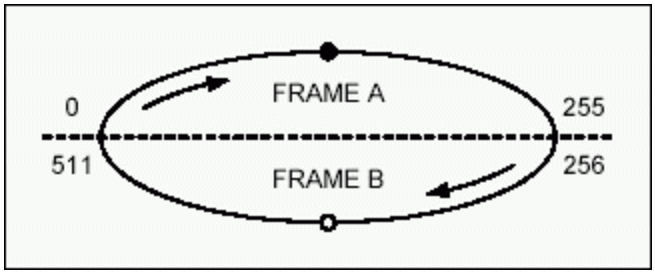

Figure 1. Elastic store read and write pointers are exactly one frame apart.

In **Figure 2**, the read pointer (black dot) is about to enter frame B. When either pointer crosses a frame boundary, the distance between the two pointers is compared in the forward direction. Any distance below a set threshold will cause a frame slip and the pointer that just crossed the frame boundary is moved to the beginning of the next frame. Depending on which pointer slipped, there will either be a repeated or deleted frame. The threshold depends on the mode of operation: 16 bits in E1 mode and 9 bits for all other modes. In the example below, the write pointer (white dot) is almost a frame away thus no slip occurs and the read pointer will continue into frame B.

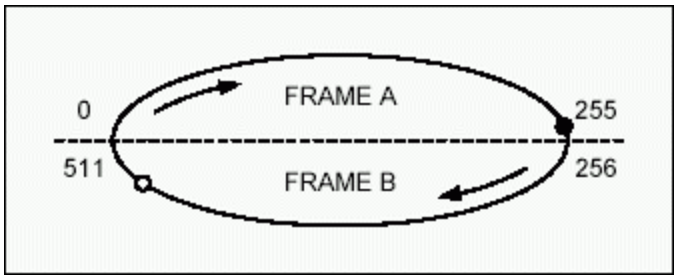

Figure 2. Read and write pointers are far enough apart that no slip occurs after a compare.

In **Figure 3**, the read pointer (black dot) is running faster than the write pointer (white dot) and will eventually catch up. As the read pointer crosses the boundary into frame A, it detects that the write pointer is within 16 bits of the start of frame A. Rather than enter frame A, the read pointer slips and returns to the start of frame B at bit position 256. Because the read pointer slipped, the last frame read from the buffer is repeated and a receive elastic store empty event is reported.

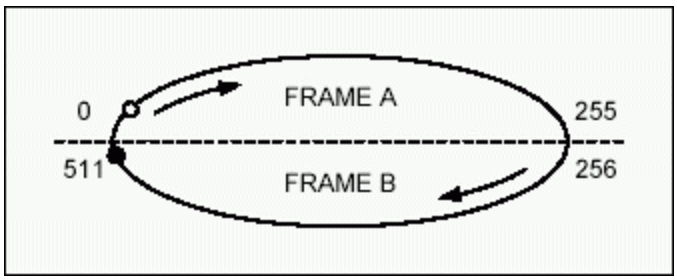

Figure 3. The read pointer is too close to the write pointer during a compare and cause a slip.

The same is true when the write pointer is running faster than the read pointer. If the write pointer detects that the read pointer is within 16 bits of the start of frame B, the write pointer slips and returns to the start of frame A at bit position 0. Since the write pointer slipped, the last frame written to the buffer is deleted and a receive elastic store full event is reported. An example of the write pointer causing the slip is shown in **Figure 4**.

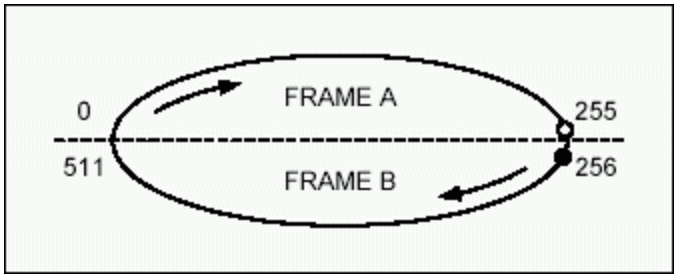

Figure 4. The write pointer is too close to the read pointer during a compare and causes a slip.

In the receive elastic store examples above, both pointers should always move around the buffer at a constant rate. The write pointer is clocked by the receive clock and is constant, based on either the recovered clock or the master clock when in carrier loss. The read pointer is clocked by the receive system clock and should be constant, based on either an external clock or backplane clock. Because of this, the slip contention logic will always be able to detect a slip event. The logic will either repeat or delete a frame of data and the elastic store will recover instantly with only a single frame error.

Additional Information

For more information on the operation of the elastic stores present in T1 or E1 framers and single-chip transceivers, please contact the Telecommunication Applications support team.

Related Parts		
DS21352	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21354	3.3V/5V E1 Single Chip Transceivers (SCT)	
DS21455	Quad T1/E1/J1 Transceivers	Free Samples
DS21458	Quad T1/E1/J1 Transceivers	Free Samples
DS2151Q	T1 Single Chip Transceiver	
DS2152	Enhanced T1 Single Chip Transceiver	
DS2153Q	E1 Single Chip Transceiver	
DS2154	Enhanced E1 Single Chip Transceiver	
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples
DS21552	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21554	3.3V/5V E1 Single Chip Transceivers (SCT)	Free Samples
DS21Q352	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q354	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q55	Quad T1/E1/J1 Transceiver	
DS21Q552	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q554	Quad T1/E1 Transceiver (3.3V, 5.0V)	

DS26401	Octal T1/E1/J1 Framer	Free Samples
DS26528	Octal T1/E1/J1 Transceiver	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

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