NCP3125

4 A Synchronous PWM Switching Converter

The NCP3125 is a flexible synchronous PWM Switching Buck Regulator. The NCP3125 is capable of producing output voltages as low as 0.8 V. The NCP3125 also incorporates voltage mode control. To reduce the number of external components, a number of features are internally set including switching frequency. The NCP3125 is currently available in an SOIC−8 package.

Features

- 4.5 V to 13.2 V Operating Input Voltage Range
- 60 mΩ High−Side, 36 mΩ Low−Side Switches
- Output Voltage Adjustable to 0.8 V
- 4 A Continuous Output Current
- Fixed 350 kHz PWM Operation
- 1.0% Initial Output Accuracy
- 75% Max Duty Ratio
- Over−Load Protection
- Programmable Current Limit
- This is a Pb−Free Device

Typical Application

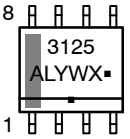
- Set Top Boxes
- DVD Drives and HDD
- LCD Monitors and TVs
- Cable Modems
- Telecom / Networking / Datacom Equipment

ON Semiconductor®

http://onsemi.com

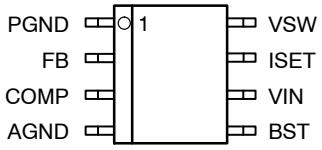
SOIC−8 NB
D SUFFIX
CASE 751

MARKING DIAGRAM



3125	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year/
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

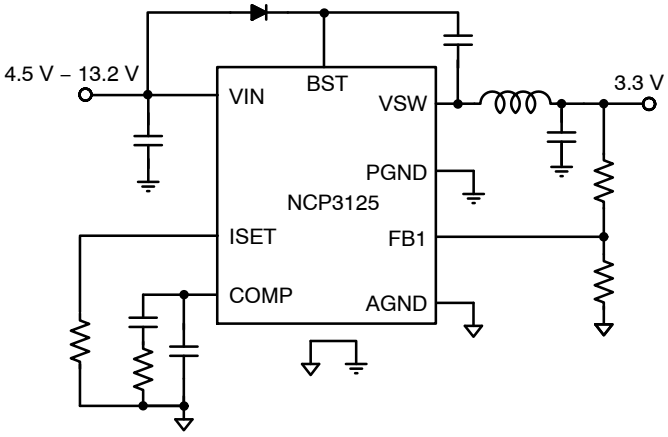


Figure 1. Typical Application Circuit

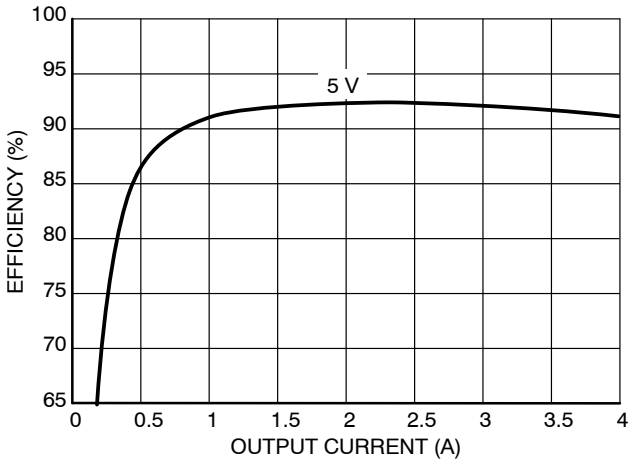


Figure 2. Efficiency (V_{IN} = 12 V) vs. Load Current

CIRCUIT DESCRIPTION

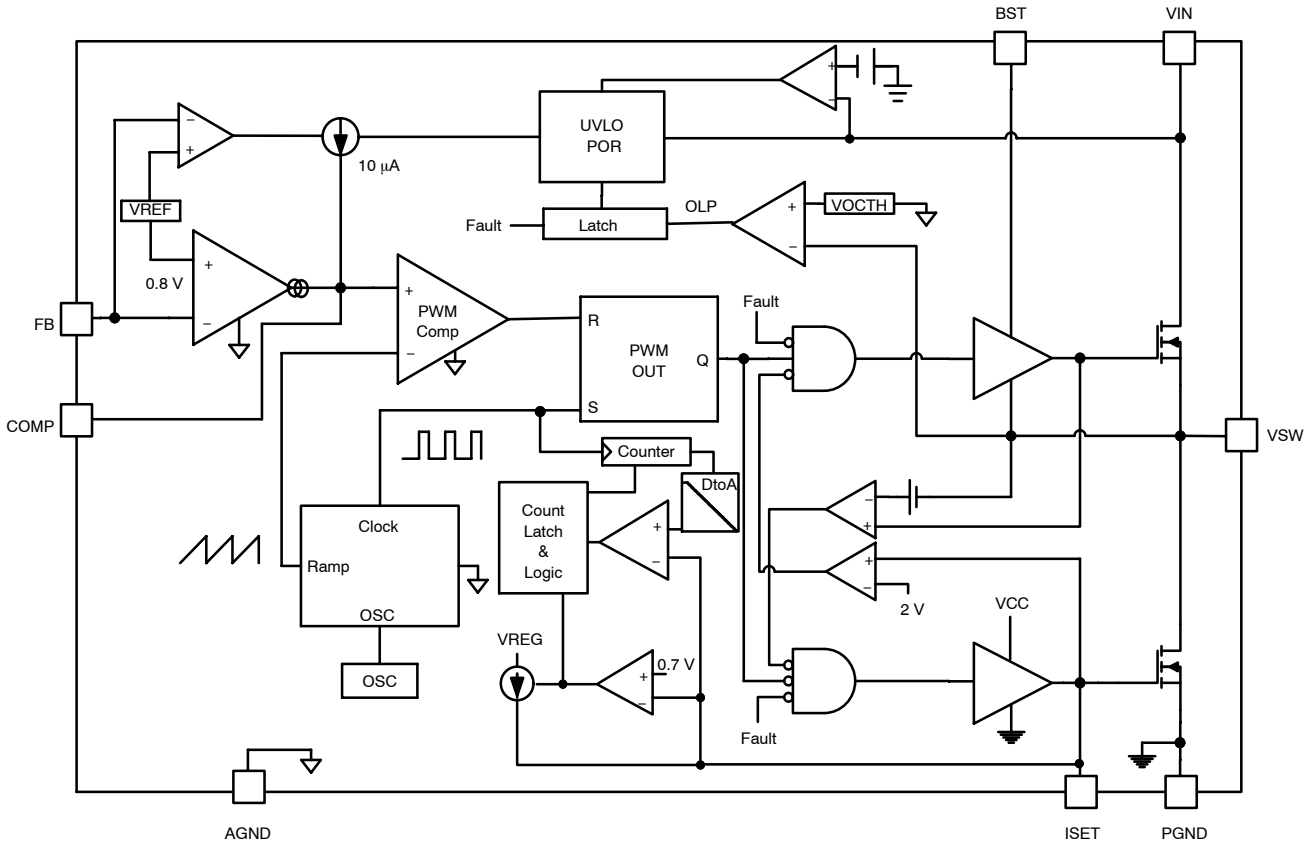


Figure 3. NCP3125 Block Diagram

Table 1. PIN DESCRIPTION

Pin	Pin Name	Description
1	PGND	The PGND pin is the high current ground pin for the low−side MOSFET and the drivers. The pin should be soldered to a large copper area to reduce thermal resistance.
2	FB	Inverting input to the Operational Transconductance Amplifier (OTA). The FB pin in conjunction with the external compensation, serves to stabilize and achieve the desired output voltage with voltage mode control.
3	COMP	COMP pin is used to compensate the OTA which stabilizes the operation of the converter stage. Place compensation components as close to the converter as possible.
4	AGND	The AGND pin serves as small−signal ground. All small−signal ground paths should connect to the AGND pin at a single point, avoiding any high current ground returns.
5	BST	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BST pin). Connect a capacitor (CBST) between this pin and the VSW pin. Typical values for CBST range from 1 nF to 10 nF. Ensure that CBST is placed near the IC.
6	VIN	The VIN pin powers the internal control circuitry and is monitored by an undervoltage comparator. The VIN pin is also connected to the internal power NMOSFET switches. The VIN pin has high dI/dt edges and must be decoupled to PGND pin close to the pin of the device.
7	ISET	Current set pin and bottom gate MOSFET driver. Place a resistor to ground to set the current limit of the converter.
8	VSW	The VSW pin is the connection of the drain and source of the internal N−MOSFETs. The VSW pin swings from V_{IN} when the high side switch is on to small negative voltages when the low side switch is on with high dV/dt transitions.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Main Supply Voltage Input	V_{IN}	−0.3	15	V
Bootstrap Supply Voltage vs GND	VBST	−0.3	15	V
Bootstrap Supply Voltage vs Ground (spikes ≤ 50 ns)	VBST spike	−5.0	35	V
Bootstrap Pin Voltage vs V_{SW}	VBST−V_{SW}	−0.3	15	V
High Side Switch Max DC Current	IV_{SW}	0	4	A
V_{SW} Pin Voltage	V_{SW}	−0.3	30	V
Switching Node Voltage Excursion (200 μA)	V_{SWLIM}	−2.0	35	V
Switch Pin voltage (spikes < 50 ns)	V_{SWtr}	−5.0	40	V
FB Pin Voltage	VFB	−0.3	5.5 < V_{CC}	V
COMP/DISABLE	VCOMP/DIS	−0.3	5.5 < V_{CC}	V
Low Side Driver Pin Voltage	VISET	−0.3	15 < V_{CC}	V
Low Side Driver Pin Voltage (spikes ≤ 200 ns)	VISET Spike	−2	15 < V_{CC}	V

Rating	Symbol	Rating	Unit
Thermal Resistance, Junction−to−Ambient (Note 2) (Note 3)	$R_{\theta JA}$	110 183	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	170	°C/W
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Operating Temperature	T_J	−40 to 125	°C
Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free	RF	260 peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The maximum package power dissipation limit must not be exceeded.
2. The value of θJA is measured with the device mounted on 1 in^2 FR−4 board with 1 oz. copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.
3. The value of θJA is measured with the device mounted on minimum footprint, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.
4. 60−180 seconds minimum above 237°C.

Table 3. ELECTRICAL CHARACTERISTICS (−40°C < T_J < 125°C; V_{IN} = 12 V, BST−VSW = 12 V, BST = 12 V, V_{SW} = 24 V, for min/max values unless otherwise noted.)

Characteristic	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN} − GND	4.5		13.2	V
Boost Voltage Range	VBST − GND	4.5		26.5	V
SUPPLY CURRENT					
Quiescent Supply Current	VFB = 1.0 V, No Switching, V_{IN} = 13.2 V	1.0	–	10.0	mA
Shutdown Supply Current	VFB = 1.0 V, COMP = 0 V, V_{IN} = 13.2 V	–	4.0	–	mA
Boost Quiescent Current	VFB = 1.0 V, No Switching, V_{IN} = 13.2 V	0.1	–	1.0	mA
UNDER VOLTAGE LOCKOUT					
V_{IN} UVLO Threshold	V_{IN} Rising Edge	3.8	–	4.3	V
V_{IN} UVLO Hysteresis	–	–	430	–	mV
SWITCHING REGULATOR					
VFB Feedback Voltage, Control Loop in Regulation	T_J = 0 to 25°C, 4.5 V < V_{CC} < 13.2 V −40°C ≤ T_J ≤ 125°C, 4.5 ≤ V_{CC} ≤ 13.2 V	792 784	800 800	808 816	mV
Oscillator Frequency	T_J = 0 to 25°C, 4.5 V < V_{CC} < 13.2 V −40°C ≤ T_J ≤ 125°C, 4.5 ≤ V_{CC} ≤ 13.2 V	300 290	350 350	400 410	kHz
Ramp−Amplitude Voltage		0.8	1.1	1.4	V
Minimum Duty Ratio		–	5.5	–	%
Maximum Duty Ratio		70	75	80	%
PWM COMPENSATION					
Transconductance		3.0	–	5	mS
Open Loop DC Gain	C_O = 1 nF	55	70	–	dB
Output Source Current Output Sink Current	V_{FB} < 0.8 V V_{FB} > 0.8 V	60 60	125 125	200 200	μA
Input Bias Current		–	0.160	1.0	μA
ENABLE					
Enable Threshold		0.3	0.4	0.5	V
SOFT−START					
Delay to Soft−Start		3	–	15	ms
SS Source Current	VFB < 0.8 V	–	10.5	–	μA
Switch Over Threshold	VFB = 0.8 V	–	100	–	% of Vref
OVER−CURRENT PROTECTION					
OCSET Current Source	Sourced from ISET pin, before SS	–	10	–	μA
OC Switch−Over Threshold		–	700	–	mV
Fixed OC Threshold		–	375		mV
PWM OUTPUT STAGE					
High−Side Switch On−Resistance	V_{IN} = 12 V (Note 5) V_{IN} = 5 V (Note 5)		60 80	75 100	mΩ
Low−Side Switch On−Resistance	V_{IN} = 12 V (Note 5) V_{IN} = 5 V (Note 5)		36 45	40 50	mΩ

5. Guaranteed by design.

TYPICAL CHARACTERISTICS

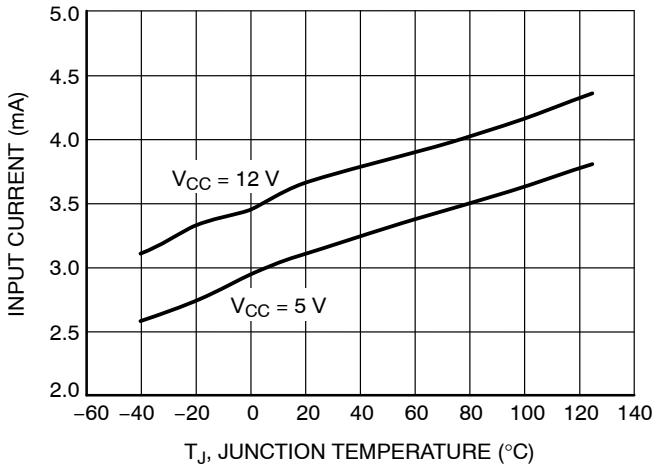


Figure 4. I_{CC} vs. Temperature

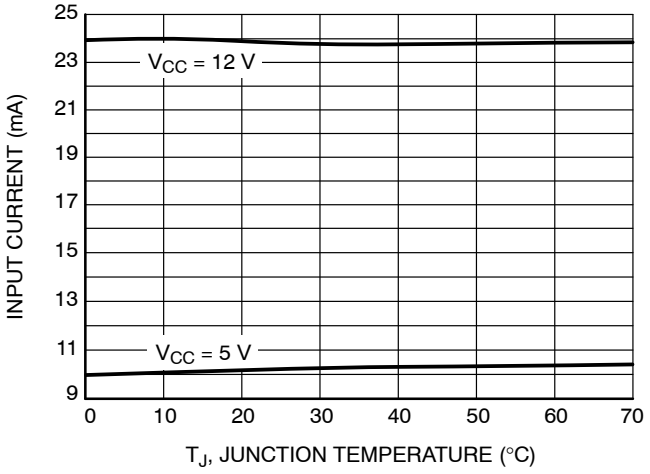


Figure 5. Input Current Switching vs. Temperature

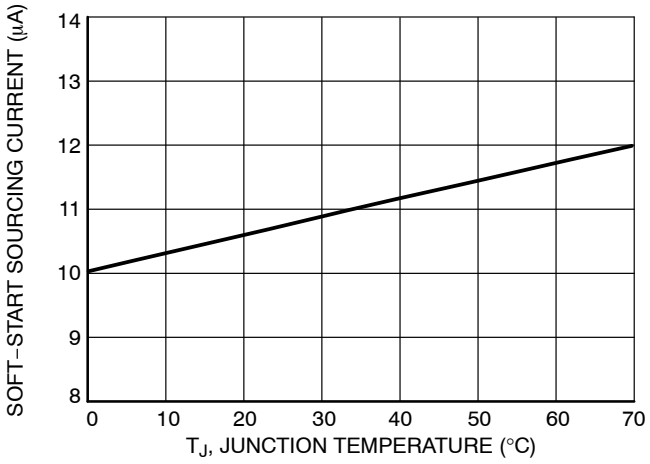


Figure 6. Soft−Start Sourcing Current vs. Temperature

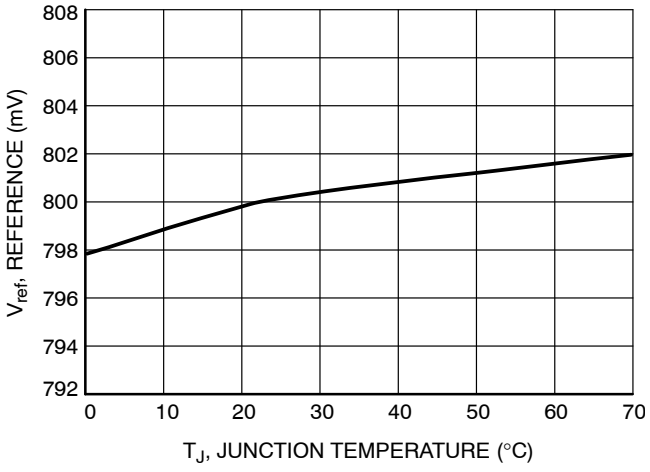


Figure 7. Reference Voltage (V_{ref}) vs. Temperature

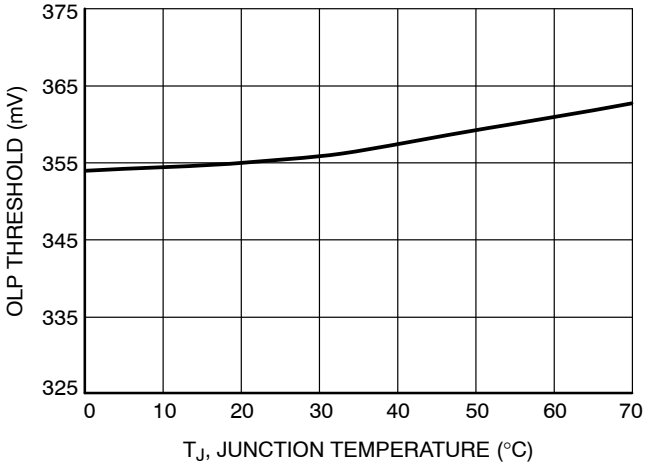


Figure 8. OLP Threshold vs. Temperature

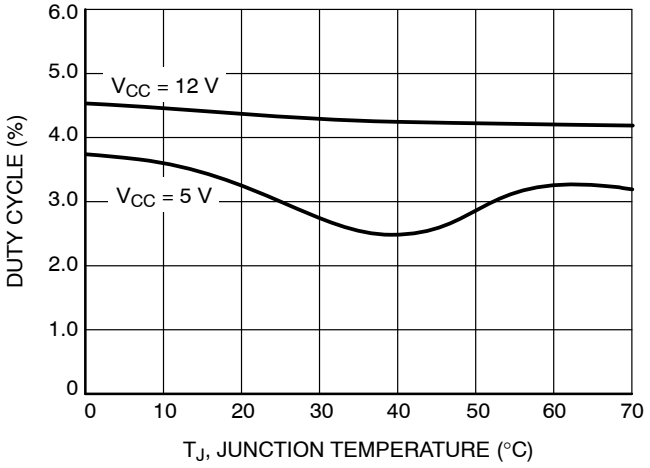


Figure 9. Minimum Active Duty Cycle vs. Temperature

TYPICAL CHARACTERISTICS

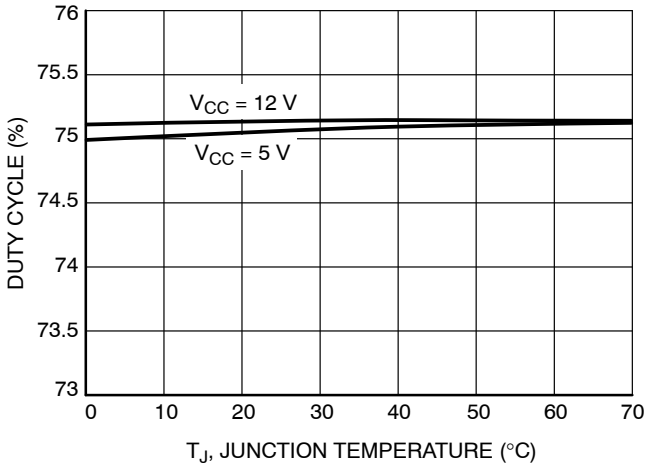


Figure 10. Duty Cycle Maximum vs. Temperature

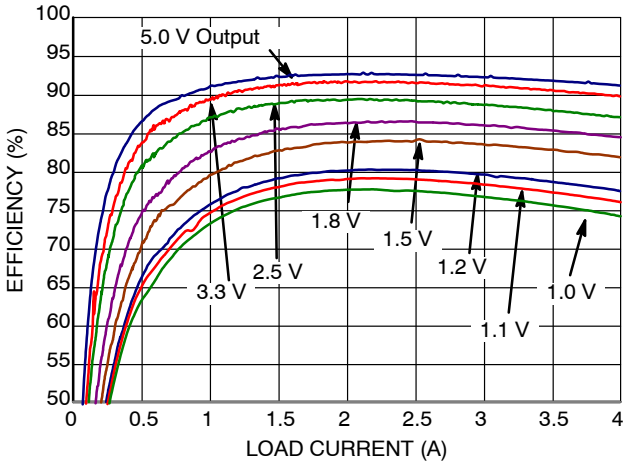


Figure 11. Efficiency (V_{IN} = 12 V) vs. Load Current

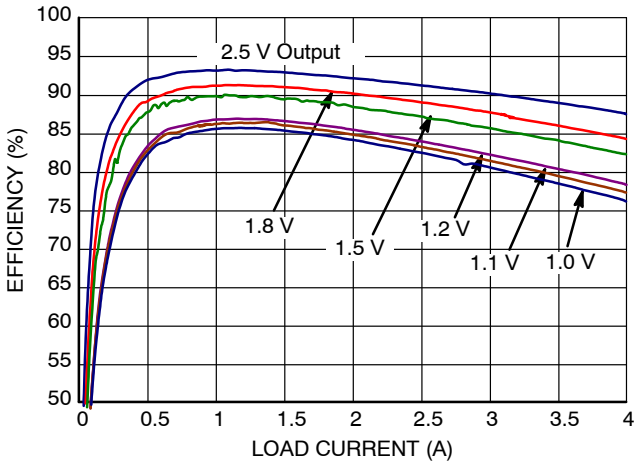


Figure 12. Efficiency (V_{IN} = 5 V) vs. Load Current

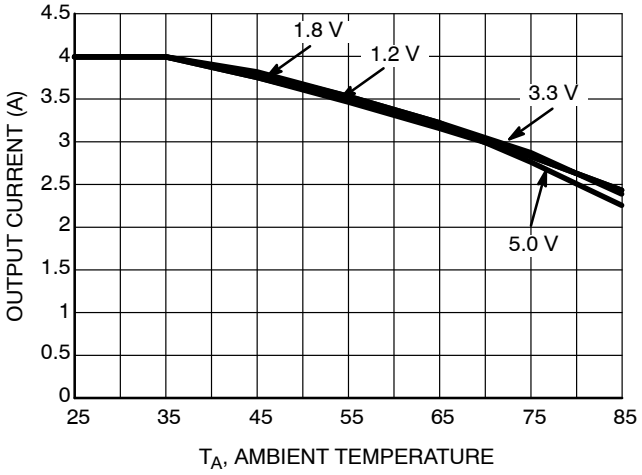


Figure 13. Derating Curve 5 V/6 V Input

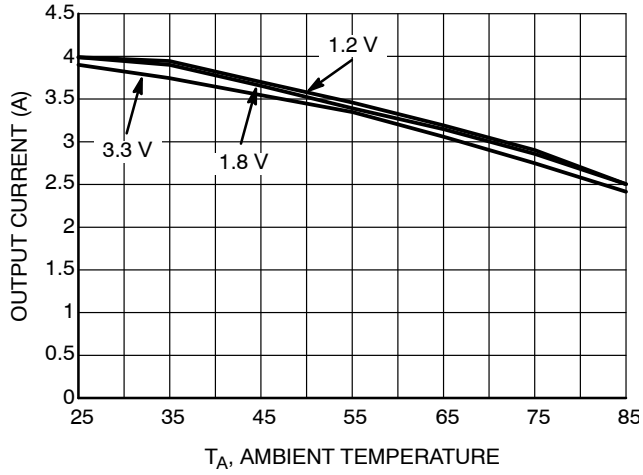


Figure 14. Derating Curve 12 V Input

General

The NCP3125 is a PWM synchronous buck regulator intended to supply up to a 4 A load for DC−DC conversion from 5 V and 12 V buses. The NCP3125 is a regulator that has integrated high−side and low−side NMOSFETs switches. The output voltage of the converter can be precisely regulated down to 800 mV ±1.0% when the VFB pin is tied to V_{OUT}. The switching frequency is internally set to 350 kHz. A high gain operational transconductance amplifier (OTA) is used for voltage mode control of the power stage.

Duty Ratio and Maximum Pulse Width Limits

In steady state DC operation, the duty ratio will stabilize at an operating point defined by the ratio of the input to the output voltage. The device can achieve a 75% duty ratio. The NCP3125 has a preset off−time of approximately 150 ns, which ensures that the bootstrap supply is charged every switching cycle. The preset off time does not interfere with the conversion of 12 V to 0.8 V.

Input Voltage Range (V_{IN} and BST)

The input voltage range for both V_{IN} and BST is 4.5 V to 13.2 V with respect to GND and V_{SW}. Although BST is rated at 13.2 V with respect to V_{SW}, it can also tolerate 26.5 V with respect to GND.

External Enable/Disable

Once the input voltage has exceeded the boost and UVLO threshold at 3 V and V_{IN} threshold at 4 V, the COMP pin starts to rise. The V_{SW} node is tri−stated until the COMP voltage exceeds 0.9 V. Once the 0.9 V threshold is exceeded, the part starts to switch and the part is considered enabled. When the COMP pin voltage is pulled below the 400 mV threshold, it disables the PWM logic, the top MOSFET is driven off, and the bottom MOSFET is driven on. In the disabled mode, the OTA output source current is reduced to 10 μA.

When disabling the NCP3125 using the COMP / Disable pin, an open collector or open drain drive should be used as shown in Figure 15:

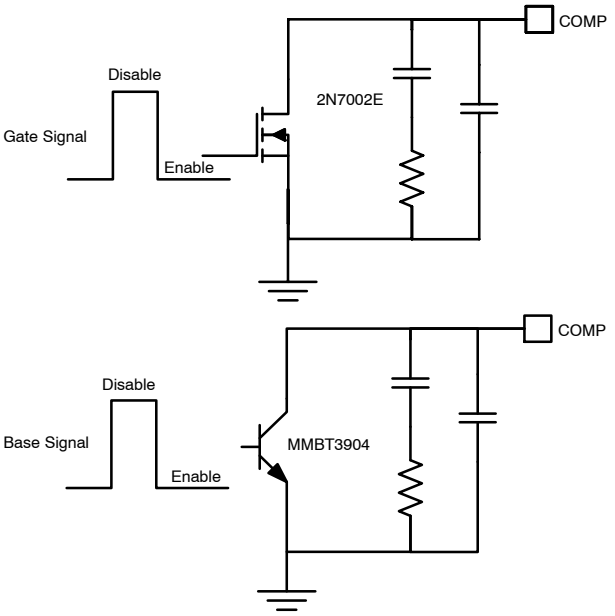


Figure 15. Recommended Disable Circuits

Power Sequencing

Power sequencing can be achieved with NCP3125 using two general purpose bipolar junction transistors or MOSFETs. An example of the power sequencing circuit using the external components is shown in Figure 16.

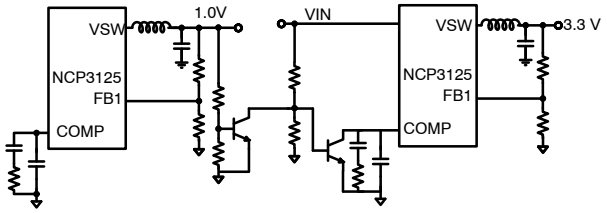


Figure 16. Power Sequencing

Input Voltage Shutdown Behavior

Input voltage shutdown occurs when the IC stops switching because the input supply reaches UVLO threshold. Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when VCC is too low to support the internal rails and power the converter. The UVLO is set to permit operation when converting from an input voltage of 5 V. If the UVLO is tripped, switching stops, the internal SS is discharged, and all MOSFET gates are driven low. The V_{SW} node enters a high impedance state and the output capacitors discharge through the load with no ringing on the output voltage.

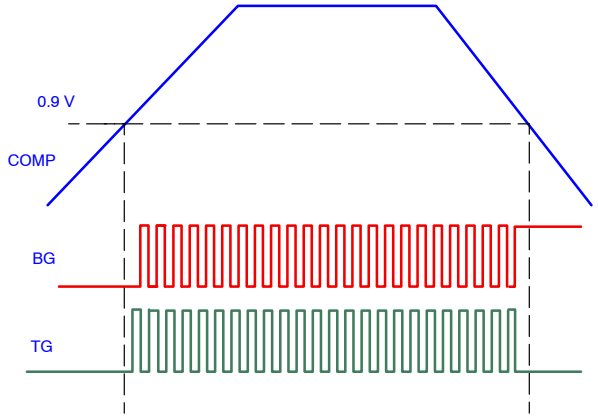


Figure 17. Enable/Disable Driver State Diagram

External Soft−Start

The NCP3125 features an external soft−start function, which reduces inrush current and overshoot of the output voltage. Soft−start is achieved by using the internal current source of 10.5 μA (typ), which charges the external integrator capacitor of the OTA. Figure 18 is a typical soft−start sequence. The sequence begins once V_{IN} and V_{BST} surpass their UVLO thresholds and OCP programming is complete. The current sourced out of the COMP pin continually increases the voltage until regulation is reached. Once the voltage reaches 400 mV logic is enabled. When the voltage exceeds 900 mV, switching begins. Current is sourced out of the COMP pin, placing the regulator into open loop operation until 800 mV is sensed at the FB pin. Once 800 mV is sensed at the FB pin, open loop operation ends and closed loop operation begins. In closed loop operation, the OTA is capable of sourcing and sinking 120 μA.

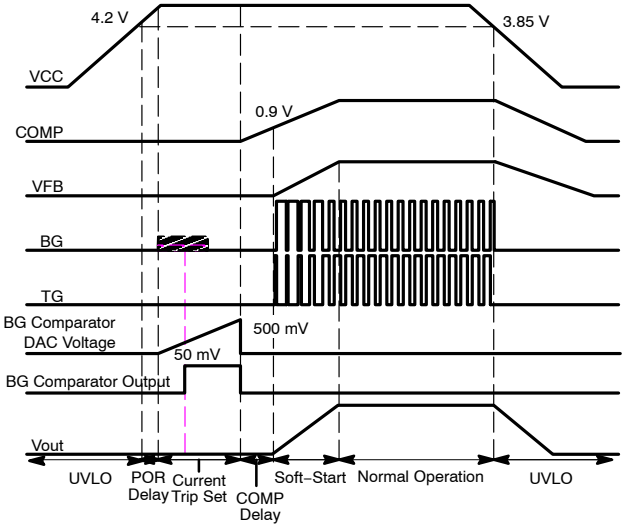


Figure 18. Soft−Start Sequence

Overcurrent Threshold Setting

NCP3125 overcurrent threshold can be set from 50 mV to 550 mV, by adding a resistor (R_{SET}) between ISET and GND. During a short period of time following V_{IN} rising over UVLO threshold, an internal 10 μA current (I_{OCSET}) is sourced from the ISET pin, creating a voltage drop across R_{SET}. The voltage drop is compared against a stepped internal voltage ramp. Once the internal stepped voltage reaches the R_{SET} voltage, the value is stored internally until power is cycled. The overall time length for the OC setting procedure is approximately 9 ms. Connecting an R_{SET} resistor between ISET and GND, the programmed threshold will be:

$$I_{OCth} = \frac{I_{OCSET} * R_{SET}}{R_{DS(on)}} \rightarrow 4.2\ A = \frac{10\ \mu A * 21\ k\Omega}{50\ m\Omega} \quad \text{(eq. 1)}$$

I_{OCSET} = Sourced current
I_{OCth} = Current trip threshold
$R_{DS(on)}$ = On resistance of the low side MOSFET
R_{SET} = Current set resistor

The R_{SET} values range from 5 kΩ to 55 kΩ. If R_{SET} is not connected, the device switches the OCP threshold to a fixed 375 mV value. An internal safety clamp on ISET is triggered as soon as ISET voltage reaches 700 mV, enabling the 375 mV fixed threshold and ending the OCP setting period. The current trip threshold tolerance is ±25 mV. The accuracy is best at the highest set point (550 mV). The accuracy will decrease as the set point decreases. MOSFET tolerances with temperature and input voltage will vary the over current set threshold operating point. A graph of the typical current limit set thresholds at 4.5 V and 12 V is shown in Figure .

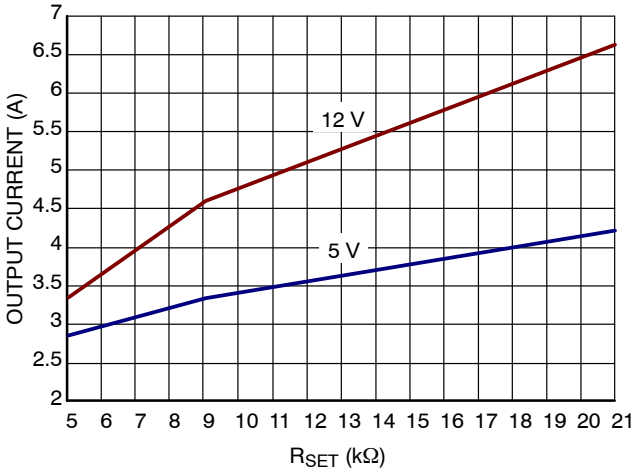


Figure 19. R_{SET} Value for Output Current

Current Limit Protection

In case of an overload, the low−side (LS) FET will conduct large currents. The regulator will latch off, protecting the load and MOSFETs from excessive heat and damage. Low−side $R_{DS(on)}$ sense is implemented at the end of each LS−FET turn−on duration to sense the current. While the low side MOSFET is on, the V_{SW} voltage is compared to the user set internally generated OCP trip voltage. If the V_{SW} voltage is lower than OCP trip voltage, an overcurrent condition occurs and a counter counts consecutive current trips. If the counter reaches 7, the PWM logic and both HS−FET and LS−FET are turned off. The regulator has to go through a Power On Reset (POR) cycle to reset the OCP fault as shown in Figure 20.

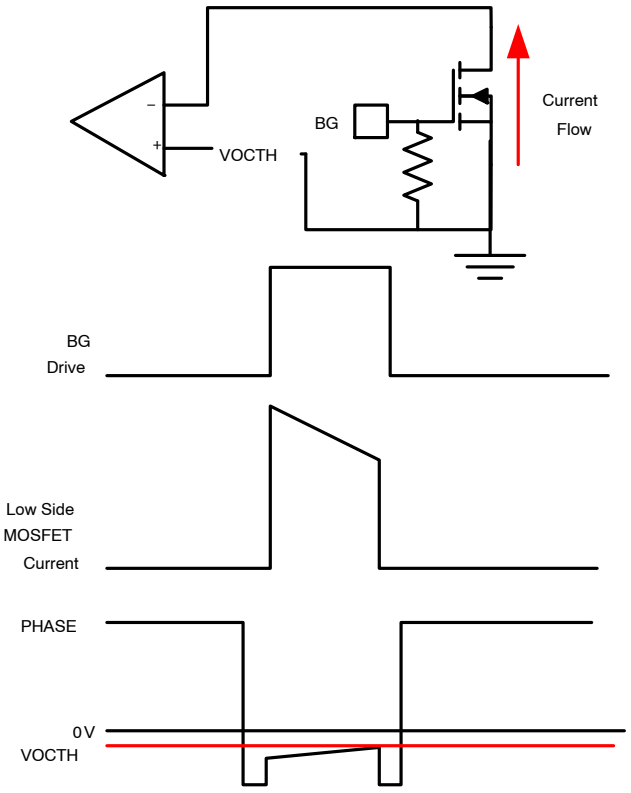


Figure 20. Current Limit Trip

APPLICATION SECTION

Design Procedure

When starting the design of a buck regulator, it is important to collect as much information as possible about the behavior of the input and output before starting the design.

ON Semiconductor has a Microsoft Excel® based design tool available online under the design tools section of the NCP3125 product page. The tool allows you to capture your design point and optimize the performance of your regulator based on your design criteria.

Table 4. DESIGN PARAMETERS

Design Parameter		Example Value
Input voltage	(V_{IN})	10.8 V to 13.2 V
Output voltage	(V_{OUT})	3.3 V
Input ripple voltage	($V_{INRIPPLE}$)	300 mV
Output ripple voltage	($V_{OUTRIPPLE}$)	60 mV
Output current rating	(I_{OUT})	4 A
Operating frequency	(F_{SW})	350 kHz

The buck converter produces input voltage V_{IN} pulses that are LC filtered to produce a lower DC output voltage V_{OUT}. The output voltage can be changed by modifying the on time relative to the switching period T or switching frequency. The ratio of high side switch on time to the switching period is called duty ratio D. Duty ratio can also be calculated using V_{OUT}, V_{IN}, the Low Side Switch Voltage Drop V_{LSD}, and the High Side Switch Voltage Drop V_{HSD}.

$$F_{SW} = \frac{1}{T} \quad \text{(eq. 2)}$$

$$D = \frac{T_{ON}}{T} \text{ and } (1 - D) = \frac{T_{OFF}}{T} \quad \text{(eq. 3)}$$

$$D = \frac{V_{OUT} + V_{LSD}}{V_{IN} - V_{HSD} + V_{LSD}} \approx D = \frac{V_{OUT}}{V_{IN}} \rightarrow 27.5\% = \frac{3.3\ V}{12\ V} \quad \text{(eq. 4)}$$

D = Duty cycle
F_{SW} = Switching frequency
T = Switching period
T_{OFF} = High side switch off time
T_{ON} = High side switch on time
V_{HSD} = High side switch voltage drop
V_{IN} = Input voltage
V_{LSD} = Low side switch voltage drop
V_{OUT} = Output voltage

Inductor Selection

When selecting an inductor, the designer can employ a rule of thumb for the design where the percentage of ripple current in the inductor should be between 10% and 40%. When using ceramic output capacitors, the ripple current can be greater because the ESR of the output capacitor is smaller, thus a user might select a higher ripple current. However,

when using electrolytic capacitors, a lower ripple current will result in lower output ripple due to the higher ESR of electrolytic capacitors. The ratio of ripple current to maximum output current is given in Equation 5.

$$ra = \frac{\Delta I}{Iout} \quad \text{(eq. 5)}$$

ΔI = Ripple current
I_{OUT} = Output current
ra = Ripple current ratio

Using the ripple current rule of thumb, the user can establish acceptable values of inductance for a design using Equation 6.

$$L_{OUT} = \frac{V_{OUT}}{I_{OUT} \cdot ra \cdot F_{SW}} \cdot (1 - D) \rightarrow \quad \text{(eq. 6)}$$
$$5.7\ \mu H = \frac{3.3\ V}{4\ A \cdot 30\% \cdot 350\ kHz} \cdot (1 - 27.5\%)$$

D = Duty ratio
F_{SW} = Switching frequency
I_{OUT} = Output current
L_{OUT} = Output inductance
ra = Ripple current ratio

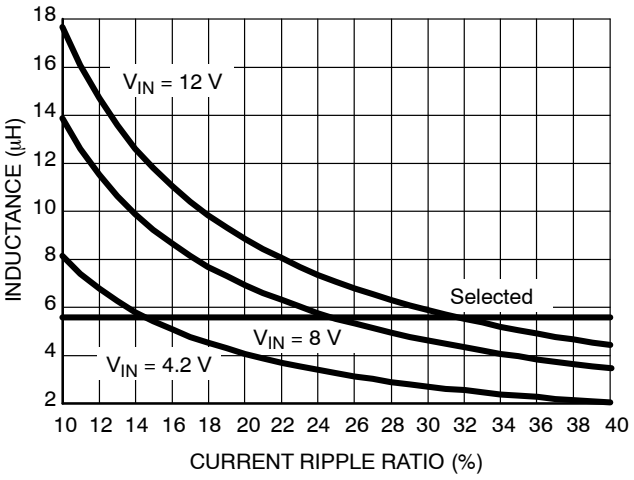


Figure 21. Inductance vs. Current Ripple Ratio

When selecting an inductor, the designer must not exceed the current rating of the part. To keep within the bounds of the part's maximum rating, a calculation of the RMS and peak inductor current is required.

$$I_{RMS} = I_{OUT} \cdot \sqrt{1 + \frac{ra^2}{12}} \rightarrow \quad \text{(eq. 7)}$$
$$4.01\ A = 4\ A * \sqrt{1 + \frac{30\%^2}{12}}$$

I_{OUT} = Output current
I_{RMS} = Inductor RMS current
ra = Ripple current ratio

$$I_{PK} = I_{OUT} \cdot \left(1 + \frac{ra}{2}\right) \rightarrow 4.6\ A = 4\ A \cdot \left(1 + \frac{30\%}{2}\right) \quad \text{(eq. 8)}$$

I_{OUT} = Output current
I_{PK} = Inductor peak current
ra = Ripple current ratio

A standard inductor should be found so the inductor will be rounded to 5.6 μH. The inductor should also support an RMS current of 4.01 A and a peak current of 4.6 A.

The final selection of an output inductor has both mechanical and electrical considerations. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space constrained applications. From an electrical perspective, the maximum current slew rate through the output inductor for a buck regulator is given by Equation 9.

$$SlewRate_{LOUT} = \frac{V_{IN} - V_{OUT}}{L_{OUT}} \rightarrow 1.53 \frac{A}{\mu s} = \frac{12\ V - 3.3\ V}{5.6\ \mu H} \quad \text{(eq. 9)}$$

L_{OUT} = Output inductance
V_{IN} = Input voltage
V_{OUT} = Maximum output voltage

Equation 9 implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. Reduced inductance to increase slew rates results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak−to−peak ripple current for NCP3125 is given by the following equation:

$$Ipp = \frac{V_{OUT} \times (1 - D)}{L_{OUT} \cdot F_{SW}} \rightarrow \quad \text{(eq. 10)}$$
$$1.2\ A = \frac{3.3\ V\ \times (1 - 27.5\%)}{5.6\ \mu H \cdot 350\ kHz}$$

D = Duty ratio
F_{SW} = Switching frequency
Ipp = Peak−to−peak current of the inductor
L_{OUT} = Output inductance
V_{OUT} = Output voltage

From Equation 10 it is clear that the ripple current increases as L_{OUT} decreases, emphasizing the trade−off between dynamic response and ripple current.

The power dissipation of an inductor falls into two categories: copper and core losses. The copper losses can be further categorized into DC losses and AC losses. A good first order approximation of the inductor losses can be made using the DC resistance as shown below:

$$LP_{\_DC} = I_{RMS}{}^2 \cdot DCR \rightarrow 281\ mW = 4.01^2 \cdot 17.5\ m\Omega \quad \text{(eq. 11)}$$

I_{RMS} = Inductor RMS current
DCR = Inductor DC resistance
LP_{CU_DC} = Inductor DC power dissipation

The core losses and AC copper losses will depend on the geometry of the selected core, core material, and wire used. Most vendors will provide the appropriate information to make accurate calculations of the power dissipation at which point the total inductor losses can be captured by the equation below:

$$LP_{tot} = LP_{CU\_DC} + LP_{CU\_AC} + LP_{Core} \rightarrow 303\ mW = 281\ mW + 1\ mW + 21\ mW \quad \text{(eq. 12)}$$

LP_{CU_DC} = Inductor DC power dissipation
LP_{CU_AC} = Inductor AC power dissipation
LP_{Core} = Inductor core power dissipation

Output Capacitor Selection

The important factors to consider when selecting an output capacitor are DC voltage rating, ripple current rating, output ripple voltage requirements, and transient response requirements.

The output capacitor must be rated to handle the ripple current at full load with proper derating. The RMS ratings given in datasheets are generally for lower switching frequency than used in switch mode power supplies, but a multiplier is usually given for higher frequency operation. The RMS current for the output capacitor can be calculated below:

$$Co_{RMS} = I_{OUT} \cdot \frac{ra}{\sqrt{12}} \rightarrow 0.346\ A = 4\ A \frac{30\%}{\sqrt{12}} \quad \text{(eq. 13)}$$

Co_{RMS} = Output capacitor RMS current
I_{OUT} = Output current
ra = Ripple current ratio

The maximum allowable output voltage ripple is a combination of the ripple current selected, the output capacitance selected, the Equivalent Series Inductance (ESL), and Equivalent Series Resistance (ESR).

The main component of the ripple voltage is usually due to the ESR of the output capacitor and the capacitance selected, which can be calculated as shown in Equation 14:

$$V_{ESR\_C} = I_{OUT} * ra * \left(Co_{ESR} + \frac{1}{8 * F_{SW} * C_{OUT}} \right) \rightarrow \quad \text{(eq. 14)}$$

$$60.91\ mV = 4 * 30\% * \left(50\ m\Omega + \frac{1}{8 * 350\ kHz * 470\ \mu F} \right)$$

Co_{ESR} = Output capacitor ESR
C_{OUT} = Output capacitance
F_{SW} = Switching frequency
I_{OUT} = Output current
ra = Ripple current ratio

The ESL of capacitors depends on the technology chosen, but tends to range from 1 nH to 20 nH, where ceramic capacitors have the lowest inductance and electrolytic capacitors have the highest. The calculated contributing voltage ripple from ESL is shown for the switch on and switch off below:

$$V_{ESLON} = \frac{ESL * Ipp * F_{SW}}{D} \rightarrow 15.27\ mV = \frac{10\ nH * 1.2\ A * 350\ kHz}{27.5\%} \quad \text{(eq. 15)}$$

$$V_{ESLOFF} = \frac{ESL * Ipp * F_{SW}}{(1 - D)} \rightarrow 5.79\ mV = \frac{10\ nH * 1.2\ A * 350\ kHz}{(1 - 27.5\%)} \quad \text{(eq. 16)}$$

D = Duty ratio
ESL = Capacitor inductance
F_{SW} = Switching frequency
Ipp = Peak−to−peak current

The output capacitor is a basic component for the fast response of the power supply. For the first few microseconds of a load transient, the output capacitor supplies current to the load. Once the regulator recognizes a load transient, it adjusts the duty ratio, but the current slope is limited by the inductor value.

During a load step transient, the output voltage initially drops due to the current variation inside the capacitor and the ESR (neglecting the effect of the ESL).

$$\Delta V_{OUT-ESR} = I_{TRAN} \times Co_{ESR} \rightarrow 115\ mV = 2.3\ \times 50\ m\Omega \quad \text{(eq. 17)}$$

Co_{ESR} = Output capacitor Equivalent Series Resistance
I_{TRAN} = Output transient current
ΔV_{OUT_ESR} = Voltage deviation of V_{OUT} due to the effects of ESR

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to output capacitor discharge is given by the following equation:

$$\Delta V_{OUT-DIS} = \frac{(I_{TRAN})^2 \times L_{OUT}}{2 \times D_{MAX} C_{OUT} \times (V_{IN} - V_{OUT})} \rightarrow 4.9\ mV = \frac{(2.3\ A)^2 \times 5.6\ \mu H}{2 \times 75\% \times 470\ \mu F \times (12\ V - 3.3\ V)} \quad \text{(eq. 18)}$$

C_{OUT} = Output capacitance
D_{MAX} = Maximum duty ratio
I_{TRAN} = Output transient current
L_{OUT} = Output inductor value
V_{IN} = Input voltage
V_{OUT} = Output voltage
ΔV_{OUT_DIS} = Voltage deviation of V_{OUT} due to the effects of capacitor discharge

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. Please note that $\Delta V_{OUT-DIS}$ and $\Delta V_{OUT-ESR}$ are out of phase with each other, and the larger of these two voltages will determine the maximum deviation of the output voltage (neglecting the effect of the ESL).

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of the input ripple current is:

$$Iin_{RMS} = I_{OUT}\sqrt{D \times (1 - D)} \rightarrow 1.79\ A = 4\ A * \sqrt{27.5 * (1 - 27.5)} \quad \text{(eq. 19)}$$

D = Duty ratio
IIN_{RMS} = Input capacitance RMS current
I_{OUT} = Load current

The equation reaches its maximum value with D = 0.5. Loss in the input capacitors can be calculated with the following equation:

$$P_{CIN} = CIN_{ESR} * \left(IiN_{RMS}\right)^2 \rightarrow 32\ mW = 10\ m\Omega * \left(1.79\ A\right)^2 \quad \text{(eq. 20)}$$

CIN_{ESR} = Input capacitance Equivalent Series Resistance
IIN_{RMS} = Input capacitance RMS current
P_{CIN} = Power loss in the input capacitor

Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected, otherwise, capacitor failure could occur.

Power MOSFET Dissipation

MOSFET power dissipation, package size, and the thermal environment drive power supply design. Once the dissipation is known, the thermal impedance can be calculated to prevent the specified maximum junction temperatures from being exceeded at the highest ambient temperature.

Power dissipation has two primary contributors: conduction losses and switching losses. The high−side MOSFET will display both switching and conduction losses. The switching losses of the low side MOSFET will not be calculated as it switches into nearly zero voltage and the losses are insignificant. However, the body diode in the low−side MOSFET will suffer diode losses during the non−overlap time of the gate drivers.

Starting with the high−side MOSFET, the power dissipation can be approximated from:

$$P_{D\_HS} = P_{COND} + P_{SW\_TOT} \quad \text{(eq. 21)}$$

P_{COND} = Conduction power losses
P_{SW_TOT} = Total switching losses
P_{D_HS} = Power losses in the high side MOSFET

The first term in Equation 21 is the conduction loss of the high−side MOSFET while it is on.

$$P_{COND} = \left(I_{RMS\_HS}\right)^2 \cdot R_{DS(on)\_HS} \quad \text{(eq. 22)}$$

I_{RMS_HS} = RMS current in the high−side MOSFET
$R_{DS(on)\_HS}$ = On resistance of the high−side MOSFET
P_{cond} = Conduction power losses

Using the ra term from Equation 5, I_{RMS} becomes:

$$I_{RMS\_HS} = I_{OUT} \cdot \sqrt{D \cdot \left(1 + \frac{ra^2}{12}\right)} \quad \text{(eq. 23)}$$

I_{RMS_HS} = High side MOSFET RMS current
I_{OUT} = Output current
D = Duty ratio
ra = Ripple current ratio

The second term from Equation 21 is the total switching loss and can be approximated from the following equations.

$$P_{SW\_TOT} = P_{SW} + P_{DS} + P_{RR} \quad \text{(eq. 24)}$$

P_{DS} = High side MOSFET drain source losses
P_{RR} = High side MOSFET reverse recovery losses
P_{SW} = High side MOSFET switching losses
P_{SW_TOT} = High side MOSFET total switching losses

The first term for total switching losses from Equation 24 are the losses associated with turning the high−side MOSFET on and off and the corresponding overlap in drain voltage and current.

$$P_{SW} = P_{TON} + P_{TOFF} = \frac{1}{2} \cdot \left(I_{OUT} \cdot V_{IN} \cdot F_{SW}\right) \cdot \left(t_{RISE} + t_{FALL}\right) \quad \text{(eq. 25)}$$

F_{SW} = Switching frequency
I_{OUT} = Load current
t_{FALL} = MOSFET fall time
t_{RISE} = MOSFET rise time
V_{IN} = Input voltage
P_{SW} = High side MOSFET switching losses
P_{TON} = Turn on power losses
P_{TOFF} = Turn off power losses

When calculating the rise time and fall time of the high side MOSFET it is important to know the charge characteristic shown in Figure 22.

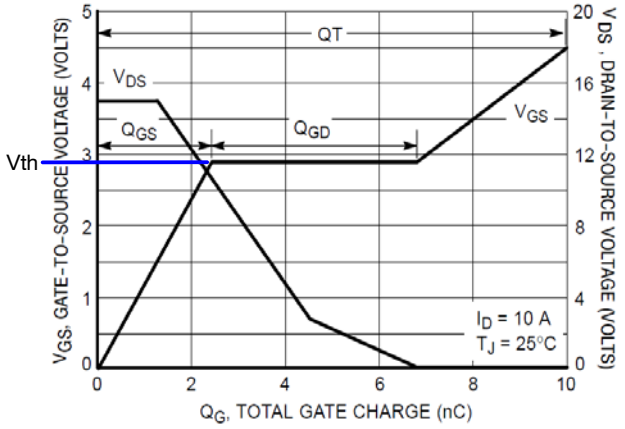


Figure 22. MOSFET Switching Characteristics

$$t_{RISE} = \frac{Q_{GD}}{I_{G1}} = \frac{Q_{GD}}{(V_{BST} - V_{TH})/(R_{HSPU} + R_G)} \quad \text{(eq. 26)}$$

I_{G1} = Output current from the high−side gate drive
Q_{GD} = MOSFET gate to drain gate charge
R_{HSPU} = Drive pull up resistance
R_G = MOSFET gate resistance
t_{RISE} = MOSFET rise time
V_{BST} = Boost voltage
V_{TH} = MOSFET gate threshold voltage

$$t_{FALL} = \frac{Q_{GD}}{I_{G2}} = \frac{Q_{GD}}{(V_{BST} - V_{TH})/(R_{HSPD} + R_G)} \quad \text{(eq. 27)}$$

I_{G2} = Output current from the low−side gate drive
Q_{GD} = MOSFET gate to drain gate charge
R_G = MOSFET gate resistance
R_{HSPD} = Drive pull down resistance
t_{FALL} = MOSFET fall time
V_{BST} = Boost voltage
V_{TH} = MOSFET gate threshold voltage

Next, the MOSFET output capacitance losses are caused by both the high−side and low−side MOSFETs, but are dissipated only in the high−side MOSFET.

$$P_{DS} = \frac{1}{2} \cdot C_{OSS} \cdot V_{IN}^2 \cdot F_{SW} \quad \text{(eq. 28)}$$

C_{OSS} = MOSFET output capacitance at 0V
F_{SW} = Switching frequency
P_{DS} = MOSFET drain to source charge losses
V_{IN} = Input voltage

Finally, the loss due to the reverse recovery time of the body diode in the low−side MOSFET is shown as follows:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot F_{SW} \quad \text{(eq. 29)}$$

F_{SW} = Switching frequency
P_{RR} = High side MOSFET reverse recovery losses
Q_{RR} = Reverse recovery charge
V_{IN} = Input voltage

The low−side MOSFET turns on into small negative voltages so switching losses are negligible. The low−side MOSFET's power dissipation only consists of conduction loss due to $R_{DS(on)}$ and body diode loss during the non−overlap periods.

$$P_{D\_LS} = P_{COND} + P_{BODY} \quad \text{(eq. 30)}$$

P_{BODY} = Low side MOSFET body diode losses
P_{COND} = Low side MOSFET conduction losses
P_{D_LS} = Low side MOSFET losses

Conduction loss in the low−side MOSFET is described as follows:

$$P_{COND} = \left(I_{RMS\_LS}\right)^2 \cdot R_{DS(on)\_LS} \quad \text{(eq. 31)}$$

I_{RMS_LS} = RMS current in the low side
$R_{DS(on)\_LS}$ = Low−side MOSFET on resistance
P_{COND} = High side MOSFET conduction losses

$$I_{RMS\_LS} = I_{OUT} \cdot \sqrt{(1 - D) \cdot \left(1 + \left(\frac{ra^2}{12}\right)\right)} \quad \text{(eq. 32)}$$

D = Duty ratio
I_{OUT} = Load current
I_{RMS_LS} = RMS current in the low side
ra = Ripple current ratio

The body diode losses can be approximated as:

$$P_{BODY} = V_{FD} \cdot I_{OUT} \cdot F_{SW} \cdot (NOL_{LH} + NOL_{HL}) \quad \text{(eq. 33)}$$

F_{SW} = Switching frequency
I_{OUT} = Load current
NOL_{HL} = Dead time between the high−side MOSFET turning off and the low−side MOSFET turning on, typically 50 ns
NOL_{LH} = Dead time between the low−side MOSFET turning off and the high−side MOSFET turning on, typically 50 ns
P_{BODY} = Low−side MOSFET body diode losses
V_{FD} = Body diode forward voltage drop

Control Dissipation

The control portion of the IC power dissipation is determined by the formula below:

$$P_C = I_{CC} \times V_{IN} \quad \text{(eq. 34)}$$

I_{CC} = Control circuitry current draw
P_C = Control power dissipation
V_{IN} = Input voltage

Once the IC power dissipations are determined, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case

ambient temperature. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D \cdot R_{\theta JA} \quad \text{(eq. 35)}$$

P_D = Power dissipation of the IC
$R_{\theta JA}$ = Thermal resistance junction to ambient of the regulator package
T_A = Ambient temperature
T_J = Junction temperature

As with any power design, proper laboratory testing should be performed to ensure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e., worst case MOSFET $R_{DS(on)}$).

Compensation Network

To create a stable power supply, the compensation network around the transconductance amplifier must be used in conjunction with the PWM generator and the power stage. Since the power stage design criteria is set by the application, the compensation network must correct the over all system response to ensure stability. The output inductor and capacitor of the power stage form a double pole at the frequency as shown in Equation 36:

$$F_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \rightarrow$$
$$3.102\ \text{kHz} = \frac{1}{2\pi \times \sqrt{5.6\ \mu\text{H} \times 470\ \mu\text{F}}} \quad \text{(eq. 36)}$$

C_{OUT} = Output capacitor
F_{LC} = Double pole inductor and capacitor frequency
L_{OUT} = Output inductor value

The ESR of the output capacitor creates a “zero” at the frequency as shown in Equation 37:

$$F_{ESR} = \frac{1}{2\pi \times CO_{ESR} \times C_{OUT}} \rightarrow$$
$$6.772\ \text{kHz} = \frac{1}{2\pi \times 0.050\ \text{m}\Omega \times 470\ \mu\text{F}} \quad \text{(eq. 37)}$$

CO_{ESR} = Output capacitor ESR
C_{OUT} = Output capacitor
F_{LC} = Output capacitor ESR frequency

The two equations above define the bode plot that the power stage has created or open loop response of the system. The next step is to close the loop by considering the feedback values. The closed loop crossover frequency should be greater than the F_{LC} and less than 1/5 of the switching frequency, which would place the maximum crossover frequency at 70 kHz. Further, the calculated F_{ESR} frequency should meet the following:

$$F_{ESR} < \frac{F_{SW}}{5} \quad \text{(eq. 38)}$$

F_{SW} = Switching frequency
F_{ESR} = Output capacitor ESR zero frequency

If the criteria is not met, the compensation network may not provide stability and the output power stage must be modified.

Figure 23 shows a pseudo Type III transconductance error amplifier.

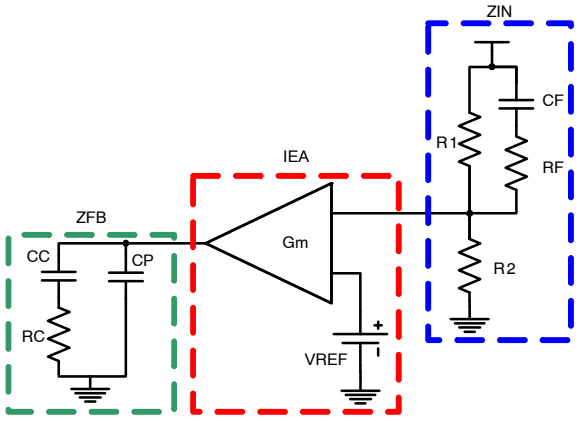


Figure 23. Pseudo Type III Transconductance Error Amplifier

The compensation network consists of the internal OTA and the impedance networks Z_{IN} (R_1, R_2, R_F, and C_F) and external Z_{FB} (R_C, C_C, and C_P). The compensation network has to provide a closed loop transfer function with the highest 0 dB crossing frequency to have fast response and the highest gain in DC conditions to minimize the load regulation issues. A stable control loop has a gain crossing with −20 dB/decade slope and a phase margin greater than 45°. Include worst−case component variations when determining phase margin. To start the design, a resistor value should be chosen for R_2 from which all other components can be chosen. A good starting value is 10 kΩ.

The NCP3125 allows the output of the DC−DC regulator to be adjusted down to 0.8 V via an external resistor divider network. The regulator will maintain 0.8 V at the feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to V_{OUT}, the regulator will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin.

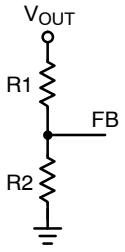


Figure 24. Feedback Resistor Divider

The relationship between the resistor divider network above and the output voltage is shown in Equation 39:

$$R_2 = R_1 \cdot \left(\frac{V_{REF}}{V_{OUT} - V_{REF}} \right) \quad \text{(eq. 39)}$$

R_1 = Top resistor divider
R_2 = Bottom resistor divider
V_{OUT} = Output voltage
V_{REF} = Regulator reference voltage

The most frequently used output voltages and their associated standard R_1 and R_2 values are listed in Table 5.

Table 5. OUTPUT VOLTAGE SETTINGS

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	1.0	Open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.6	10
5.0	52.3	10

The compensation components for the Pseudo Type III Transconductance Error Amplifier can be calculated using the method described below. The method serves to provide a good starting place for compensation of a power supply. The values can be adjusted in real time using the compensation tool comp calc, available for download at ON Semiconductor's website.

The value of the feed through resistor should always be at least 2X the value of R_2 to minimize error from feed through noise. Using the 2X assumption, R_F will be set to 20 kΩ and the feed through capacitor can be calculated as shown below:

$$C_F = \frac{(R_1 + R_2)}{2\pi \times (R_1 + R_F + R_2 \times R_F + R_2 \times R_1) \times f_{cross}} \quad \text{(eq. 40)}$$

$$0.96\ nF = \frac{(31.6\ k\Omega + 10\ k\Omega)}{2\pi \times (31.6\ k\Omega \times 20\ k\Omega + 10\ k\Omega \times 20\ k\Omega + 10\ k\Omega \times 31.6\ k\Omega) \times 30\ kHz}$$

C_F = Feed through capacitor
f_{cross} = Crossover frequency
R_1 = Top resistor divider
R_2 = Bottom resistor divider
R_F = Feed through resistor

The cross over of the overall feedback occurs at F_{PO}:

$$F_{PO} = \frac{(R_1 + R_F)}{(2\pi)^2 \times (C_F)^2 \left[(R_1 + R_F) \times R_2 + R_1 \times R_F\right] \times (R_F + R_1)} \times \frac{V_{ramp}}{FLC \times V_{IN}} \rightarrow \quad \text{(eq. 41)}$$

$$1.152\ kHz = \frac{(31.6\ k\Omega + 20\ k\Omega)}{(2\pi)^2 \times (0.96)^2 \left[(31.6\ k\Omega + 20\ k\Omega) \times 10\ k\Omega + 31.6\ k\Omega \times 20\ k\Omega\right] \times (20\ k\Omega + 31.6\ k\Omega)} \times \frac{1.1\ V}{3.102\ kHz \times 12\ V}$$

C_F = Feed through capacitor
F_{LC} = Frequency of the output inductor and capacitor
F_{PO} = Pole frequency
R_1 = Top of resistor divider
R_2 = Bottom of resistor divider
R_F = Feed through resistor
V_{IN} = Input voltage
V_{ramp} = Peak−to−peak voltage of the ramp

The cross over combined compensation network can be used to calculate the transconductance output compensation network as follows:

$$C_C = \frac{1}{F_{PO}} \times \frac{R_2}{R_2 \times R_1} \times gm \rightarrow \quad \text{(eq. 42)}$$

$$84\ nF = \frac{1}{1.152\ kHz} \times \frac{10\ k\Omega}{10\ k\Omega + 31.6\ k\Omega} \times 4\ ms$$

C_C = Compensation capacitor
F_{PO} = Pole frequency
gm = Transconductance of amplifier
R_1 = Top of resistor divider
R_2 = Bottom of resistor divider

$$R_C = \frac{1}{2 \times F_{LC} \times C_C \times \left(\sqrt{2}/2 + f_{cross} \times CO_{ESR} \times C_{OUT}\right)} \quad \text{(eq. 43)}$$

$$1.355\ k\Omega = \frac{1}{2 \times 3.102\ kHz \times 84\ nF \times \left(\sqrt{2}/2 + 30\ kHz \times 0.05\ m\Omega \times 470\ \mu F\right)}$$

C_C = Compensation capacitance
CO_{ESR} = Output capacitor ESR
C_{OUT} = Output capacitance
f_{cross} = Crossover frequency
F_{LC} = Output inductor and capacitor frequency
R_C = Compensation resistor

$$C_P = C_{OUT} \times \frac{CO_{ESR}}{R_C \times 2 \times \pi} \rightarrow \quad \text{(eq. 44)}$$

$$2.76\ nF = 470\ \mu F \times \frac{0.05\ m\Omega}{1.355\ k\Omega \times 2 * \pi}$$

CO_{ESR} = Output capacitor ESR
C_{OUT} = Output capacitor
C_P = Compensation pole capacitor
R_C = Compensation resistor

Assuming an output capacitance of 470 μF in parallel with 22 μF with a crossover frequency of 35 kHz, the compensation values for common output voltages can be calculated as shown in Table 6:

Table 6. COMPENSATION VALUES

V_{in} (V)	V_{out} (V)	L_{out} (μF)	RF (kΩ)	Cf (nF)	Cc (nF)	Rc (kΩ)	Cp (nF)
12	0.8	2.2	X	X	150	0.243	5.6
12	1.2	2.7	20	1	100	0.412	2.7
12	1.5	2.7	20	1	100	0.487	2.7
12	1.8	3.9	20	1	120	0.806	1.8
12	2.5	4.7	20	1	82	1.07	1.5
12	3.3	5.6	20	1	68	1.4	1.2
12	5.0	6.8	20	1	47	1.96	0.82
5	0.8	1.8	20	1	68	0.453	1
5	1.2	2.7	20	1	56	0.953	1
5	1.5	2.7	20	1	39	1.15	0.82
5	1.8	3.3	20	1	33	1.5	0.68
5	2.5	3.3	20	1	27	1.82	0.56

Calculating Soft−Start Time

To calculate the soft−start delay and soft−start time, the following equations can be used.

$$t_{SSdelay} = \frac{(C_P + C_C) \times 0.9\ V}{I_{SS}} \rightarrow \quad \text{(eq. 45)}$$

$$7.45\ ms = \frac{(2.83\ nF + 80\ nF) \times 0.9\ V}{10\ \mu A}$$

C_P = Compensation pole capacitor
C_C = Compensation capacitor
I_{SS} = Soft−start current

The time the output voltage takes to increase from 0 V to a regulated output voltage is t_{ss} as shown in Equation 46:

$$t_{SS} = \frac{(C_P + C_C) \times D \times V_{ramp}}{I_{SS}} \quad \text{(eq. 46)}$$

$$2.51\ ms = \frac{(2.83\ nF + 80\ nF) \times 27.5\% \times 1.1\ V}{10\ \mu A}$$

C_P = Compensation pole capacitor
C_C = Compensation capacitor
D = Duty ratio
I_{SS} = Soft−start current
t_{SS} = Soft−start interval
V_{ramp} = Peak−to−peak voltage of the ramp

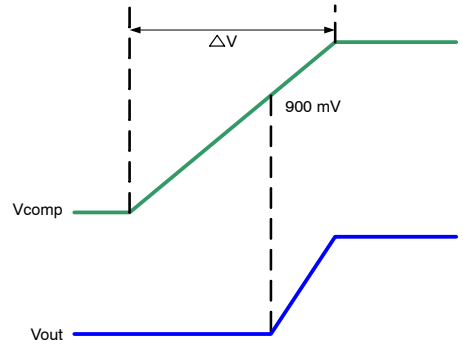


Figure 25. Soft−Start Ramp

The delay from the charging of the compensation network to the bottom of the ramp is considered $t_{ssdelay}$. The total delay time is the addition of the current set delay and $t_{ssdelay}$, which in this case is 9 ms and 7.45 ms respectively, for a total of 16.45 ms.

Calculating Input Inrush Current

The input inrush current has two distinct stages: input charging and output charging. The input charging of a buck stage is usually not controlled, and is limited only by the input RC network, and the output impedance of the upstream power stage. If the upstream power stage is a perfect voltage source, then the input charge inrush current can be depicted as shown in Figure 26 and calculated as:

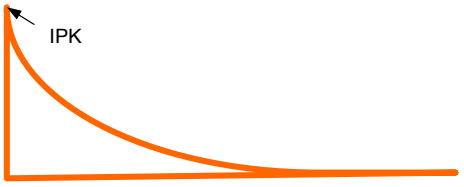


Figure 26. Input Charge Inrush Current

$$I_{ICinrush\_PK}1 = \frac{V_{IN}}{CIN_{ESR}} \quad \text{(eq. 47)}$$

$$120\ A = \frac{12}{0.1}$$

$$I_{ICinrush\_RMS}1 = \frac{V_{IN}}{CIN_{ESR}} \times \left(1 - \frac{1}{e^{\left[\frac{t_{DELAY\_TOTAL}}{CIN_{ESR} \times C_{IN}}\right]}} \right) \times 0.316 \times \frac{5 \times CIN_{ESR} \times C_{IN}}{t_{DELAY\_TOTAL}} \quad \text{(eq. 48)}$$

$$380\ mA = \frac{12\ V}{0.1\ \Omega} \times \left(1 - \frac{1}{e^{\left[\frac{16.45\ ms}{0.1\Omega \times 330\ \mu F}\right]}} \right) \times 0.316 \times \frac{5 \times 0.1\ \Omega \times 330\ \mu F}{16.45\ ms}$$

C_{IN} = Output capacitor
CIN_{ESR} = Output capacitor ESR
t_{DELAY_TOTAL} = Total delay interval
V_{IN} = Input voltage

Once the t_{DELAY_TOTAL} has expired, the buck converter starts to switch and a second inrush current can be calculated:

$$I_{OCinrush\_RMS} = \frac{\left(C_{OUT} + C_{LOAD}\right) \times V_{OUT}}{t_{SS}} \frac{D}{\sqrt{3}} + I_{CL} \times D \quad \text{(eq. 49)}$$

C_{OUT} = Total converter output capacitance
C_{LOAD} = Total load capacitance
D = Duty ratio of the load
I_{CL} = Applied load at the output
$I_{OCinrush\_RMS}$ = RMS inrush current during start−up
t_{SS} = Soft−start interval
V_{OUT} = Output voltage

From the above equation, it is clear that the inrush current is dependant on the type of load that is connected to the output. Two types of load are considered in Figure 27: a resistive load and a stepped current load.

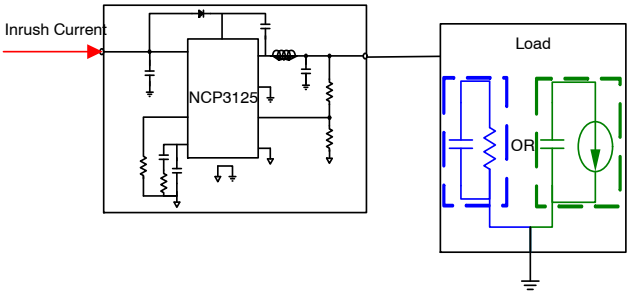


Figure 27. Load Connected to the Output Stage

If the load is resistive in nature, the output current will increase with soft−start linearly which can be quantified in Equation 50.

$$I_{CLR\_RMS} = \frac{1}{\sqrt{3}} \times \frac{V_{OUT}}{R_{OUT}} \qquad I_{CR\_PK} = \frac{V_{OUT}}{R_{OUT}} \quad \text{(eq. 50)}$$

$$191\ mA = \frac{1}{\sqrt{3}} \times \frac{3.3\ V}{10\ \Omega} \qquad 330\ mA = \frac{3.3\ V}{10\ \Omega}$$

R_{OUT} = Output resistance
V_{OUT} = Output voltage
I_{CLR_RMS} = RMS resistor current
I_{CR_PK} = Peak resistor current

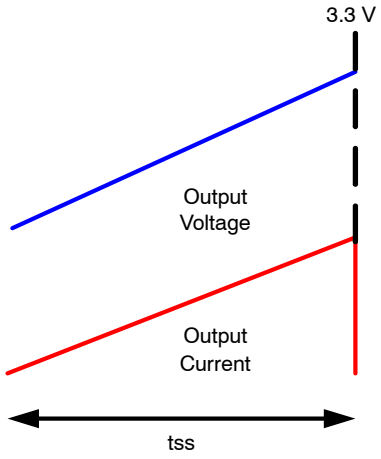


Figure 28. Resistive Load Current

Alternatively, if the output has an under voltage lockout, turns on at a defined voltage level, and draws a consistent current, then the RMS connected load current is:

$$I_{CLI} = \sqrt{\frac{V_{OUT} - V_{OUT\_TO}}{V_{OUT}}} \times I_{OUT} \qquad \text{(eq. 51)}$$

$$798\ mA = \sqrt{\left(\frac{(3.3\ V - 1.2\ V)}{3.3\ V}\right)} \times 1\ A$$

I_{OUT} = Output current
V_{OUT} = Output voltage
V_{OUT_TO} = Output voltage load turn on

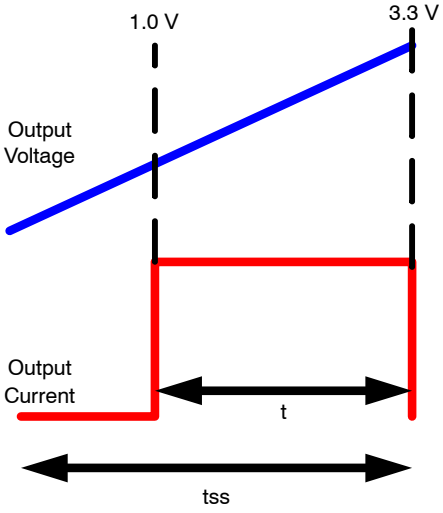


Figure 29. Voltage Enable Load Current

If the inrush current is higher than the steady state input current during max load, then an input fuse should be rated accordingly using I^2t methodology.

Layout Considerations

As in any high frequency switching regulator, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. The interconnecting impedances should be minimized by using wide short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding. For optimal performance, the NCP3125 should have a layout similar to the one shown in Figure 30. An important note is that the input voltage to the NCP3125 should have local decoupling to PGND. The recommended decoupling for input voltage is a 1 μF general purpose ceramic capacitor and a 0.01 μF COG ceramic capacitor placed in parallel.

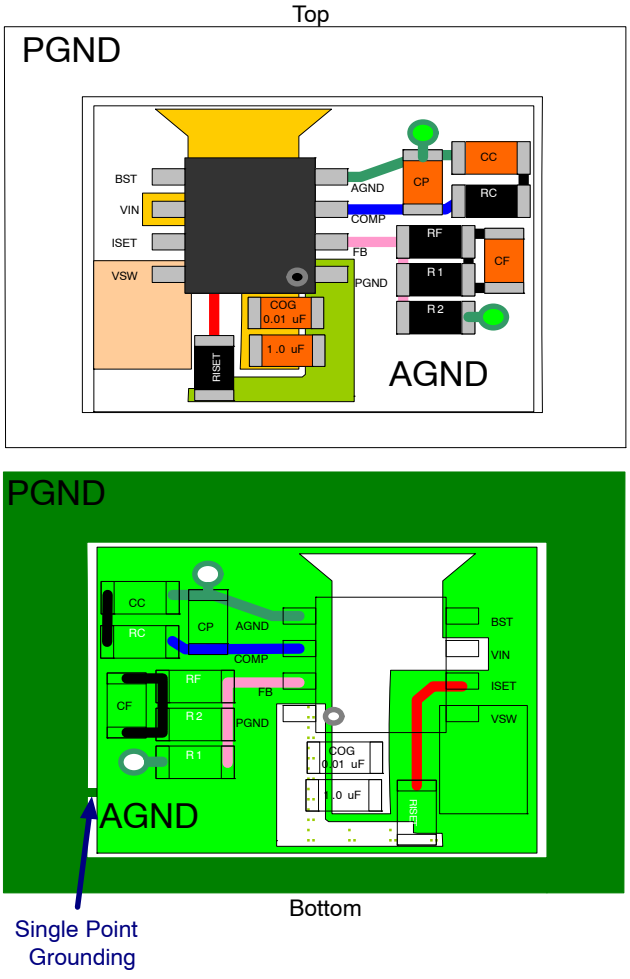


Figure 30. Recommended Layout

The typical applications are shown in Figures 31 and 32 for output electrolytic and ceramic bulk capacitors, respectively.

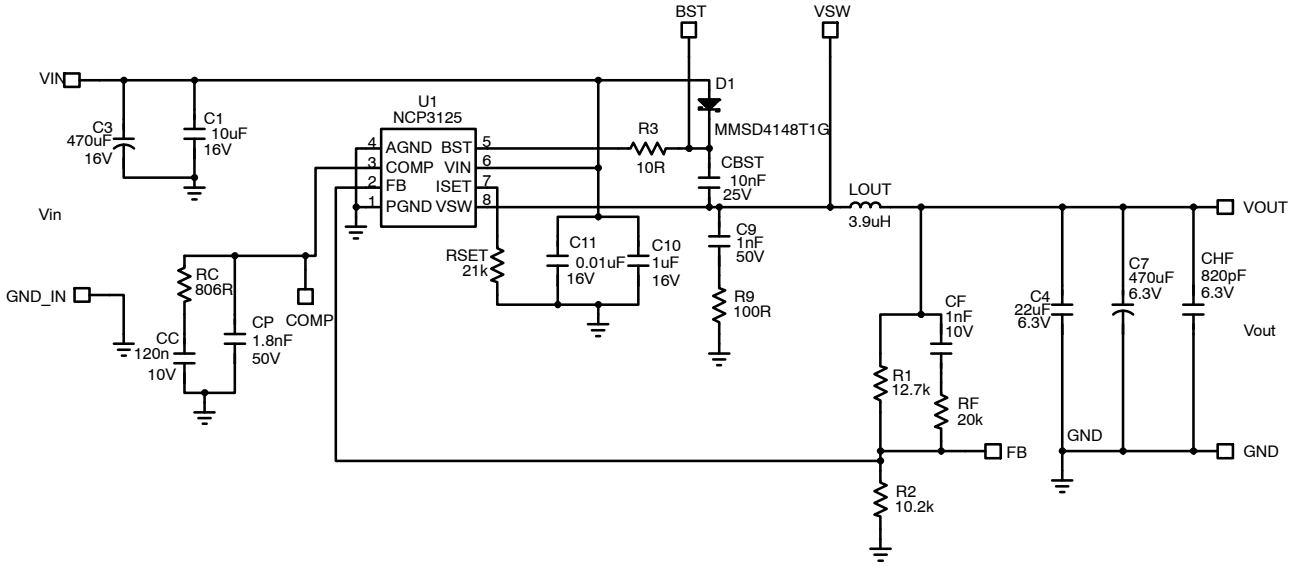


Figure 31. Standard Application 12 V to 1.8 V 4 A

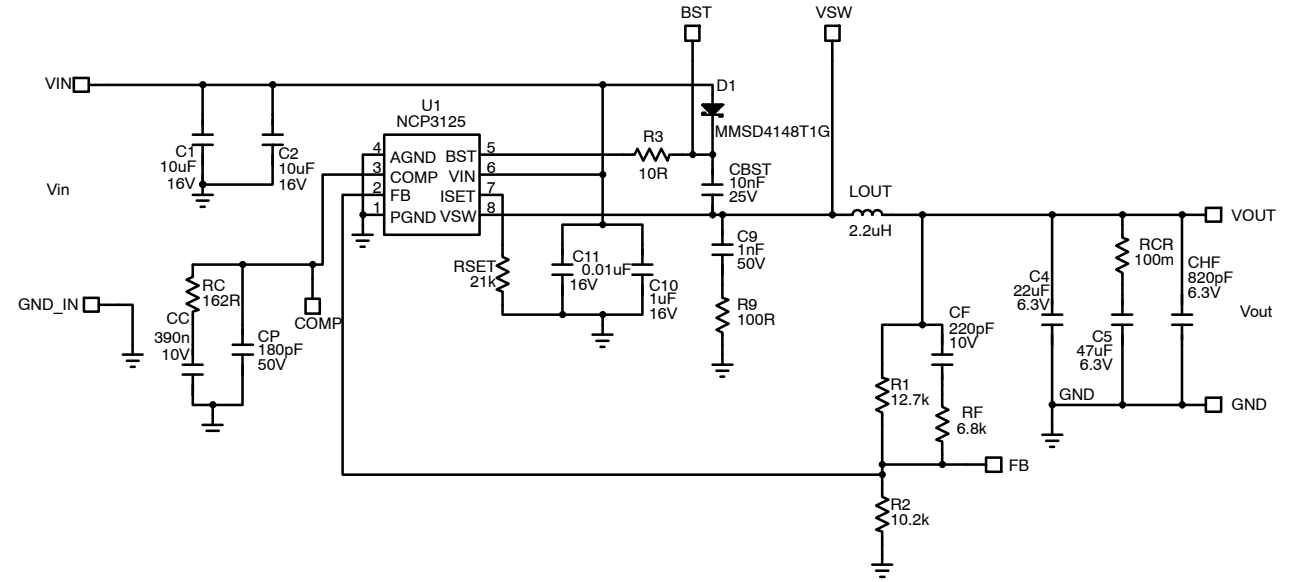


Figure 32. Ceramic Capacitor Application 12 V to 1.8 V 4 A

ORDERING INFORMATION

Device	Package	Shipping†
NCP3125ADR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

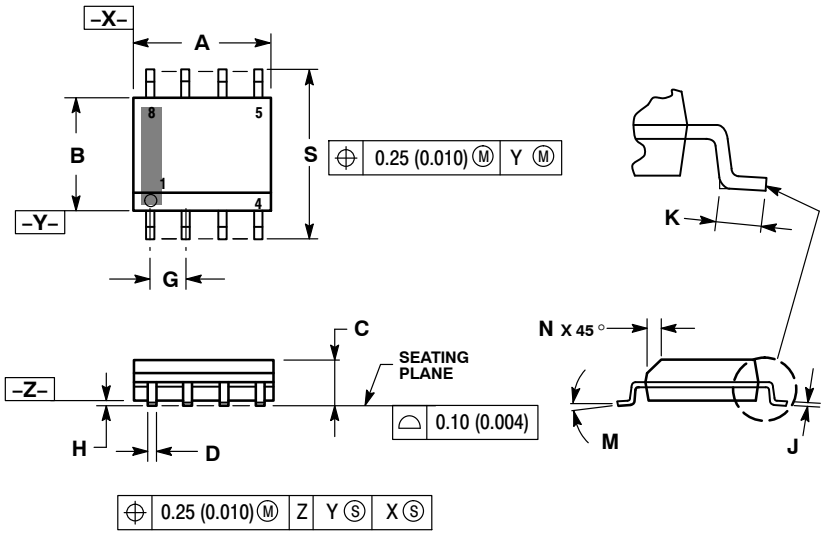
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

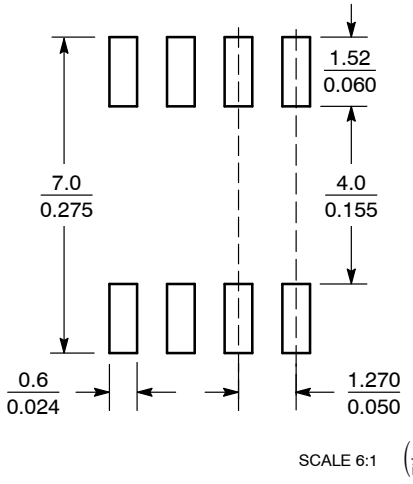
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

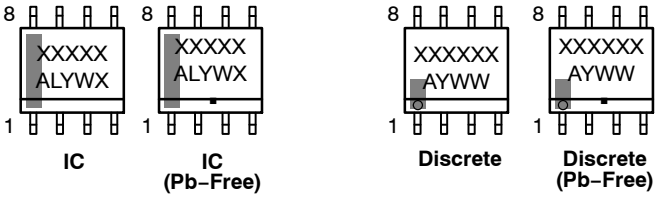
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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