TPS61086 18.5-V PFM – PWM Step-Up DC – DC Converter With 2.0-A Switch

1 Features

- 2.3-V to 6.0-V Input Voltage Range
- 18.5-V Boost Converter With 2.0-A Switch Current
- 1.2-MHz Switching Frequency
- Power Save Mode for Improved Efficiency at Low-Output Power or Forced PWM
- Adjustable Soft-Start
- Thermal Shutdown
- Undervoltage Lockout
- 10-Pin VSON Package

2 Applications

- Handheld Devices
- GPS Receivers
- Digital Still Cameras
- Portable Applications
- DSL Modems
- PCMCIA Cards
- TFT LCD Bias Supply

3 Description

The TPS61086 device is a high-frequency, high-efficiency DC-to-DC converter with an integrated 2.0-A, 0.13-Ω power switch capable of providing an output voltage up to 18.5 V. The implemented boost converter is based on a fixed frequency of 1.2-MHz, pulse-width-modulation (PWM) controller that allows the use of small external inductors and capacitors and provides fast transient response.

At light-load, the device can operate in Power Save Mode with pulse-frequency-modulation (PFM) to improve the efficiency while keeping a low-output voltage ripple. For very noise-sensitive applications, the device can be forced to PWM Mode operation over the entire load range by pulling the MODE pin high. The external compensation allows optimizing the application for specific conditions. A capacitor connected to the soft-start pin minimizes inrush current at start-up.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61086	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

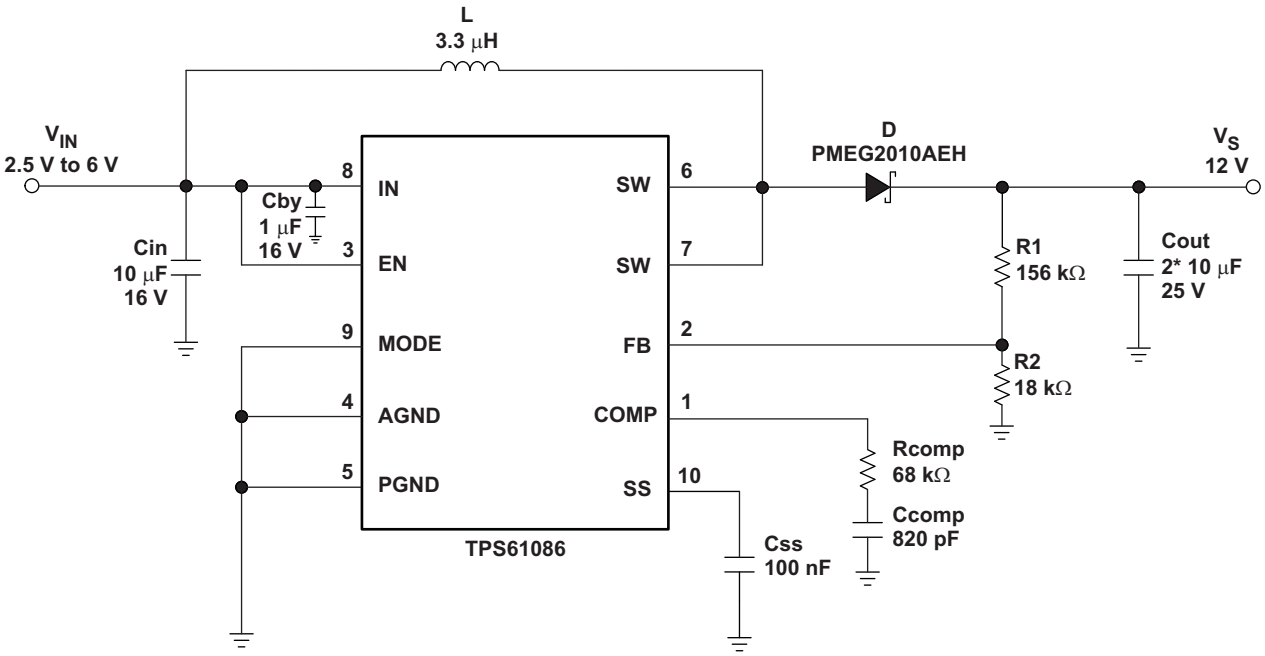


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2015) to Revision B **Page**

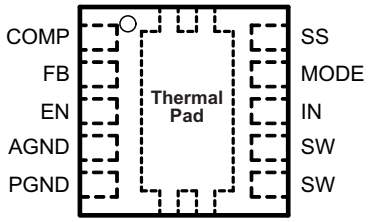
- Changed "FREQ" to "MODE" in Absolute Maximum Ratings table ... 4
- Changed "mA" to "A" in X-axis label for Figure 4 ... 6
- Changed V_S from "12V/50 mA" to "12V/500 mA" in Figure 7. ... 10

Changes from Original (August 2009) to Revision A **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table ... 1

5 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	1	I/O	Compensation pin
FB	2	I	Feedback pin
EN	3	I	Shutdown control input. Connect this pin to logic high level to enable the device
AGND	4	—	Analog ground
	Thermal Pad		
PGND	5	—	Power ground
SW	6	—	Switch pin
	7		
IN	8	—	Input supply pin
MODE	9	I	Operating mode selection pin. MODE = 'high' for forced PWM operation. MODE = 'low' for PFM operation
SS	10	—	Soft-start control pin. Connect a capacitor to this pin if soft-start needed. Open = no soft-start

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage IN(2)	–0.3	7	V
Voltage on pins EN, FB, SS, MODE, COMP	–0.3	7	V
Voltage on pin SW	–0.3	20	V
Operating junction temperature	–40	150	°C
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	2.3	6	V
V_S	Boost output voltage	V_{IN} + 0.5	18.5	V
T_A	Operating free-air temperature	–40	85	°C
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS61086 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 3.3 V, EN = IN, V_S = 12 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.3		6	V
I_Q	Operating quiescent current into IN	Device not switching, V_{FB} = 1.3 V		75	100	µA
I_{SDVIN}	Shutdown current into IN	EN = GND			1	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling			2.2	V
		V_{IN} rising			2.3	V
T_{SD}	Thermal shutdown	Temperature rising		150		°C
T_{SDHYS}	Thermal shutdown hysteresis			14		°C
LOGIC SIGNALS EN, FREQ						
V_{IH}	High level input voltage	V_{IN} = 2.3 V to 6 V	2			V
V_{IL}	Low level input voltage	V_{IN} = 2.3 V to 6 V			0.5	V
I_{INLEAK}	Input leakage current	EN = GND			0.1	µA
BOOST CONVERTER						
V_S	Boost output voltage		V_{IN} + 0.5		18.5	V
V_{FB}	Feedback regulation voltage		1.23	1.238	1.246	V
gm	Transconductance error amplifier			107		µA/V
I_{FB}	Feedback input bias current	V_{FB} = 1.238 V			0.1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 5 V, I_{SW} = current limit		0.13	0.2	Ω
		V_{IN} = V_{GS} = 3.3 V, I_{SW} = current limit		0.16	0.23	
I_{SWLEAK}	SW leakage current	EN = GND, V_{SW} = 6 V			10	µA
I_{LIM}	N-channel MOSFET current limit		2	2.6	3.2	A
I_{SS}	Soft-start current	V_{SS} = 1.238 V	7	10	13	µA
f_S	Oscillator frequency		0.9	1.2	1.5	MHz
	Line regulation	V_{IN} = 2.3 V to 6 V, I_{OUT} = 10 mA		0.0002		%/V
	Load regulation	V_{IN} = 3.3 V, I_{OUT} = 1 mA to 400 mA		0.11		%/A

6.6 Typical Characteristics

The typical characteristics are measured with the inductor CDRH6D12 3.3 µH from Sumida and the rectifier diode SL22.

Table 1. Table of Graphs

			FIGURE
η	Efficiency vs Load current- PFM	V_{IN} = 3.3 V, V_S = 9 V, 12 V, 15 V	Figure 1
η	Efficiencyvs Load current - Forced PWM	V_{IN} = 3.3 V, V_S = 9 V, 12 V, 15 V	Figure 2
$I_{out(max)}$	Maximum output current		Figure 3
f_S	Switching frequency - Forced PWM	vs Load current, V_{IN} = 3.3 V, V_S = 12 V	Figure 4
f_S	Switching frequency - Forced PWM	vs Supply voltage, V_S = 12 V, I_{out} = 200 mA	Figure 5
	Supply current	vs Supply voltage,V_{IN} = 3.3 V, V_S = 12 V	Figure 6

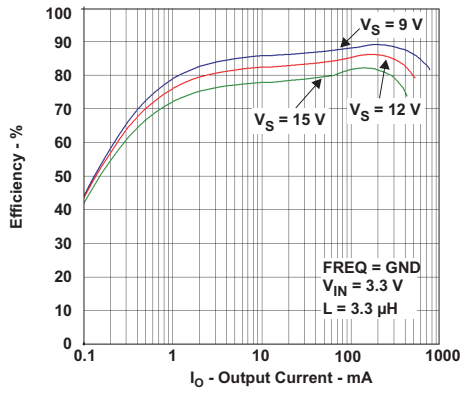


Figure 1. PFM Mode Efficiency vs Output Current

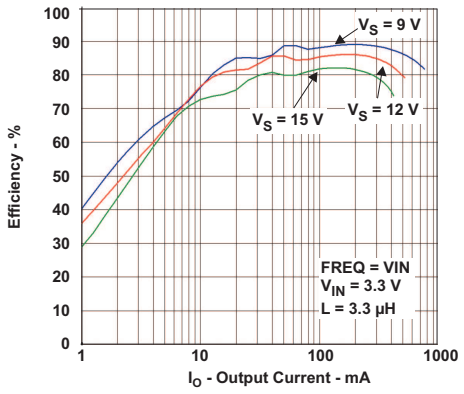


Figure 2. Force PWM Mode Efficiency vs Output Current

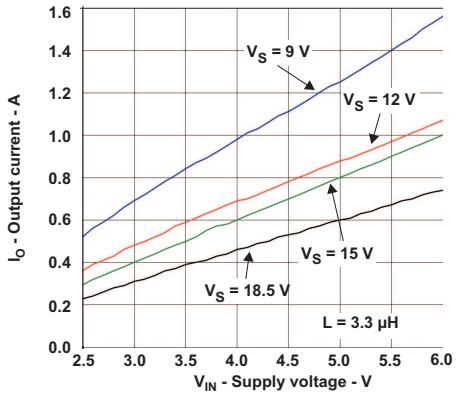


Figure 3. Output Current vs Supply Voltage

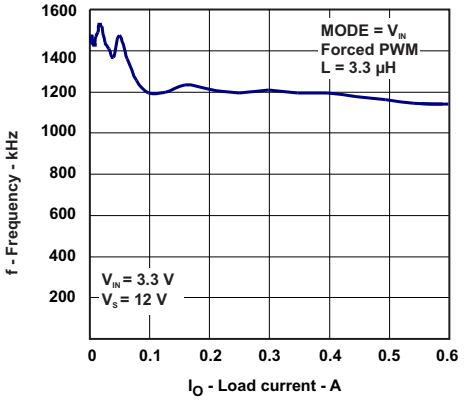


Figure 4. Frequency vs Load Current

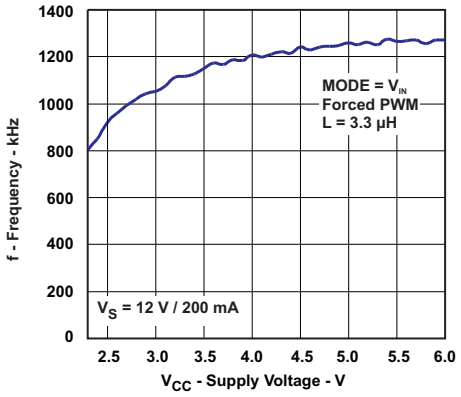


Figure 5. Frequency vs Supply Voltage

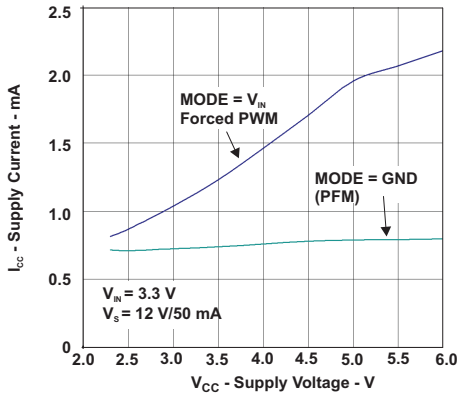


Figure 6. Supply Current vs Supply Voltage

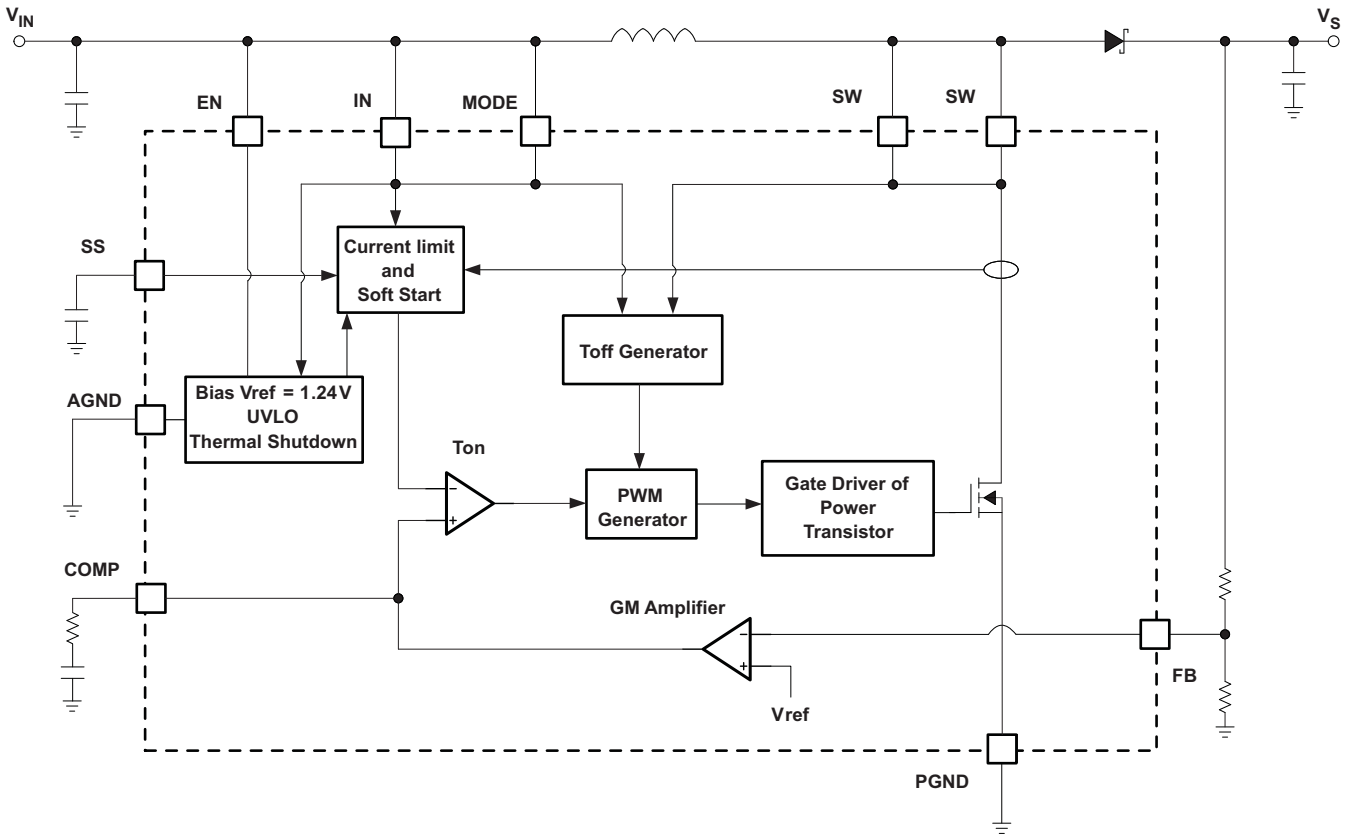
7 Detailed Description

7.1 Overview

The boost converter is designed for output voltages up to 18.5 V with a switch peak current limit of 2.0 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is fixed to 1.2 MHz and the minimum input voltage is 2.3 V. To limit the inrush current at start-up a soft-start pin is available.

TPS61086 boost converter's novel topology using adaptive OFF-time provides superior load and line transient responses and operates also over a wider range of applications than conventional converters.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft-Start

The boost converter has an adjustable soft-start to prevent high inrush current during start-up. To minimize the inrush current during start-up an external capacitor, connected to the soft-start pin SS and charged with a constant current, is used to slowly ramp up the internal current limit of the boost converter. When the EN pin is pulled high, the soft-start capacitor C_{SS} is immediately charged to 0.3 V. The capacitor is then charged at a constant current of 10 µA typically until the output of the boost converter V_S has reached its Power Good threshold (90% of V_S nominal value). During this time, the SS voltage directly controls the peak inductor current, starting with 0 A at V_{SS} = 0.3 V up to the full current limit at V_{SS} ≈ 800 mV. The maximum load current is available after the soft-start is completed. The larger the capacitor the slower the ramp of the current limit and the longer the soft-start time. A 100 nF capacitor is usually sufficient for most of the applications. When the EN pin is pulled low, the soft-start capacitor is discharged to ground.

Feature Description (continued)

7.3.2 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages an undervoltage lockout is included that disables the device, if the input voltage falls below 2.2 V.

7.3.3 Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically the thermal shutdown happens at a junction temperature of 150°C. When the thermal shutdown is triggered the device stops switching until the junction temperature falls below typically 136°C. Then the device starts switching again.

7.3.4 Overvoltage Prevention

If overvoltage is detected on the FB pin (typically 3% above the nominal value of 1.238 V) the part stops switching immediately until the voltage on this pin drops to its nominal value. This prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

7.4 Device Functional Modes

7.4.1 Power Save Mode

Connecting the MODE pin to GND (or any low logic level) enables the Power Save Mode operation. The converter operates in quasi fixed frequency PWM (Pulse Width Modulation) mode at moderate to heavy load and in the PFM (Pulse Frequency Modulation) mode during light loads, which maintains high efficiency over a wide load current range.

In PFM mode the converter is skipping switch pulses. However, within a PFM pulse, the switching frequency is still fixed to 1.2 MHz typically and the duty cycle determined by the input and output voltage. Therefore, the inductor peak current will remain constant for a defined application. With an increasing output load current, the PFM pulses become closer and closer (the PFM mode frequency gets higher) until no pulse is skipped anymore: the device operates then in CCM (Continuous Conduction Mode) with normal PWM mode.

The PFM mode frequency (between each PFM pulse) depends on the load current, the external components like the inductor or the output capacitor values as well as the output voltage. The device enters Power Save Mode as the inductor peak current falls below a 0.6A typically and switches until V_S is 1% higher than its nominal value. The converter stops switching when $V_S = V_S + 0.5\%$. The output voltage will thenrefore oscillate between 0.5% and 1% more than its nominal value which will provide excellent transient response to sudden load change, since the output voltage drop will be reduced due to this slight positive offset (see Figure 12).

7.4.2 Forced PWM Mode

Pulling the MODE pin high forces the converter to operate in a continuous PWM mode evan at light load currents. The advantage is that the converter operates with a quai constant frequency that allows simple filtering of the swithcing frequency for noise-sensitive applications. In this mode and at light load, the efficiency is lower compared to the Power Save Mode.

For additional flexibility, it is possible to switch from Power Save Mode to Forced PWM Mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61086 is designed for output voltages up to 18.5 V with a switch peak current limit of 2.0 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is fixed to 1.2 MHz and the minimum input voltage is 2.3 V. To limit the inrush current at start-up, a soft-start pin is available.

TPS61086 boost converter's novel topology using adaptive off-time provides superior load and line transient responses and operates also over a wider range of applications than conventional converters.

8.2 Typical Applications

8.2.1 3.3-V to 12-V Boost Converter With PFM Mode at Light Load

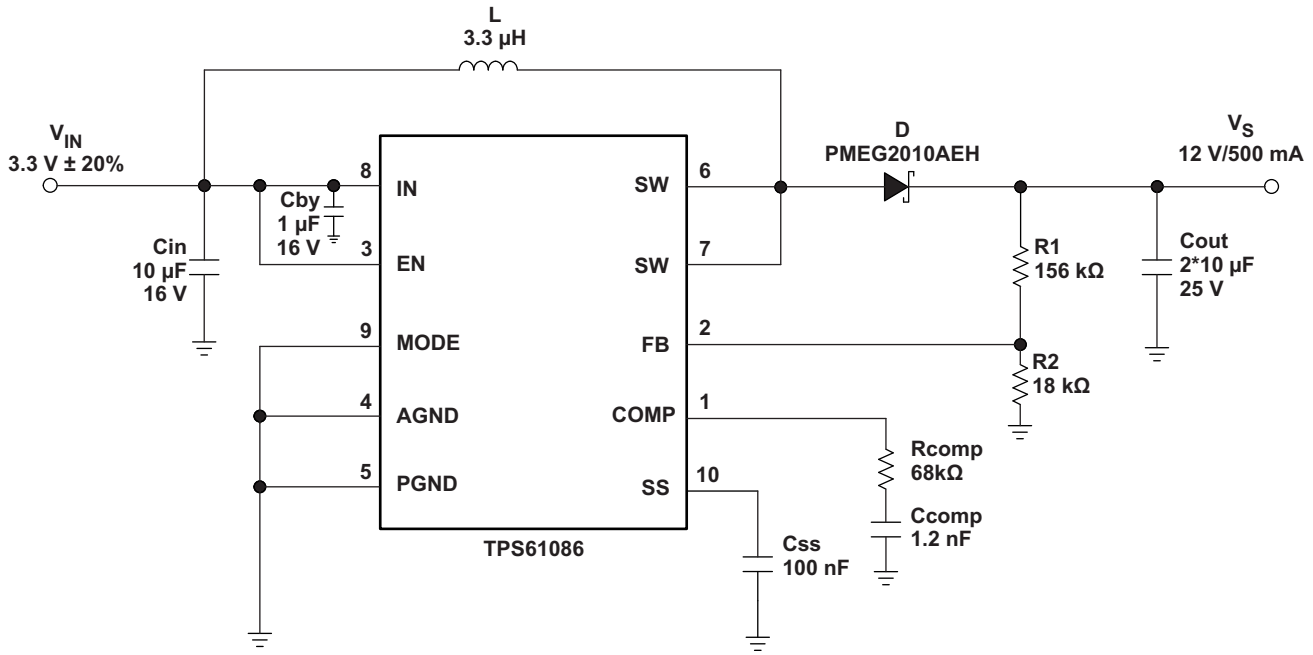


Figure 7. Typical Application, 3.3 V to 12 V (PFM Mode)

8.2.1.1 Design Requirements

For this example, the design parameters are listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage	3.3 V ± 20%
Output Voltage	12 V
Output Current	500 mA
Operation Mode at Light Load	PFM

8.2.1.2 Detailed Design Procedure

The first step in the design procedure is to verify that the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, for example, 90%.

1. Duty cycle, *D*:

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_S} \tag{1}$$

2. Maximum output current, $I_{out(max)}$:

$$I_{out(\max)} = \left(I_{LIM(\min)} - \frac{\Delta I_L}{2} \right) \cdot (1 - D) \tag{2}$$

3. Peak switch current in application, I_{swpeak} :

$$I_{swpeak} = \frac{\Delta I_L}{2} + \frac{I_{out}}{1 - D} \tag{3}$$

with the inductor peak-to-peak ripple current, ΔI_L

$$\Delta I_L = \frac{V_{IN} \cdot D}{f_S \cdot L}$$

where

- V_{IN} is Minimum input voltage.
- V_S is Output voltage.
- $I_{LIM(min)}$ is Converter switch current limit (minimum switch current limit = 2.0 A).
- f_S is Converter switching frequency (typically 1.2 MHz).
- *L* is Selected inductor value.
- η is Estimated converter efficiency (please use the number from the efficiency plots or 90% as an estimation.

(4)

The peak switch current is the steady-state peak switch current that the integrated switch, inductor and external Schottky diode has to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.

8.2.1.2.1 Inductor Selection

The TPS61086 is designed to work with a wide range of inductors. The main parameter for the inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated in the *Detailed Design Procedure* section with additional margin to cover for heavy load transients. An alternative, more conservative, is to choose an inductor with a saturation current at least as high as the maximum switch current limit of 3.2 A. The other important parameter is the inductor DC resistance. Usually the lower the DC resistance the higher the efficiency.

NOTE

The inductor DC resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and core material of the inductor influences the efficiency as well.

Usually an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. For the TPS61086, inductor values between 3 µH and 6 µH are a good choice. Possible inductors are shown in Table 3.

Typically, TI recommends that the inductor current ripple is below 35% of the average inductor current. The following equation can therefore be used to calculate the inductor value, *L*:

$$L = \left(\frac{V_{IN}}{V_S}\right)^2 \cdot \left(\frac{V_S - V_{IN}}{I_{out} \cdot f_S}\right) \cdot \left(\frac{\eta}{0.35}\right)$$

where

- V_{IN} is Minimum input voltage.
- V_S is Output voltage.
- I_{out} is Maximum output current in the application.
- f_S is Converter switching frequency (typically 1.2 MHz).
- η is Estimated converter efficiency (please use the number from the efficiency plots or 90% as an estimation.

(5)

Table 3. Inductor Selection

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (L×W×H mm)	DCR TYP (mΩ)	I_{sat} (A)
3.3	Sumida	CDH38D09	4 x 4 x 1	240	1.25
4.7	Sumida	CDPH36D13	5 x 5 x 1.5	155	1.36
3.3	Sumida	CDPH4D19F	5.2 x 5.2 x 2	33	1.5
3.3	Sumida	CDRH6D12	6.7 x 6.7 x 1.5	62	2.2
4.7	Würth Elektronik	7447785004	5.9 x 6.2 x 3.3	60	2.5
5	Coilcraft	MSS7341	7.3 x 7.3 x 4.1	24	2.9

8.2.1.2.2 Rectifier Diode Selection

To achieve high efficiency a Schottky type should be used for the rectifier diode. The reverse voltage rating should be higher than the maximum output voltage of the converter. The averaged rectified forward current I_{avg} , the Schottky diode needs to be rated for, is equal to the output current I_{out} :

$$I_{avg} = I_{out}$$

(6)

Usually a Schottky diode with 1-A maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier can be selected with lower forward current capability depending on the output current I_{out} but has to be able to dissipate the power. The dissipated power, P_D , is the average rectified forward current times the diode forward voltage, $V_{forward}$.

$$P_D = I_{avg} \cdot V_{forward}$$

(7)

Typically the diode should be able to dissipate around 500 mW depending on the load current and forward voltage.

Table 4. Rectifier Diode Selection

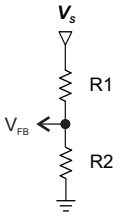
CURRENT RATING I_{avg}	V_r	$V_{forward}/I_{avg}$	SUPPLIER	COMPONENT CODE	PACKAGE TYPE
750 mA	20 V	0.425 V / 1 A	Fairchild Semiconductor	FYV0704S	SOT 23
1 A	20 V	0.39 V / 1 A	NXP	PMEG2010AEH	SOD 123
1 A	20 V	0.5 V / 1 A	Vishay Semiconductor	SS12	SMA
1 A	20 V	0.44 V / 1 A	Vishay Semiconductor	MSS1P2L	Âµ -SMP
2 A	20 V	0.44 V / 2 A	Vishay Semiconductor	SL22	SMB

8.2.1.2.3 Setting the Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of 50 µA flowing through the feedback divider gives good accuracy and noise covering. A standard low side resistor of 18 kΩ is typically selected. The resistors are then calculated as:

$$R2 = \frac{V_{FB}}{70\mu A} \approx 18k\Omega \qquad R1 = R2 \cdot \left(\frac{V_S}{V_{FB}} - 1 \right)$$

$$V_{FB} = 1.238V$$



(8)

8.2.1.2.4 Compensation (COMP)

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier.

Standard values of R_{COMP} = *16 kΩ* and C_{COMP} = *2.7 nF* will work for the majority of the applications.

Please refer to Table 5 for dedicated compensation networks giving an improved load transient response. The following equations can be used to calculate R_{COMP} and C_{COMP} :

$$R_{COMP} = \frac{110 \cdot V_{IN} \cdot V_S \cdot C_{out}}{L \cdot I_{out}} \qquad C_{COMP} = \frac{V_S \cdot C_{out}}{7.5 \cdot I_{out} \cdot R_{COMP}}$$

where

- V_{IN} is Minimum input voltage.
- V_S is Output voltage.
- C_{out} is Output capacitance.
- L is Inductor value, for example, 3.3 µH or 4.7 µH.
- I_{out} is Maximum output current in the application.

(9)

Make sure that R_{COMP} < *120 kΩ* and C_{COMP}> *820 pF*, independent of the results of the above formulas.

Table 5. Recommended Compensation Network Values at High/Low Frequency

L	V_S	V_{IN} ± 20%	R_{COMP}	C_{COMP}
3.3 µH	15 V	5 V	100 kΩ	820 pF
		3.3 V	91 kΩ	1.2 nF
	12 V	5 V	68 kΩ	820 pF
		3.3 V	68 kΩ	1.2 nF
	9 V	5 V	39 kΩ	820 pF
		3.3 V	39 kΩ	1.2 nF

Table 5 gives conservative R_{COMP} and C_{COMP} values for certain inductors, input and output voltages providing a very stable system. For a faster response time, a higher R_{COMP} value can be used to enlarge the bandwidth, as well as a slightly lower value of C_{COMP} to keep enough phase margin. These adjustments should be performed in parallel with the load transient response monitoring of TPS61086.

8.2.1.2.5 Input Capacitor Selection

For good input voltage filtering low-ESR ceramic capacitors are recommended. TPS61086 has an analog input IN. Therefore, a 1-µF bypass is highly recommended as close as possible to the IC from IN to GND.

One 10-µF ceramic input capacitors are sufficient for most of the applications. For better input voltage filtering this value can be increased. Refer to Table 6 and typical applications for input capacitor recommendation

8.2.1.2.6 Output Capacitor Selection

For best output voltage filtering a low-ESR output capacitor like ceramic capcaitor is recommended. Two to four 10-µF ceramic output capacitors (or two 22 µF) work for most of the applications. Higher capacitor values can be used to improve the load transient response. Refer to Table 6 for the selection of the output capacitor.

Table 6. Rectifier Input and Output Capacitor Selection

	CAPACITOR/SIZE	VOLTAGE RATING	SUPPLIER	COMPONENT CODE
C_{IN}	22 µF/1206	16 V	Taiyo Yuden	EMK316 BJ 226ML
IN bypass	1 µF/0603	16 V	Taiyo Yuden	EMK107 BJ 105KA
C_{OUT}	10 µF/1206	25 V	Taiyo Yuden	TMK316 BJ 106KL

To calculate the output voltage ripple, the following equation can be used:

$$\Delta V_C = \frac{V_S - V_{IN}}{V_S \cdot f_S} \cdot \frac{I_{out}}{C_{out}} \qquad \Delta V_{C\_ESR} = I_{L(peak)} \cdot R_{C\_ESR}$$

where

- ΔV_C is Output voltage ripple dependent on output capacitance,output current and switching frequency.
- V_S is Output voltage.
- V_{IN} is Minimum input voltage of boost converter.
- f_S is Converter switching frequency (typically 1.2 MHz).
- I_{out} is Output capacitance.
- ΔV_{C_ESR} is Output voltage ripple due to output capacitors ESR (equivalent series resistance).
- I_{SWPEAK} is Inductor peak switch current in the application.
- R_{C_ESR} is Output capacitors equivalent series resistance (ESR). (10)

ΔV_{C_ESR} can be neglected in many cases since ceramic capacitors provide very low ESR.

8.2.1.3 Application Curves

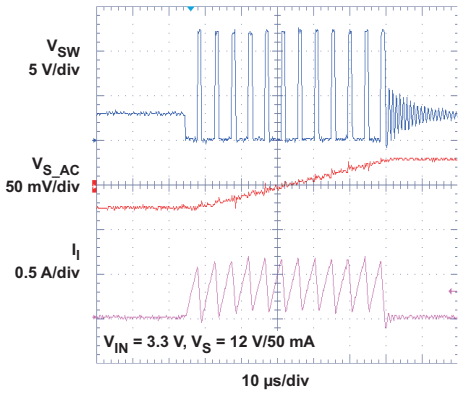


Figure 8. PFM Mode Switching Pulse

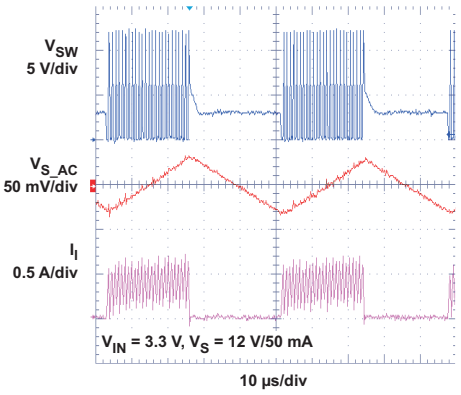


Figure 9. PFM Mode Switching Pulses

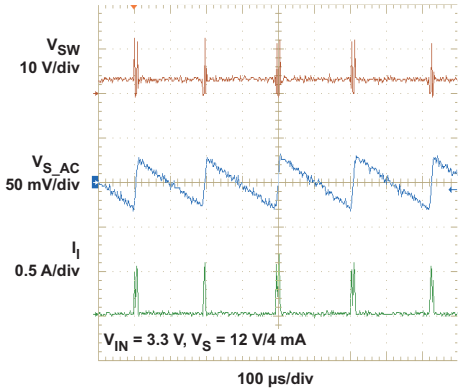


Figure 10. PFM Mode - Light Load

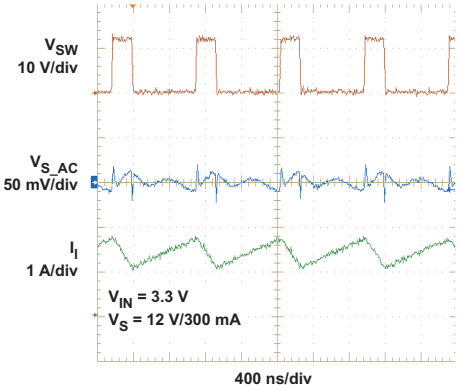


Figure 11. Forced PWM / PFM Mode - Heavy Load

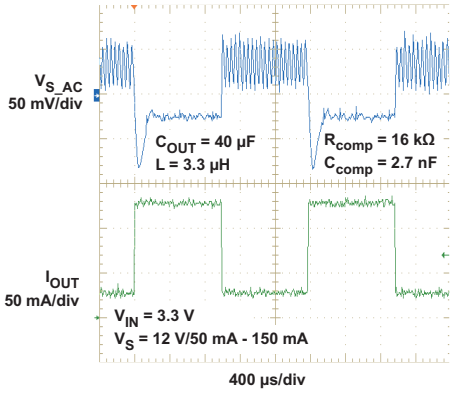


Figure 12. Load Transient Response PFM Mode

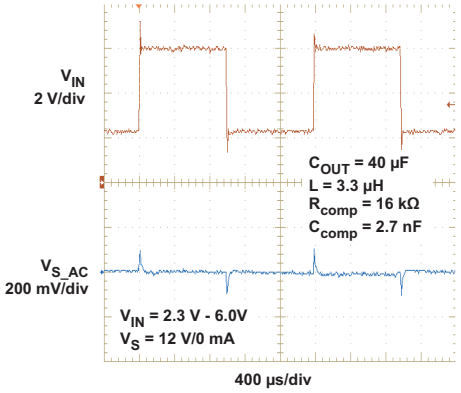


Figure 13. Line Transient Response Light Load

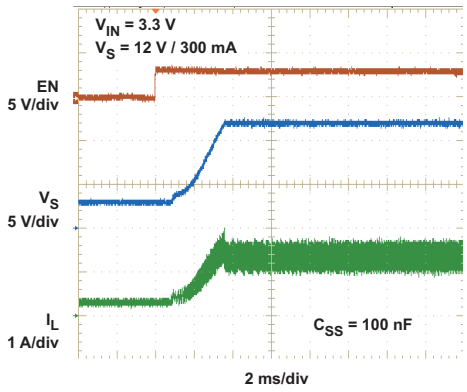


Figure 14. Soft-Start

8.2.2 3.3-V to 12-V Boost Converter With Forced PWM Mode at Light Load

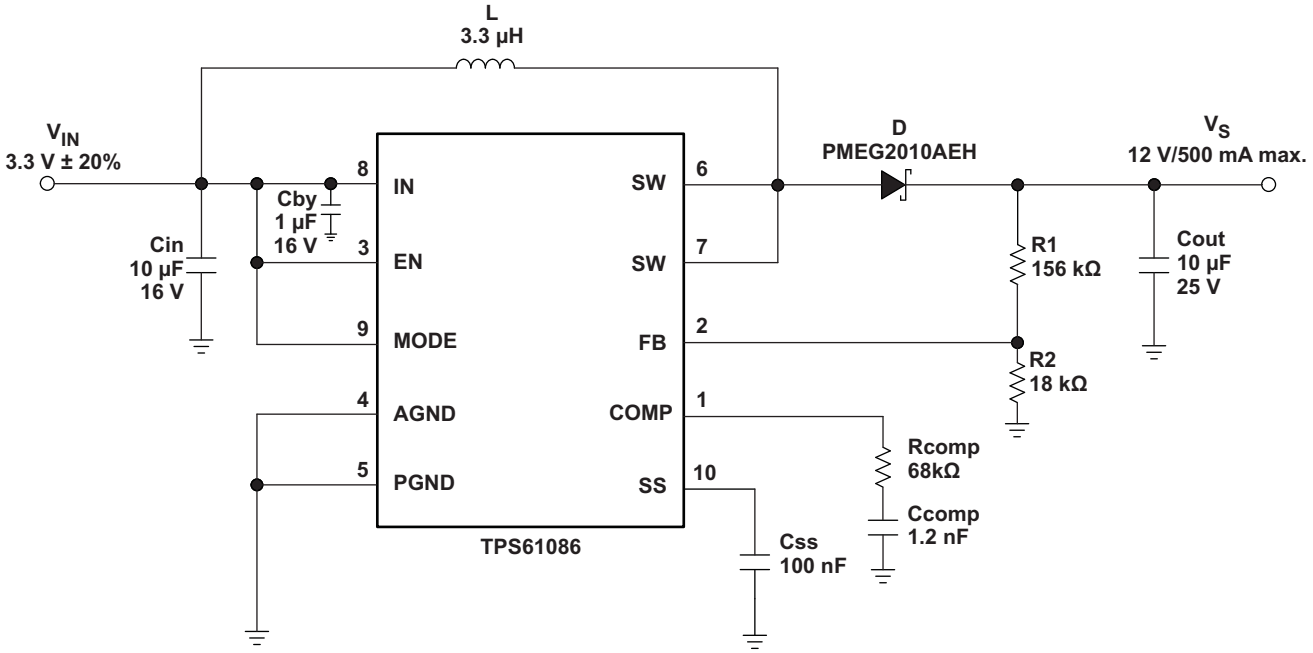


Figure 15. Typical Application, 3.3 V to 12 V (Force PWM Mode)

8.2.2.1 Design Requirements

For this example, the design parameters are listed in Table 7.

Table 7. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage	3.3 V ± 20%
Output Voltage	12 V
Output Current	500 mA
Operation Mode at Light Load	Forced PWM

8.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* in the *3.3-V to 12-V Boost Converter With PFM Mode at Light Load* section.

8.2.2.3 Application Curves

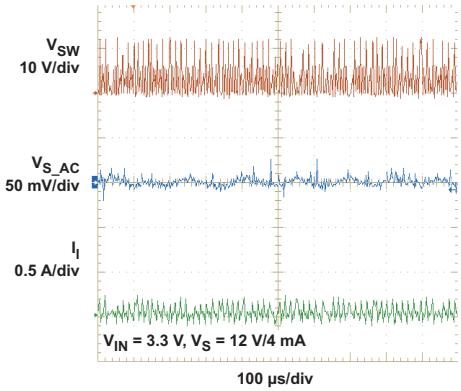


Figure 16. Forced PWM Mode - Light Load

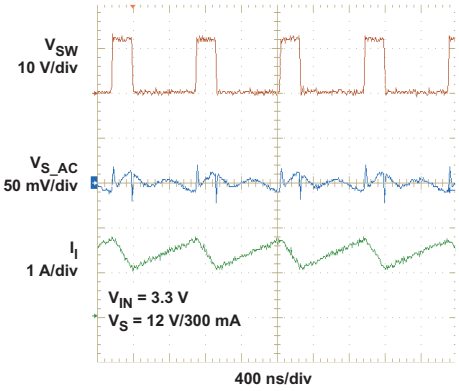


Figure 17. Forced PWM / PFM Mode - Heavy Load

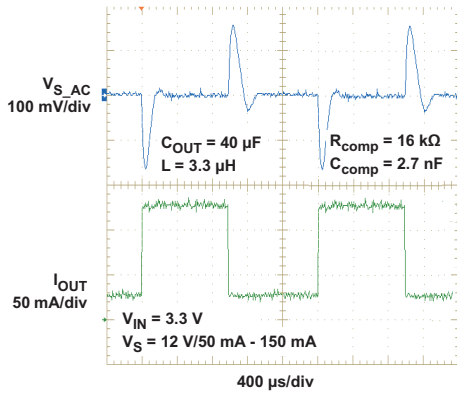


Figure 18. Load Transient Response Force PWM Mode

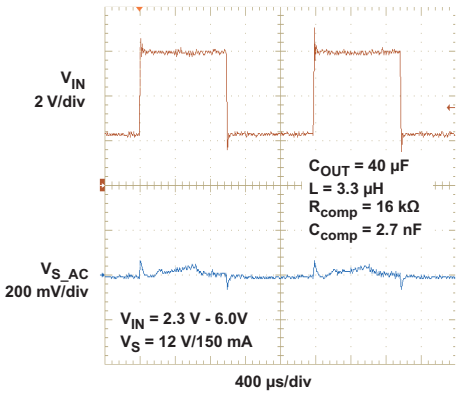


Figure 19. Line Transient Response Heavy Load

8.3 System Examples

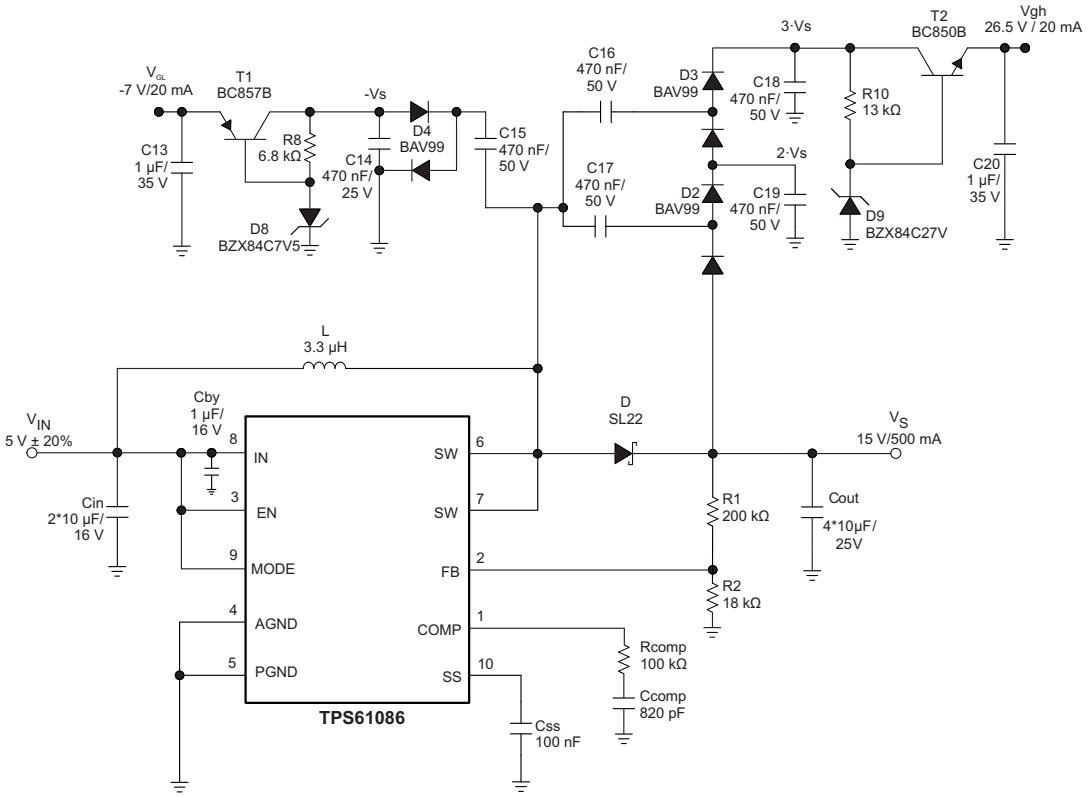


Figure 20. Typical Application 5 V to 15 V (Force PWM Mode) for TFT LCD With External Charge Pumps (VGH, VGL)

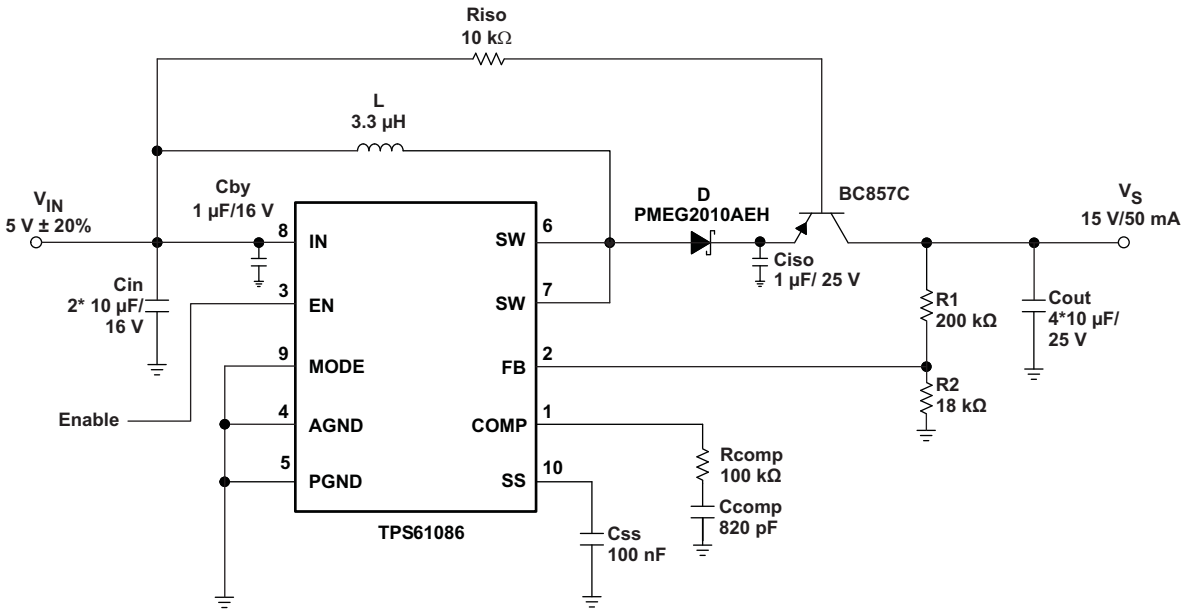


Figure 21. Typical Application With External Load Disconnect Switch

System Examples (continued)

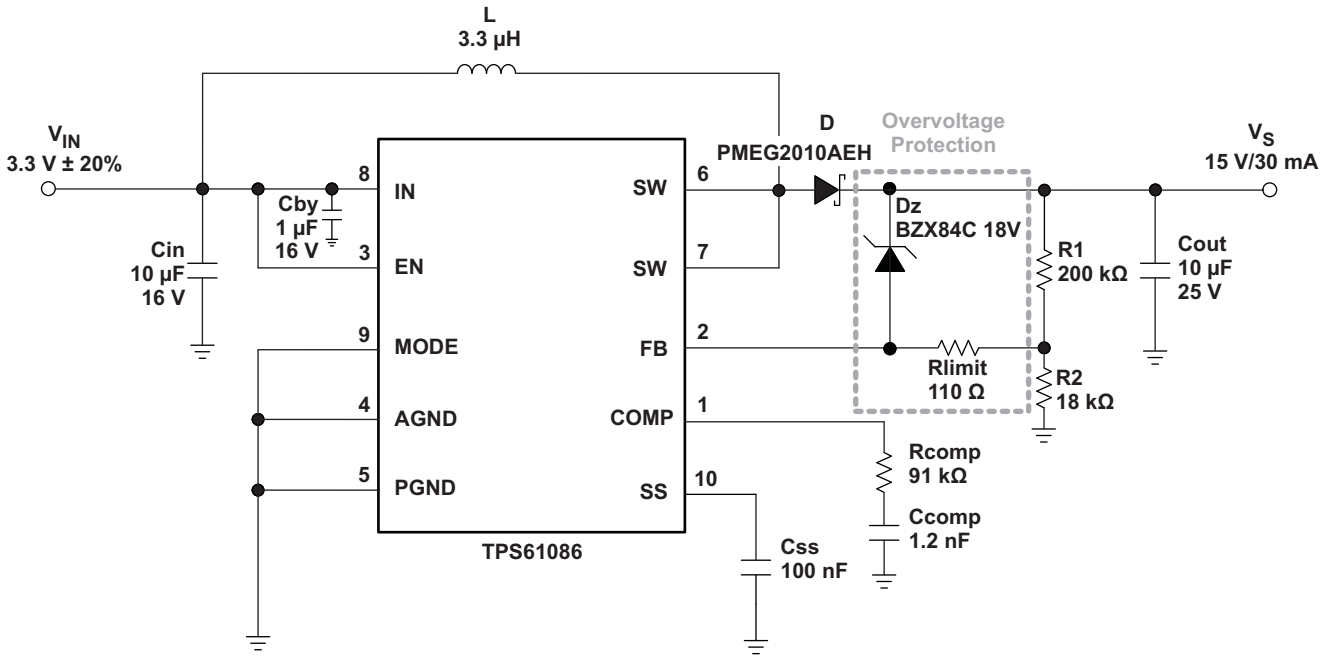


Figure 22. Typical Application, 3.3 V to 15 V (PFM Mode) With Overvoltage Protection

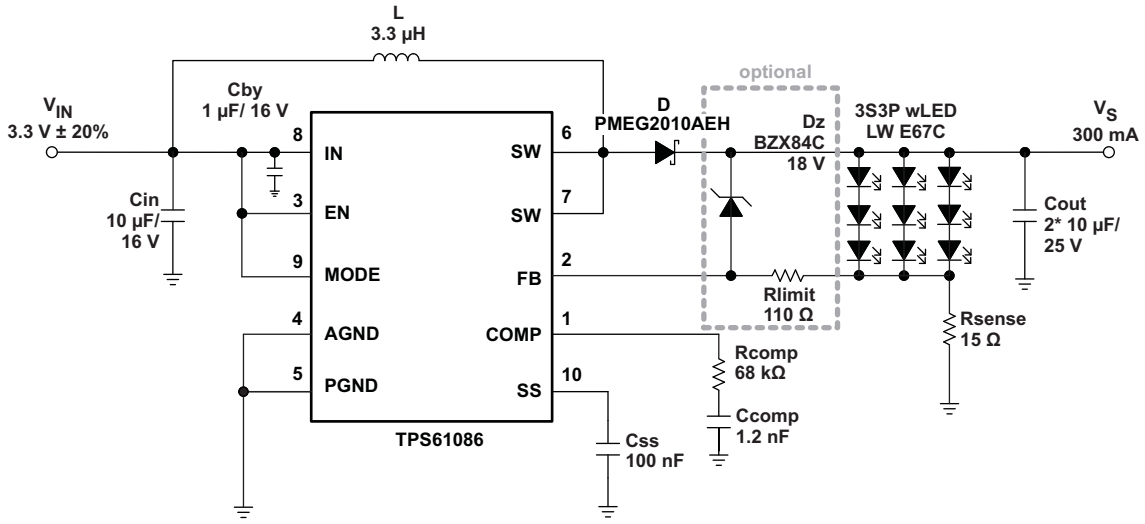


Figure 23. Simple Application (3.3-V Input Voltage - Forced PWM Mode) for wLED Supply (3S3P) (With Optional Clamping Zener Diode)

System Examples (continued)

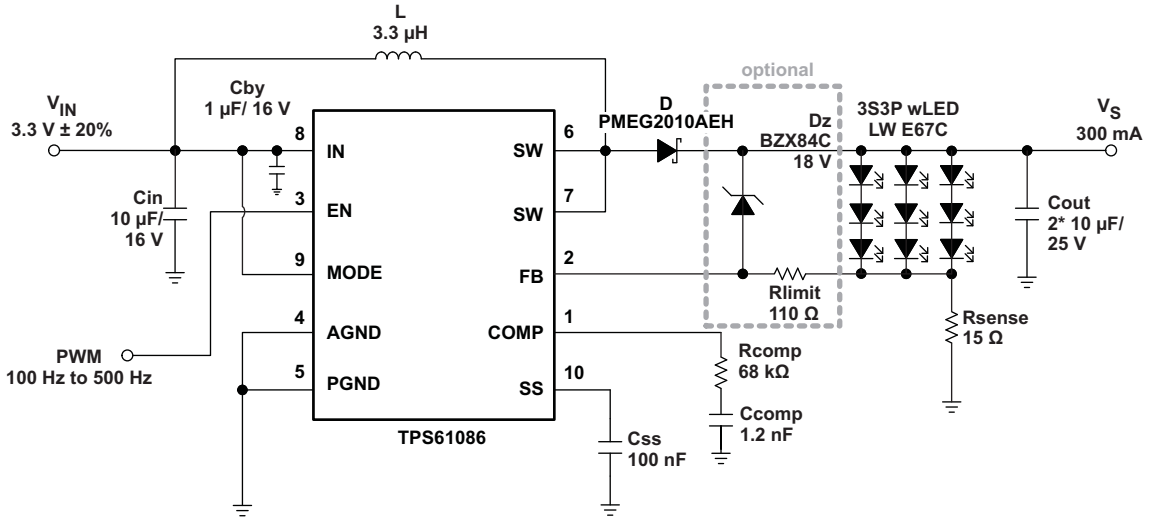


Figure 24. Simple Application (3.3-V Input Voltage - Forced PWM Mode) for wLED Supply (3S3P) With Adjustable Brightness Control Using a PWM Signal on the Enable Pin (With Optional Clamping Zener Diode)

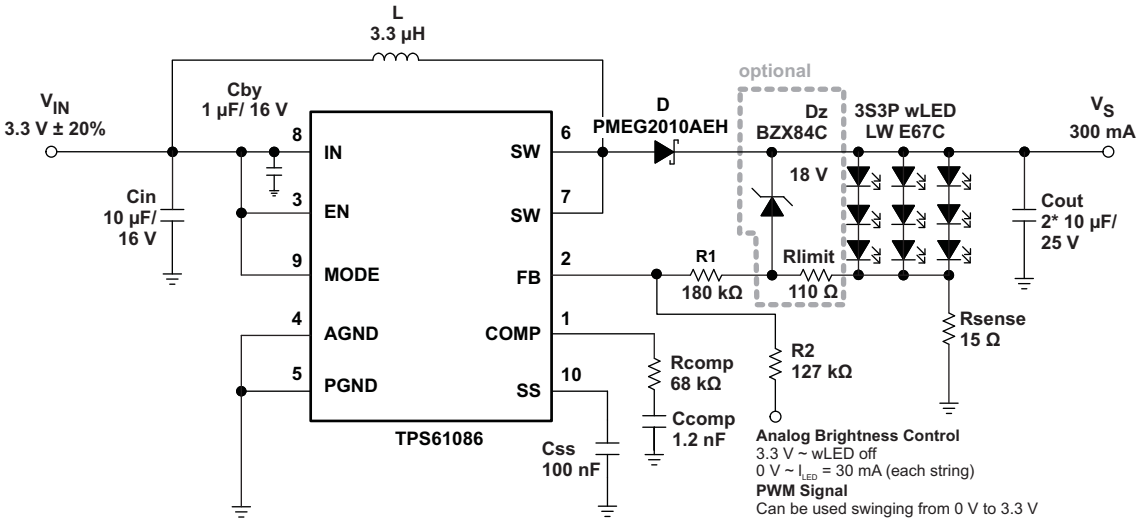


Figure 25. Simple Application (3.3-V Input Voltage - Forced PWM Mode) for wLED Supply (3S3P) With Adjustable Brightness Control Using an Analog Signal on the Feedback Pin (With Optional Clamping Zener Diode)

9 Power Supply Recommendations

The TPS61086 is designed to operate from an input voltage supply range between 2.3 V and 6.0 V. The power supply to the TPS61086 needs to have a current rating according to the supply voltage, output voltage, and output current of the TPS61086.

10 Layout

10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground connecting to the PGND terminal and a different one for control ground connecting to the AGND terminal to minimize the effects of ground noise. Connect these ground nodes at the PGND terminal of the IC. The most critical current path for all boost converters is from the switching FET, through the rectifier diode, then the output capacitors, and back to ground of the switching FET. Therefore, the output capacitors and their traces should be placed on the same board layer as the IC and as close as possible between the IC's SW and PGND terminal.

10.2 Layout Example

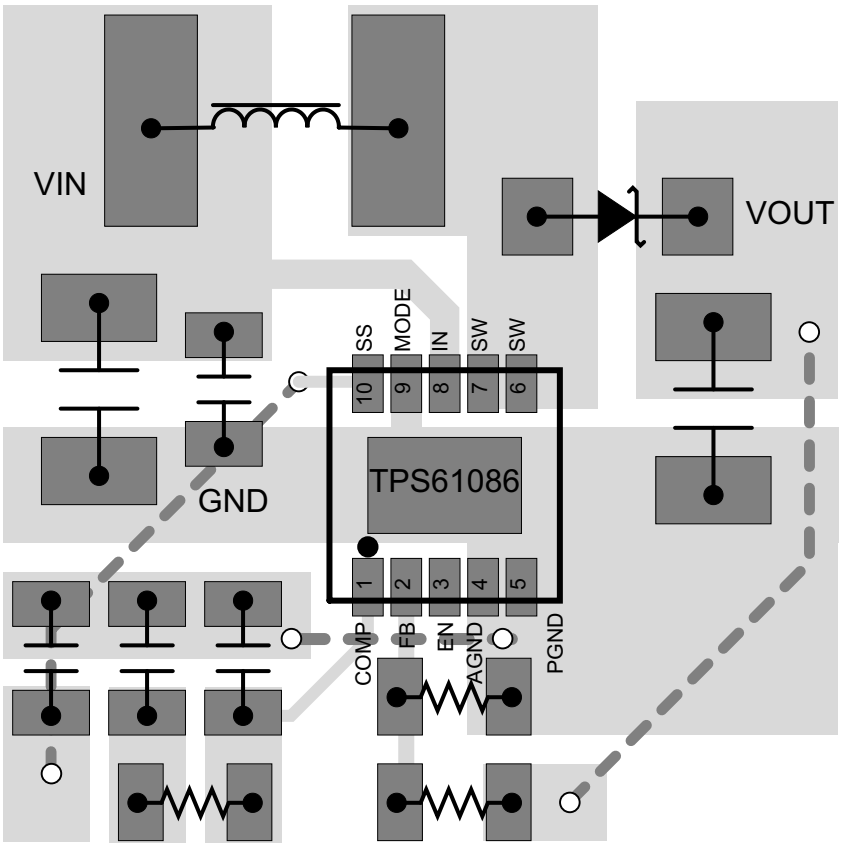


Figure 26. TPS61086 Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61086DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PSRI	Samples
TPS61086DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PSRI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

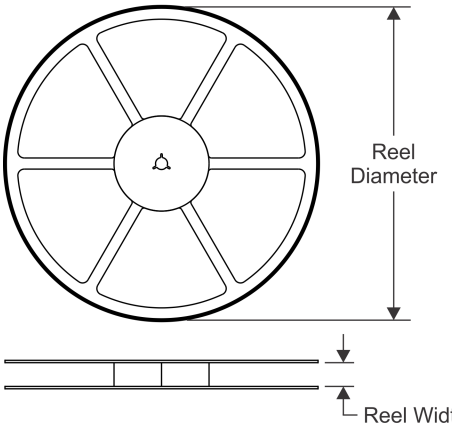
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

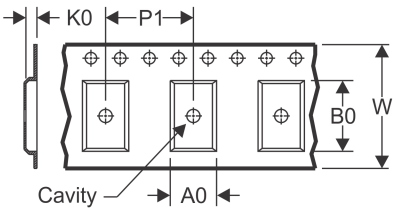
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

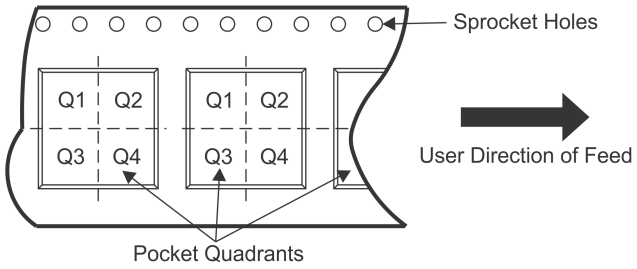


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

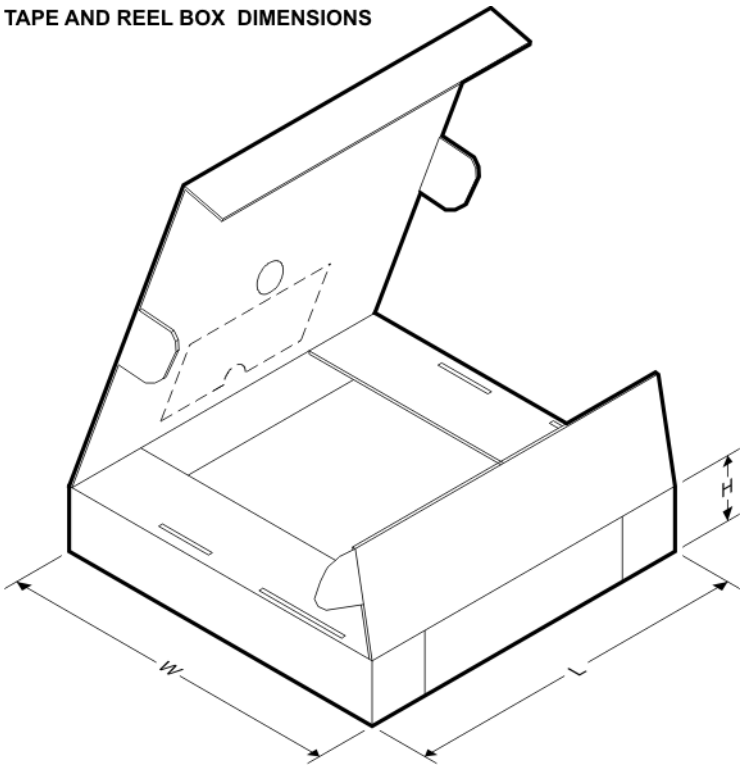
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61086DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61086DRCT	VSON	DRC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61086DRCR	VSON	DRC	10	3000	338.0	355.0	50.0
TPS61086DRCT	VSON	DRC	10	250	205.0	200.0	33.0

GENERIC PACKAGE VIEW

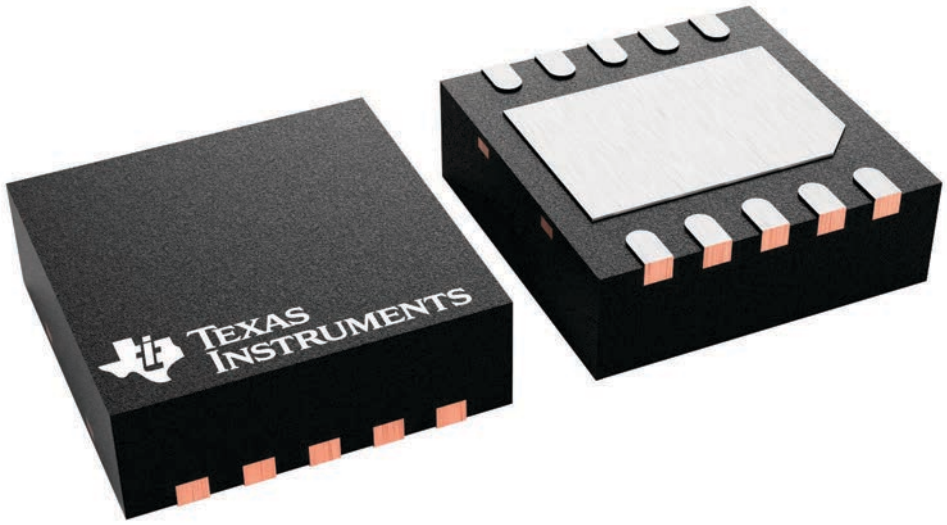
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



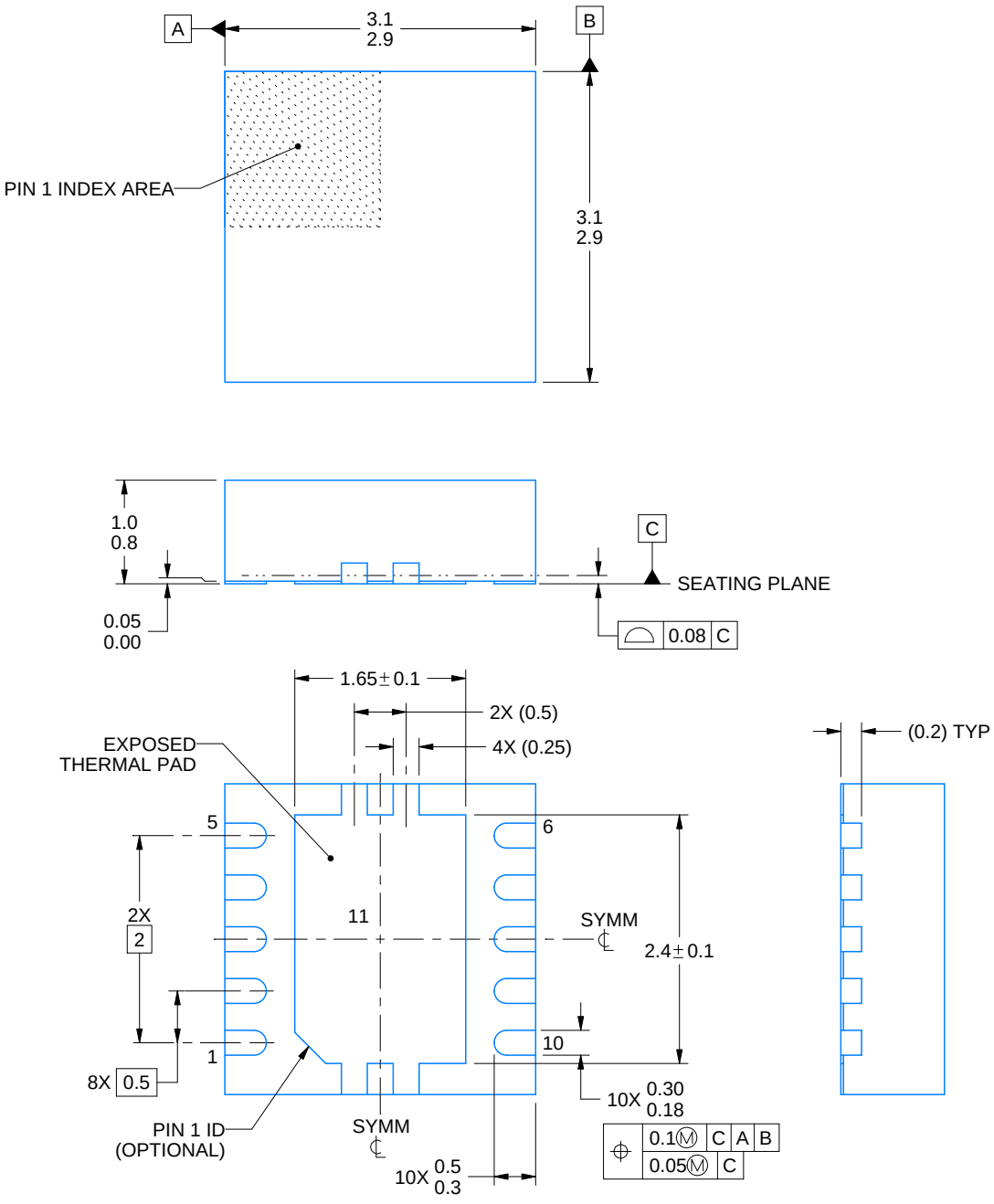
4226193/A

DRC0010J

PACKAGE OUTLINE

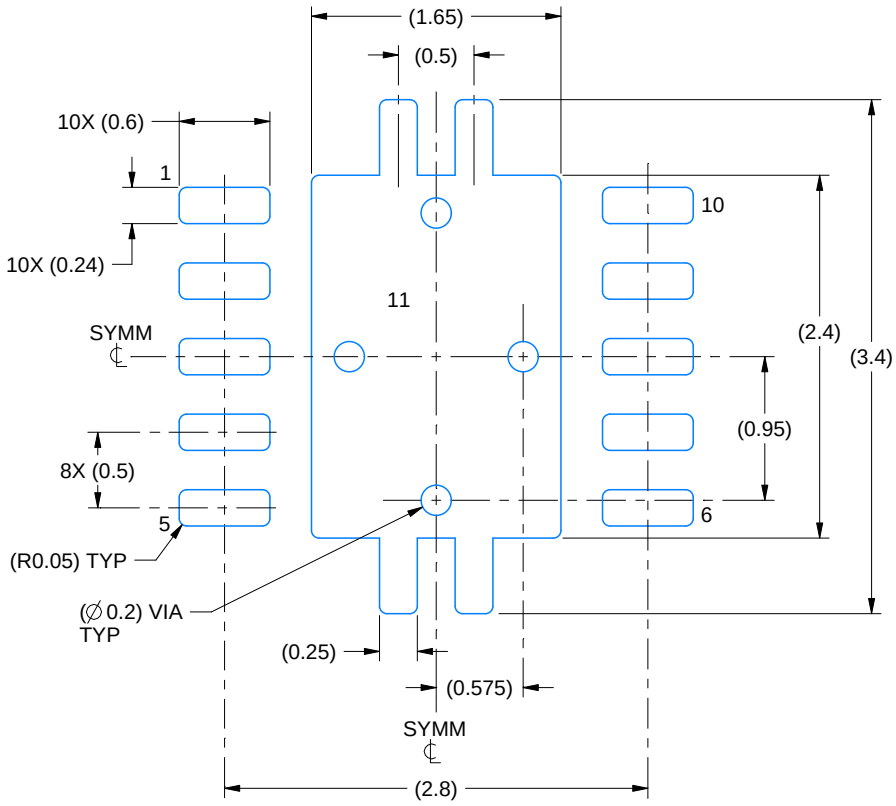
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

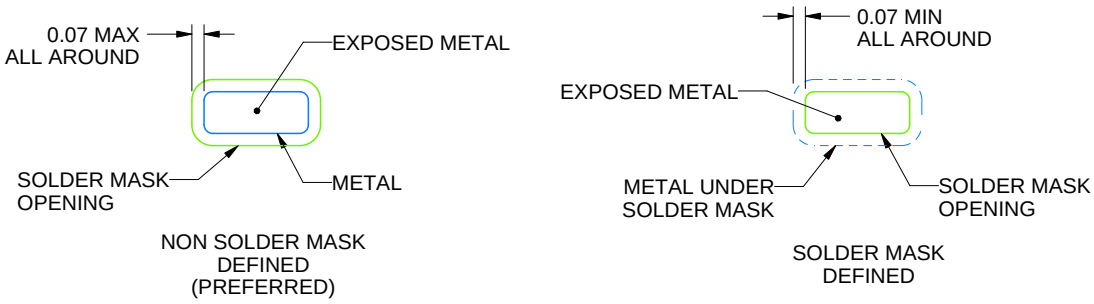


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

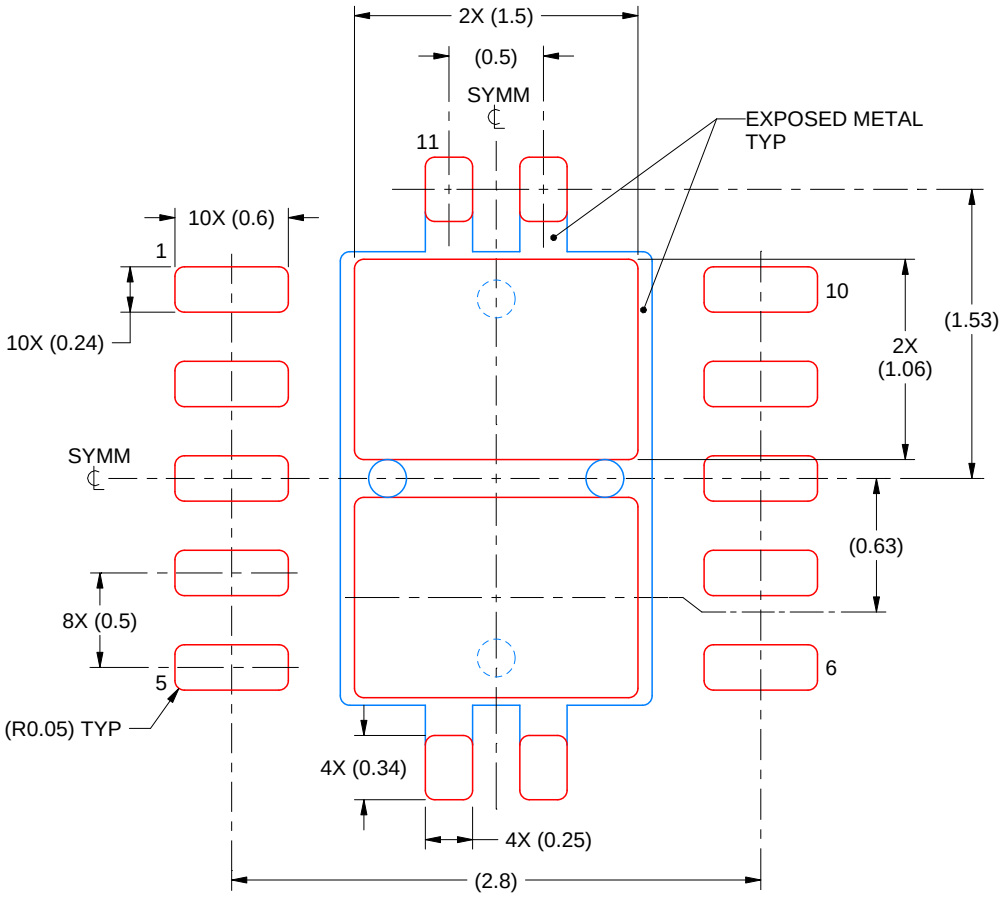
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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