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Migrating from the 71M6513 to the 71M6533/6534

The TERIDIAN Semiconductor family of metering chips has recently been expanded by adding two new members, the 71M6533 and the 71M6534, which are powerful alternatives for implementing poly-phase metering applications. This Application Note explains the considerations that apply when migrating firmware from the 71M6513 to the 71M6533 and how designs based on the 71M6513 can be adapted to both the 71M6533 and the 71M6534.

Hardware details are intentionally omitted when they are described in the preliminary datasheet (PDS).

Similarities in Tools, Firmware and I/O

The CPU and its emulator interface are compatible, permitting the same compiler (Keil Cx51, version 7.2 or later) and debugger (Signum Systems ADM51 3.11.05 or later) to be used for both the 71M6513 and 71M653X.

The serial I/O, timers and the digital I/O are also compatible. Crucially, the metering outputs are organized and controlled by similar configuration structures. The standard 71M653X CE code uses the same conversion constants as the 71M6513.

However, versions of 71M653X-series CE code that measures neutral current have a different sample frequency (2184Hz), and different conversion constants, as compared to the CE codes of the 71M6513.

CE code that works in the 71M6533 will also work in the 71M6534 and vice-versa. MPU code for the 71M6533 requires minor modifications to run in a 71M6534, mostly correct assignment of pins and LCD outputs.

Since a 71M6534 has 256 KB of flash memory, not all firmware for a 71M6534 can fit or work in a 71M6533.

Trace Feature

The 71M6534 implements a trace system for use by the emulator, similar to the 71M6513. The trace logic permits real-time trace of execution, and can log read and write operations. The complex trace version of the ADM51 has programmable logic to select trace data in real time. TSC recommends to use trace emulators when possible and uses them in internal development.

The trace feature is not available on the 71M6533.

Differences in Firmware and I/O

LCD Segment and Pin Assignment

Although the pins of the 71M6533 have similar functions when compared with the 71M6513, the 71M6533 has a more flexible pin assignment system. The rather coarse general division between LCD pins and DIO pins in the 71M6513, controlled by *LCD_NUM*, has been dropped in the 71M6533, where most pins with multiple uses can be individually controlled. This unavoidably causes some incompatibility with 71M6513 firmware.

In some cases, configuration and data bits for DIOs are placed directly in the LCD output buffer. In the 71M6513, the code could blank the LCD by simply writing zeros to all LCD segment registers. In the 71M6533, the code must not write to segment data for pins that have been configured as DIOs. Most firmware that uses the LCD has tables to select valid segments. The clearing function can step through these tables.

Another difference is that many bytes of the LCD segment data control up to eight segments.

Memory Paging

The 71M6533 has 128 KB flash memory controlled by the page register *FL_BANK[1:0]*. The 71M6534 has 256 KB controlled by the page register *FL_BANK[2:0]*. The page register *FL_BANK[2:0]* selects the 32KB page that replaces the upper 32K of the MPU's code space. When the page register is set to 1 (the hardware default), the chip behaves much like a 71M6513 with 64KB of flash memory.

The Software User Guide (SUG) for the 71M653X contains detailed suggestions for utilizing the bank-switching hardware. The demo code has a ported version of Keil's bank-switching code and some helpful utilities.

RAM

The 71M653X has 4 KB of RAM. This is twice the RAM of the 71M6513's MPU, but this extra RAM is shared between the CE (the compute-engine), and the MPU (the 80515).

The RAM of the CE is assigned to a range from 0 to *MAX_CE*, where *MAX_CE* is the maximum address used by the CE code. This address varies depending on the exact implementation of CE code. The MPU should not use those addresses for general-purpose data storage, because if active, the CE overwrites the data.

A helpful improvement over the 71M6513 is that the RAM used by the CE is now fully accessible to both the CE and the MPU. In earlier TERIDIAN metering chips, special code had to assure the timing of the read and write operations to CE RAM. This code is no longer needed because CE RAM and MPU RAM are located in the same physical RAM. Likewise, in earlier TERIDIAN demo code, the XFER_BUSY interrupt had to copy data from the

CE DRAM to a stable, accessible copy in MPU RAM. That copy operation is no longer necessary, provided the CE data is accessed by the MPU only while it is stable.

Just as in the 71M6513, the CE output data of the 71M653X periodically changes once per accumulation interval, and generates a XFER_BUSY request. The CE output data begins changing about 400µs before this request, and is unstable until the XFER_BUSY request occurs. The MPU must take care not to access the CE outputs during the time that these are unstable.

I/O RAM Map

Many fields in the I/O RAM (Configuration RAM) are similar between the 71M6513 and 71M653X. In all common meter configurations, the 71M653X has settings functionally identical or superior to earlier TERIDIAN meter ICs. The 71M653X provides equivalent or superior meter operation. However, the actual RAM addresses and bits are often different.

The best porting scheme is to use C variable names and named bit field values, and then reassign the variable addresses and bit field values with different include files. These can be included from a file with an identical name, such as “options.h” so that options.h can be included by many files without changing the portable code.

TERIDIAN’s Demo Code provides these portability files. For the 71M6513 the files are named as follows:

- 80515.h
- io651x.h and .c
- ce651x.h and .c
- reg651x,h and .c.

For the 71M653X, the portability files are named as follows:

- 80515.h,
- io653x.h and .c,
- ce653x.h and .c
- reg653x,h and .c.

Similar files are also available for porting to and from 71M6523 and other ICs, if needed. All files are stable and tested.

Dual Data Pointer Use

The 80515 used in TSC meter ICs has two data pointers. In version 8 of its compiler package Cx51, Keil added a library to support Evatronix-compatible 8051 MPUs with dual data pointers. With the library option enabled, string copies run about twice as fast.

Interrupts

The interrupts are similar between the 71M6513 and 71M6533, but not identical. The timer and UART interrupts are inside the 80515 logic, so they are unchanged.

Software timer logic can use the 71M6533’s new *SUBSEC* register as a time base. This can free the interrupting timers for other uses. *SUBSEC* also keeps the same rate in battery modes with slower clock rates.

The housekeeping handled by the per-sample CE_BUSY MPU interrupt has been automated in the 71M653X, reducing the real-time burden on the MPU.

The external interrupts are somewhat different, and the differences are shown in Table 1.

Table 1: Interrupts

Event	71M6513	71M6533/4	Comments
Digital I/O, high priority	int0	int0	DIO selected with *DIO_R[]*
Digital I/O, low priority	int1	int1	DIO selected with *DIO_R[]*
Mains power failure	Not available	int0,int1, timer0, timer1	In the 71M653X series, the CE generates a pulse on YPULSE to warn of a mains power failure. *DIO_R[]* can be programmed to interrupt on YPULSE. Timers in gate mode, with a maximum count can also interrupt on YPULSE [1].
Write to flash while CE is enabled (*FWCOL0*, *FWCOL1*)	Not available	int2	In the 71M653X series, the CE runs directly from flash, so flash cannot be written while the CE is operating.
Comparator 2 or 3	int2, int4	Not available	When used at all, many customers used these to detect an imminent switch to battery power. The 71M653X series substituted a single comparator, intended to detect the switch to battery power.
Power supply comparator 1 (*PLL_OK*)	Not available.	int4	Detects change to battery power.
end of sample processing (CE_BUSY)	int3	int3	Less used in the 71M653X series. The 71M653X CE codes generate a power failure warning pulse on YPULSE. The 71M653Xs automatically set *ALT_MUX* and the chop of the ADCs' voltage reference.
EEPROM data transfer done (EEPROM_BUSY)	int5	int5	Unchanged.
end of accumulation interval (XFER_BUSYZ	int6	int6	The 71M653X series fixes an issue that caused the interrupts sharing this interrupt to interfere.
one second clock tick (*RTC_1_SEC*)	int6	int6	Shared with XFER_BUSY.
watchdog warning (NEAR_OVERFLOW)	not available	int6	New feature, shared with XFER_BUSY. A software watchdog reset is about to occur.

[1] "Timers in gate mode: If int0 and int1 are already in use, (e.g., for counting pulses), a spare timer can become an external interrupt. Timers have a "gate mode" to count external events. The firmware can set the count to the maximum value, just before the counter will turn over. The next pulse on the gate causes the counter overflow to zero, and the timers generates an interrupt.
In the 71M6521 and 71M653X demo codes, timer 1 is spare, and the timer gates can be selected for DIO pins 0 to 11, using the *DIO_R[]* registers in I/O RAM.

Differences in CE Code

CE Set-up and Use

TERIDIAN's 71M6533/6534 CE code uses set-up and algorithms similar to those used in the 71M6513. The intent is to keep the same functionality and scaling for the configuration parameters and outputs.

In the 71M6533/6534, the MPU address of a CE variable is 4*(CE address), whereas in the 71M6513, it is 0x1000 + 4*(CE address).

The 71M653X-series CEs have four pulse outputs. A new feature is that when a power failure is detected, most CE codes pulse the fourth pulse output, YPULSE. The MPU can therefore use the *DIO_R[]* registers in I/O RAM to program an external interrupt to detect imminent power failure. That way, it is no longer necessary to continually test the sag bits in the CE's status word.

The third pulse output can be programmed to output VAh, or, on some CE codes, F0, the mains frequency.

In standard CE code, it is possible to program the four pulses to simulate two sets of KYZ outputs, the legacy-standard four-quadrant pulse output. One disables the power failure pulse, sets the pulse width to maximum, to get 50% pulses, and then set pairs of pulse accumulators 90 degrees apart (e.g. WSUM_ACCUM = 0x20000000 and PULSE2_ACCUM=0x60000000). The MPU can drive one pair of pulses from Wh and the other from VARh. Firmware should periodically adjust the secondary ACCUM registers to maintain the 90-degree offset.

In addition, the ADC of the 71M653X writes to different addresses, which means that the variable map of the CE has to change. The CE memory of the 71M653X begins at XDATA RAM address 0 (rather than 0x1000, as in the 71M6513). Also, output variables will begin on a separate 256-byte PDATA page, at 0x0200, while the configuration data will begin at 0x0040. The CE code of the 71M653X also concentrates the CE's configuration data in the beginning of the CE's RAM area, while the remainder of the RAM can be set to zero.

Furthermore, the FIR length and some other values of the CE set-up have compatible selections, but not identical values. For the software engineer it is important to select values that provide identical behavior.

CE code that measures neutral uses a *MUX_DIV* value of 7, rather than 6, and uses the extra ADC slot to measure the neutral current. This changes the sample frequency from 2520.6 Hz to 2184.5 Hz. Therefore, the constants to convert to standard units differ for the neutral measurement code. Unlike the 71M6513, no special manipulation of *ALT_MUX* is needed, and the accuracy of the neutral measurement is the same as the accuracy of other current channels. See the data sheets and application notes pertaining to CE codes for further information.

Compared to the 71M6513, some additional set-up steps are required, as follows:

The ADC slot timing has to be set-up (using I/O RAM registers 0x2090..209A). The general strategy is to keep the voltage measurement (V_n) adjacent in time to the current (I_n) measurement for the same element. Alternate multiplexer cycles change a few selected samples once in an accumulation interval. In the 71M6533, the MPU programming can control these alternate multiplexer cycles. The recommended alternate cycles are to replace the current measurements, which vary less, with the alternate battery voltage and temperature measurements. For this sample frame, the CE code uses the previous current sample for the current samples that are omitted. As in the 71M6513, the error generated by this interpolation is not measurable, and is intentionally desynchronized from the line cycle.

As of December, 2008, a number of 71M653X-series CE codes exist, with different properties. These codes are listed in Table 2.

Table 2: 71M653X CE Codes

Name	Supported Equations	Power fail sense?	Temperature compensation by	Comments
ce31a01	2	poll	MPU	First 6531 CE code, used to characterize the IC. FM pulses. Single-ended current measurement.
ce31a02	0, 1	poll	MPU	FM pulses. Single-ended current measurement.
ce31a03	1, 3	interrupt	CE or MPU	FM pulses. Single-ended current measurement.
ce31a04	0	interrupt	CE or MPU	FM pulses. Single-ended current measurement.
ce31a05	1, 2	interrupt	CE or MPU	FM pulses. Single-ended current measurement. Multiple sag thresholds with hysteresis.
ce31a06	0	interrupt	CE or MPU	Real-time pulses. Single-ended current measurement.
ce34a01	5	poll	MPU	First 6533 and 6533 CE code, used to characterize the ICs. FM pulses. Single-ended current measurement.
ce34a02	5	interrupt	CE or MPU	FM pulses. Differential current measurement.
ce34a03	5	interrupt	CE or MPU	Rogowski coil current sensor. FM pulses. Differential current measurement. Requires CE clock to be 10MHz (Set M40MHZ and CE10MHZ).
ce34a05	5	interrupt	CE or MPU	Real-time or FM pulses. Differential current measurement.
ce34a06	5	interrupt	CE or MPU	Measures neutral current. Sample frequency is 2184 Hz. FM pulses. Differential current measurement.

The terms used in Table 2 are explained below:

- Equation 0..5 are as described in the data sheets.
- "poll" means that the MPU must rapidly read the "sag" bits in the CE status to detect power failure. This is often done in the MPU's per-sample interrupt, CE_BUSY.
- "interrupt" means that the CE will pulse YPULSE to indicate imminent power failure. *DIO_R[]* can be set to interrupt the MPU from the CE's YPULSE output. CE_BUSY can be disabled, saving substantial CPU time in the MPU.
- "MPU" means that the MPU must calculate and set *GAIN_ADJ* to absorb metering error caused by temperature.
- "CE or MPU" means that the CE has *PPMC* and *PPMC2* variables, and can be configured to calculate and set GAIN_ADJ to absorb metering error caused by temperature.
- "FM pulses": Each accumulation interval, the number of watt-hours for that accumulation interval is used to set the pulse rate for the next accumulation interval. The MPU performs creep logic. This method is economical of CE code space and permits sophisticated custom creep logic.
- "Real-time pulses" The CE performs creep logic and immediately integrates the watt-hours into the pulse accumulator. These code versions are less popular than FM pulses because the creep logic is less flexible.
- "Single-ended current measurement" Some 71M653X-series ICs can be programmed so current inputs are either single-ended or differential. Single-ended measurement is subject to ripple noise, but works well with simpler, less expensive meters.
- "Differential current measurement" is available on some 71M653X-series ICs and has lower noise floors because common-mode noise is eliminated. In some cases, the sensors must be more expensive to make use of the superior noise margin.

CE Address Map

The CE codes for the 71M6513 and 71M653X have similar features, but many details are different. The address for *MAX_CE* is typically less than CE address 0x140, MPU 0x500, the maximum address in Table 3.

Table 3: CE Addresses

Name	71M6513 CE Address	71M6533 CE Address	Purpose
Inputs			
CAL_IA	0x08	0x10	Current gain, element A
CAL_VA	0x09	0x11	Voltage gain, element A
CAL_IB	0x0A	0x12	Current gain, element B
CAL_VB	0x0B	0x13	Voltage gain, element B
CAL_IC	0x0C	0x14	Current gain, element C
CAL_VC	0x0D	0x15	Voltage gain, element C
CAL_ID	Not used	0x16	Current gain, neutral element (D), if present.
CAL_V3	0x65	Not used	Current gain, neutral element, if present (measured w/ V3 auxiliary pin of the 71M6513)
PHADJ_A	0x0E	0x18	Phase adjust, element A
PHADJ_B	0x0F	0x19	Phase adjust, element B
PHADJ_C	0x10	0x1A	Phase adjust, element C
PHADJ_D	none	0x1B	Phase adjust, element D, or spare
TEMP_NOM	0x11	0x1F	Temperature calibration.

Name	71M6513 CE Address	71M6533 CE Address	Purpose
APULSEW	0x26	0x41	Pulse input, Wh pulse
APULSER	0x27	0x42	Pulse input, VARh pulse
APULSE2	none, new feature	0x43	Pulse input, third pulse output (optional)
APULSE3	none, new feature	0x44	Pulse input, fourth pulse output (optional)
PULSE_SLOW	0x28	none, see *CESTATE*	Provided by bits in *CESTATE*
PULSE_FAST	0x29	none, see *CESTATE*	"
I0_SHUNT	0x2A	none, see *CESTATE*	"
I1_SHUNT	0x2B	none, see *CESTATE*	"
I2_SHUNT	0x2C	none, see *CESTATE*	"
CESTATE	none, see *FREQSEL, etc.*	0x20	Bit: 15..8: sag count Bit 6,7: *FREQSEL* Bit 5: *EXT_PULSE* Bit 3: *I1_SHUNT* Bit 2: *I0_SHUNT* Bit 1: *PULSE_FAST* Bit 0: *PULSE_SLOW*
WRATE	0x2D	0x21	Watt-rate for pulsing.
GAIN_ADJ	0x2E	0x40	Master temperature gain, used to adjust all metering elements simultaneously.
QUANT_W	0x2F	none, see *QUANT_WA* … *QUANT_WC*	Offset for all Wh measurements. Replaced by quant-watt values for each metering element.
QUANT_WA	none	0x26	Offset for Wh, element A
QUANT_WB	none	0x27	Offset for Wh, element B
QUANT_WC	none	0x28	Offset for Wh, element C
DEGSCALE	0x30	0x39	Scale for temperature measurement.
SAG_THR	0x31	0x24	Sag threshold
SAG_CNT	0x32	none, see *CESTATE*	Count of samples before reporting power failure. Replaced by a bit field in *CESTATE*.
FREQSEL	0x33	none, see *CESTATE*	Selection of voltage channel to use for frequency measurement. Replaced by a bit field in *CESTATE.*

Name	71M6513 CE Address	71M6533 CE Address	Purpose
QUANT_VAR	0x34	none, see *QUANT_VARA*… *QUANT_VARC*	Replaced by offsets for each metering element.
QUANT_VARA	none, see *QUANT_VAR*	0x2A	Offset for VARh, element A
QUANT_VARB	none, see *QUANT_VAR*	0x2B	Offset for VARh, element B
QUANT_VARC	none, see *QUANT_VAR*	0x2C	Offset for VARh, element C
QUANT_I	0x35	none, see *QUANT_IA*, *IB*, *VA* and *VB*	Offset for current and voltage, all elements
QUANT_IA	none, see *QUANT_I*	0x2E	Offset for current, element A
QUANT_IB	none, see *QUANT_I*	0x2F	Offset for current, element B
QUANT_IC	none, see *QUANT_I*	0x30	Offset for current, element C
QUANT_ID	none, see *QUANT_I*	0x31	Offset for current, element D (neutral)
SUMPRE	0x36	0x23	Samples per accumulation interval.
EXT_PULSE	0x37	none, See *CESTATE*	15=pulse generators read external values for the pulse rate.
EXT_TEMP	0x38	none, See *CESTATE*	15= *GAIN_ADJ* must be written by the MPU.
PPMC	0x39	0x3A	First order linear temperature compensation.
PPMC2	0x3A	0x3B	Second order quadratic temperature compensation.
KVAR	0x3B	0x22	VAR Scale factor
PULSEWIDTH	0x3C	0x38	Adjusts pulsewidth
WSUM_ACCUM	0x3D	0x45	Pulse accumulator for watt-hours.
VSUM_ACCUM	0x3E	0x46	Pulse accumulator for var-hours.
SUM2_ACCUM	none, new feature	0x47	Pulse accumulator for pulse 3.
SUM3_ACCUM	none, new feature	0x48	Pulse accumulator for pulse 4. (optional)
QUANT_VA	none, see *QUANT_I*	0x32	Offset for voltage, element A
QUANT_VB	none, see *QUANT_I*	0x33	Offset for voltage, element B
QUANT_VC	none, see *QUANT_I*	0x34	Offset for voltage, element C

Name	71M6513 CE Address	71M6533 CE Address	Purpose
Outputs			
File Name	0x00	0x35	Zero-terminated ECMA/ASCII CE file name, stored in the initialization data table.
TEMP	0x40	0x9D	Difference between current temperature and calibration temperature.
FREQ	0x41	0x82	Frequency
WSUM	0x42	0x85	Wh, total
W0SUM	0x43	0x86	Wh, element A
W1SUM	0x44	0x87	Wh, element B
W2SUM	0x45	0x88	Wh, element C
VARSUM	0x46	0x8A	VARh, total
VAR0SUM	0x47	0x8B	VARh, element A
VAR1SUM	0x48	0x8C	VARh, element B
VAR2SUM	0x49	0x8D	VARh, element C
I0SQSUM	0x4A	0x8F	I, element A
I1SQSUM	0x4B	0x90	I, element B
I2SQSUM	0x4C	0x91	I, element C
INSQSUM	0x4D	0x92	I, calculated neutral
V0SQSUM	0x4E	0x93	V, element A
V1SQSUM	0x4F	0x94	V, element B
V2SQSUM	0x50	0x95	V, element C
CESTATUS	0x51	0x80	CE status bits
PH_AtoB	0x52	0x97	Measure three phase sequence.
PH_AtoC	0x53	0x98	Measure three phase sequence.
TEMP_RAW	0x54	0x81	Raw temperature
MAIN_EDGE	0x55	0x83	Count of edge-crossings
VBAT_SUM	none	0x84	Battery voltage
IDSQSUM / V3SQSUM	0x5A	0x9E	Measured neutral current, only in selected CE codes

Battery Modes

The battery modes of the 71M653X are very similar to those of the 71M6521. The 71M6513 has no comparable facility (except sleep mode, which is entered automatically when the voltage at V1 is below VBIAS). For the 71M653X series of ICs, there are three new modes (brownout, LCD, and sleep mode), as described in the data sheets.

In the 71M6513 and 71M6511, the RAM is preserved during battery (sleep) operation, but current draw on the battery is above 1 µA. In the 71M653X, the RAM is unpowered in the sleep and LCD-only mode, and becomes unreliable. However, current in these modes is less than 1 µA.

The 71M653X has eight bytes of battery-powered nonvolatile RAM, *GP0...GP*, that are not affected by sleep or LCD-only mode. These registers are only cleared when the hardware reset line is asserted or when the voltage at the VBAT pin falls below specification.

Another difference with the 71M6521 is that in order to reduce the power usage, the 71M653X's sleep mode does not preserve the LCD information. This means that the LCD display has to be rewritten when the pushbutton or sleep timer interrupts the sleep mode. The new RAM registers help support this task.

The 71M653X will operate at voltages well below most auxiliary ICs, so if the meter has no battery, the firmware must make special provisions to avoid using auxiliary EEPROMs and other devices when these are powered below their nominal supply limits. In TERIDIAN's Demo Code, the PLL_OK interrupt waits in a loop for the voltage (measured by the V1 comparator) to fail or to return to normal values.

The firmware must restart the 71M653X after any battery mode is entered, even for a brief time, because the battery modes disable the CE and ADC system. In TERIDIAN's Demo Code, the PLL_OK interrupt performs a soft reset to completely restart and reinitialize the firmware and IC. Jumping to program address zero is not an adequate restart on any TERIDIAN 80515. The soft restart should also execute RTI four times to clear pending interrupts. If not cleared, the interrupt system may fail to post interrupts.

RTC

The RTC of the 71M653X has an improved compensation system. It is designed to use less power, compensate when the software is not running, and have a verifiable calibration.

All RTC registers are in battery-backed nonvolatile RAM. If the meter should shift to battery power, the clock continues to be corrected for drift. If battery power is lost, the compensation values must be reset, and the clock is usually, but not always set to default values.

One compensation register, *RTCA_ADJ*, adjusts the crystal capacitance. Writing 0x00 to it minimizes the load capacitance, maximizing the frequency. Writing 0x3F maximizes the capacitance, thus minimizing the frequency. *RTCA_ADJ* should be set early in the meter calibration, before gain and phase errors are measured.

Another feature to aid calibration is that one-second and four-second pulses are available from the test multiplexer output, TMUX. This feature may be used to measure the effects of *RTCA_ADJ.*

The RTC also has digital adjustments, *PREG* and *QREG,* designed to adjust the long-term drift for temperature and other influences.

The long-term drift registers should be adjusted by the meter firmware as it calculates the current drift based the crystal manufacturer's temperature response curve. The firmware can periodically read the current chip temperature, and adjust the drift rate accordingly. Since the temperature characteristics of crystals usually approximate a quadratic function of temperature, a compensation based on polynomial coefficients can be used.

The RTC should be set by clearing the sub-second counter, and then copying the new values into the RTC.

Support

For further information or assistance, call your local distributor.

Revision History

Revision	Date	Description
Rev. 1.0	12/04/2008	First publication.

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