INA230 36-V, 16-Bit, I²C Output Current, Voltage and Power Monitor With Alert

1 Features

- Bus voltage sensing from 0 V to 36 V
- High- or low-side sensing
- Current, voltage, and power reporting
- High accuracy:
  - 0.3% gain error (maximum)
  - 25-µV offset (maximum)
- Configurable averaging options
- Programmable alert threshold
- Power supply operation: 2.7 V to 5.5 V
- Packages:
  - 16-pin RGT (VQFN)
  - 10-pin DGS (VSSOP)

2 Applications

- Servers
- Computers
- Power management
- Battery chargers
- Power supplies
- Test equipment
- Telecom equipment

3 Description

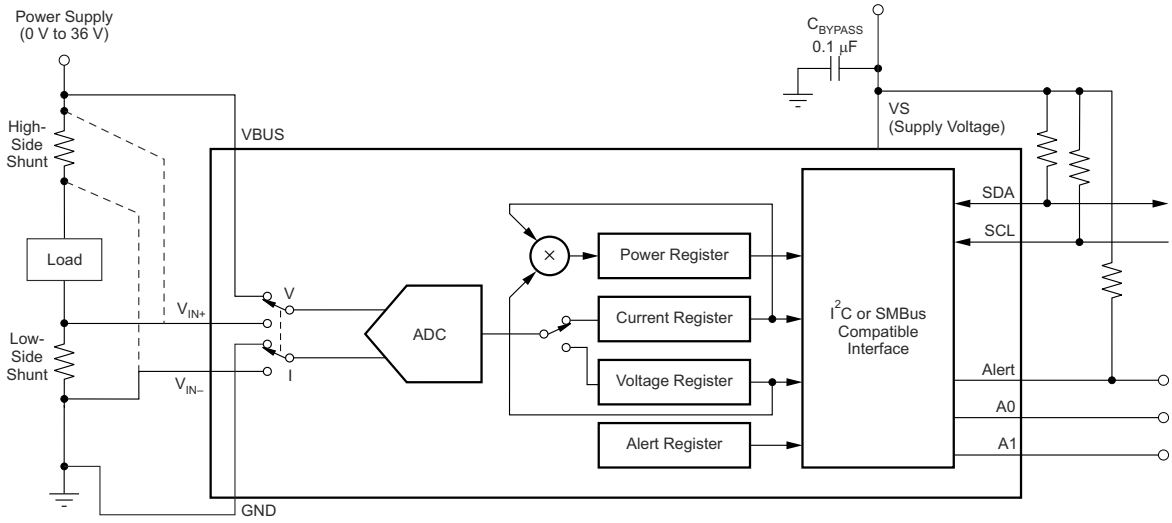
The INA230 is a current-shunt and power monitor with an I²C interface that features 16 programmable addresses. The INA230 monitors both shunt voltage drops and bus supply voltage. Programmable calibration value, conversion times, and averaging, combined with an internal multiplier, enable direct readouts of current in amperes and power in watts.

The INA230 senses current on buses that vary from 0 V to 36 V, with the device powered from a single 2.7-V to 5.5-V supply, drawing 330 µA (typical) of supply current. The INA230 is specified over the operating temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA230	VQFN (16)	3.00 mm × 3.00 mm
	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Revision History

Changes from Revision * (February 2012) to Revision A (December 2021) **Page**

- Added *ESD Ratings* table, *Recommended Operating Conditions* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section....1
- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Added the DGS (VSSOP) package....1
- Increased common-mode voltage range....4
- Improved common-mode rejection, offset, and gain error specifications....5

5 Related Products

Table 5-1. Related Products

DESCRIPTION	DEVICE
36-V, 16-Bit, High-Side or Low-Side Measurement, Current and Power Monitor	INA226
48-V, 16-Bit, Ultra-Precise, Current, Voltage, and Power Monitor	INA236
85-V, 16-Bit, Precision Power Monitor	INA237
28-V, 12-Bit, Current, Voltage, and Power Monitor	INA234
26-V, Zerø-Drift, Bidirectional Current Power Monitor	INA219

6 Pin Configuration and Functions

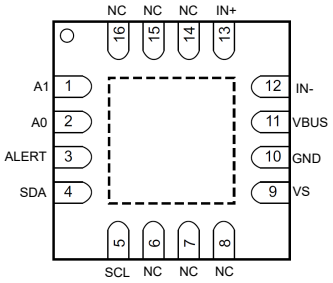


Figure 6-1. RGT Package 16-Pin VQFN (Top View)

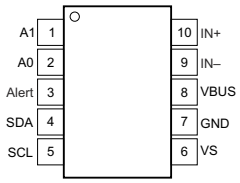


Figure 6-2. DGS Package 10-Pin VSSOP (Top View)

Table 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	VQFN	VSSOP		
A0	2	2	Digital input	Address pin. Connect to GND, SCL, SDA, or V_S. Table 8-2 shows pin settings and corresponding addresses.
A1	1	1	Digital input	Address pin. Connect to GND, SCL, SDA, or V_S. Table 8-2 shows pin settings and corresponding addresses.
ALERT	3	3	Digital output	Multi-functional alert, open-drain output.
GND	10	7	Analog	Ground
NC	6, 7, 8, 14, 15, 16	—	—	No internal connection
SCL	5	5	Digital input	Serial bus clock line, open-drain input.
SDA	4	4	Digital input/output	Serial bus data line, open-drain input/output.
VBUS	11	8	Analog input	Bus voltage input
IN–	12	9	Analog input	Negative differential shunt voltage input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+	13	10	Analog input	Positive differential shunt voltage input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
V_S	9	6	Analog	Power supply, 2.7 V to 5.5 V.
Thermal Pad	—	PAD	—	This pad can be connected to ground or left floating.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply Voltage		6	V
V_{IN+}, V_{IN-}	Differential (V_{IN+}) - (V_{IN-})	–40	40	V
	Common - mode	GND – 0.3	40	V
V_{IO}	SDA, ALERT, A0	GND – 0.3	6	V
V_{IO}	SCL	GND – 0.3	V_S + 0.3	V
	Input current into any pin		5	mA
	Open-drain digital output current (SDA, ALERT)		10	mA
T_A	Operating Temperature	–55	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range	0		36	V
V_S	Operating supply range	2.7		5.5	V
T_A	Ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA230		UNIT
		DGS (VSSOP)	RGT(QFN)	
		10 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	162.8	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.6	58.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.9	19.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.6	1.3	°C/W
Y_{JB}	Junction-to-board characterization parameter	82.4	19.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = 3.3 V, V_{SENSE} = V_{IN+} - V_{IN-} = 0 mV, V_{IN-} = V_{BUS} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
	Shunt voltage input range		–81.92		81.9175	mV
CMRR	Common-mode rejection	V_{CM} = 0 V to 36 V, T_A = –40°C to 125°C	120	140		dB
V_{os}	Shunt offset voltage	V_{CM} = 12 V		–9.8	±25	µV
dV_{os}/dT	Shunt offset voltage drift	T_A = –40°C to +125°C		±0.05	±0.1	µV/°C
$PSRR_{SHUNT}$	Power supply rejection ratio (Current measurements)			–3.0		µV/V
V_{os_b}	Bus offset Voltage			+2.3	±15	mV
dV_{os_b}/dT	Bus offset voltage drift	T_A = –40°C to +125°C			±40	µV/°C
$PSRR_{BUS}$	Power supply rejection ratio (Voltage measurements)			0.4		mV/V
Z_{BUS}	BUS input impedance			830		kΩ
I_B	Input bias current	IN+, IN-, Current measurement mode		10		µA
I_{B_SHDWN}	Input Leakage	IN+, IN-, Shutdown Mode		0.1	0.5	µA
DC ACCURACY						
	ADC Resolution	T_A = –40°C to 125°C		16		Bits
	1 LSB step size	Shunt Voltage		2.5		µV
	1 LSB step size	Bus Voltage		1.25		mV
	ADC Conversion-time	CT bit = 000		140	154	µs
		CT bit = 001		204	224	µs
		CT bit = 010		332	365	µs
		CT bit = 011		588	646	µs
		CT bit = 100		1.100	1.21	ms
		CT bit = 101		2.116	2.328	ms
		CT bit = 110		4.156	4.572	ms
		CT bit = 111		8.244	9.068	ms
G_{SERR}	Shunt voltage gain error			±0.010	±0.3	%
G_{S_DRFT}	Shunt voltage gain error drift	T_A = –40°C to +125°C		10	50	ppm/°C
G_{BERR}	Bus voltage gain error			±0.010	±0.3	%
G_{B_DRFT}	Bus voltage gain error drift	T_A = –40°C to +125°C		10	50	ppm/°C
DNL	Differential Non-Linearity			±0.1		LSB
POWER SUPPLY						
I_Q	Quiescent current	V_{SENSE} = 0 mV		330	420	µA
		Shutdown		0.5	2	µA

at T_A = 25°C, V_S = 3.3 V, V_{SENSE} = V_{IN+} - V_{IN-} = 0 mV, V_{IN-} = V_{BUS} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SMBUS						
	SMBUS timeout			28	35	ms
DIGITAL INPUT / OUTPUT						
	Input capacitance			3		pF
V_{IH}	Logic input level, high		0.7 × V_S		6	V
V_{IL}	Logic input level, low		–0.5		0.3 × V_S	V
V_{HYS}	Hysteresis			500		mV
V_{OL}	Logic output level, low	I_{OL} = 3 mA	0		0.4	V
	Digital leakage input current	0 ≤ V_{INPUT} ≤ V_S		0.1	1	µA

7.6 Timing Requirements (I^2C)

		MIN	NOM	MAX	UNIT
I^2C BUS (FAST MODE)					
$F_{(SCL)}$	I^2C clock frequency	1		400	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	600			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	0			ns
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1300			ns
$t_{(HIGH)}$	SCL clock high period	600			ns
t_F	Clock/data fall time			300	ns
t_R	Clock/data rise time			300	ns
t_R	Clock rise time (SCLK ≤ 100 kHz)			1000	ns
I^2C BUS (HIGH-SPEED MODE)					
$F_{(SCL)}$	I^2C clock frequency	10		3400	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	160			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	0			ns
$t_{(SUDAT)}$	Data setup time	10			ns
$t_{(LOW)}$	SCL clock low period	160			ns
$t_{(HIGH)}$	SCL clock high period	60			ns
t_F	Clock/data fall time			160	ns
t_R	Clock/data rise time			160	ns

7.7 Typical Characteristics

At T_A = +25°C, V_S = +3.3 V,V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV, and V_{BUS} = 12 V, unless otherwise noted.

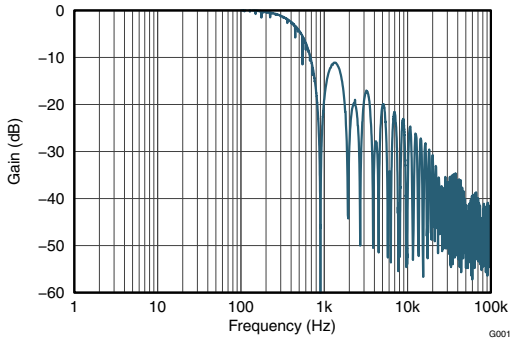


Figure 7-1. Frequency Response

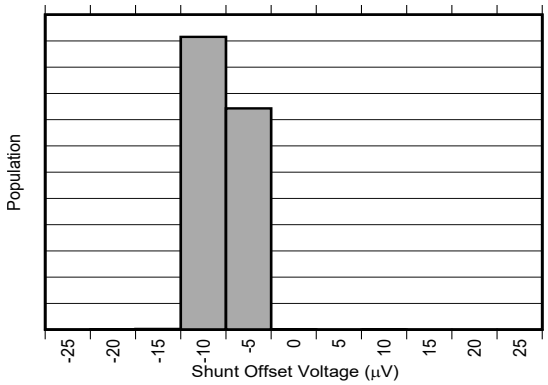


Figure 7-2. Shunt Input Offset Voltage Production Distribution

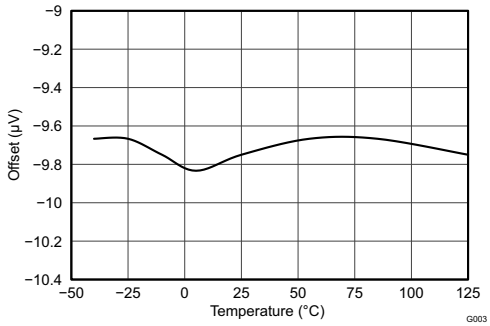


Figure 7-3. Shunt Input Offset Voltage vs. Temperature

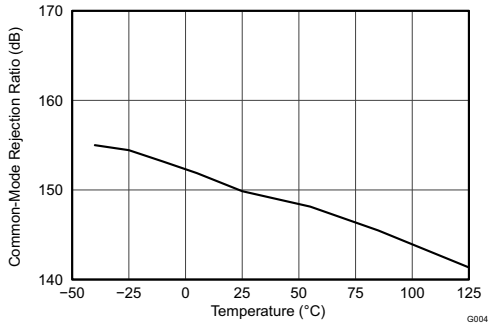


Figure 7-4. Shunt Input Common-Mode Rejection Ratio vs. Temperature

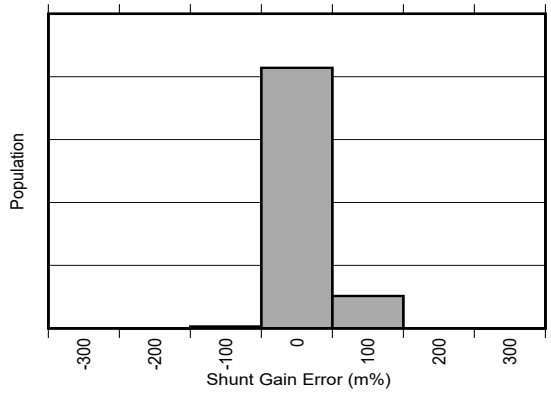


Figure 7-5. Shunt Input Gain Error Production Distribution

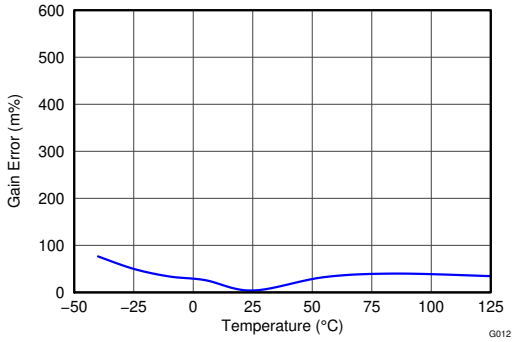


Figure 7-6. Shunt Input Gain Error vs. Temperature

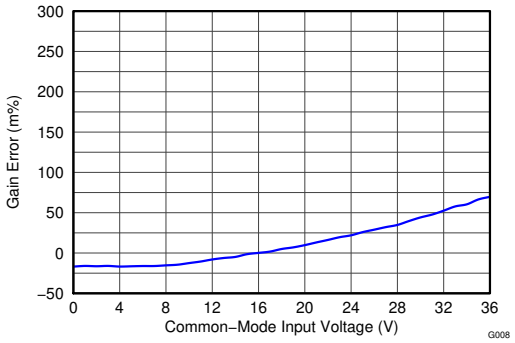


Figure 7-7. Shunt Input Gain Error vs. Common-Mode Voltage

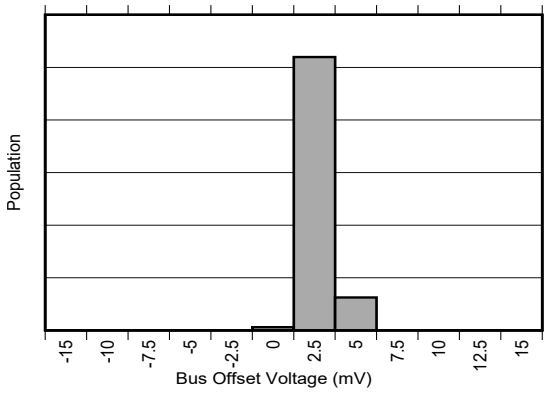


Figure 7-8. Bus Input Offset Voltage Production Distribution

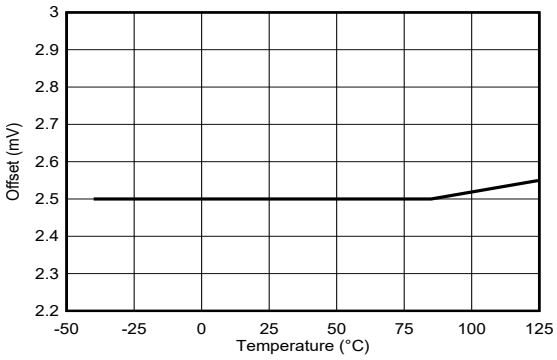


Figure 7-9. Bus Input Offset Voltage vs. Temperature

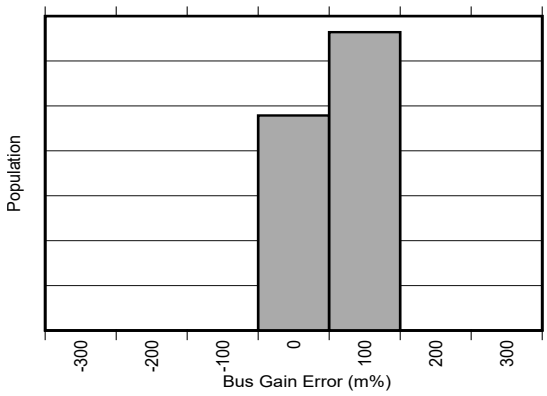


Figure 7-10. Bus Input Gain Error Production Distribution

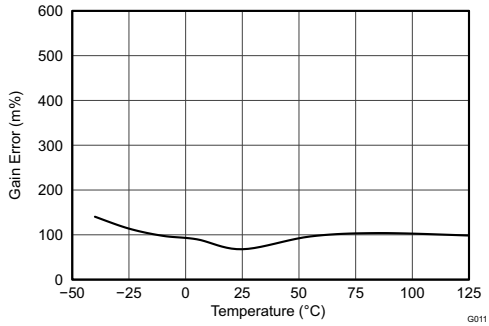


Figure 7-11. Bus Input Gain Error vs. Temperature

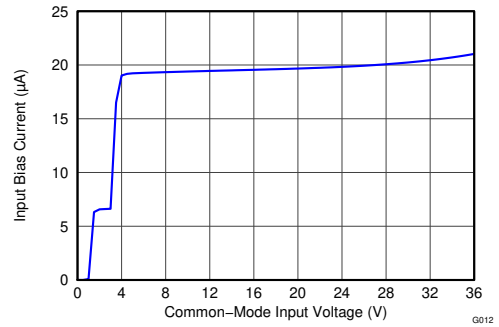


Figure 7-12. Input Bias Current (I_{B+} + I_{B-}) vs. Common-Mode Voltage

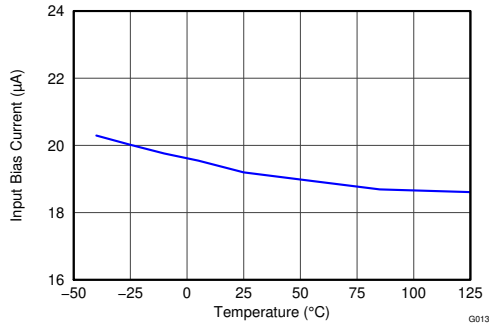


Figure 7-13. Input Bias Current (I_{B+} + I_{B-}) vs. Temperature

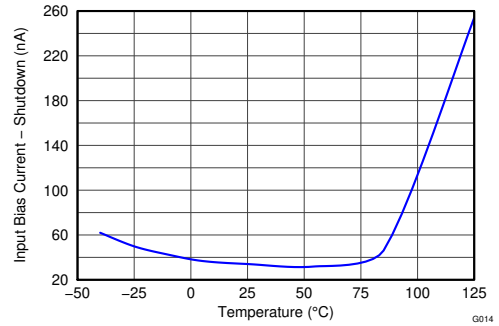


Figure 7-14. Input Bias Current vs. Temperature, Shutdown

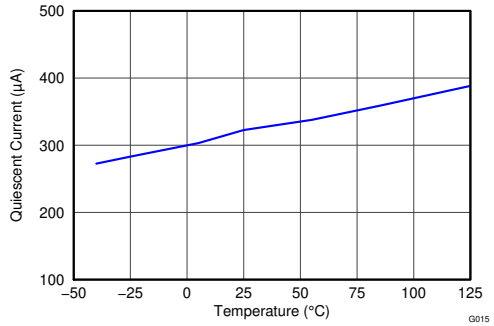


Figure 7-15. Active I_Q vs. Temperature

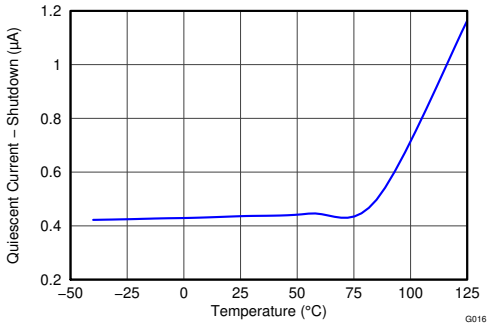


Figure 7-16. Shutdown I_Q vs. Temperature

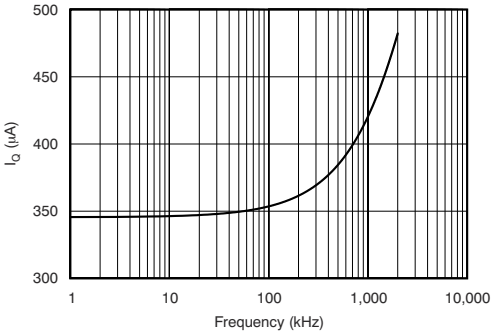


Figure 7-17. Active I_Q vs. I^2C Clock Frequency

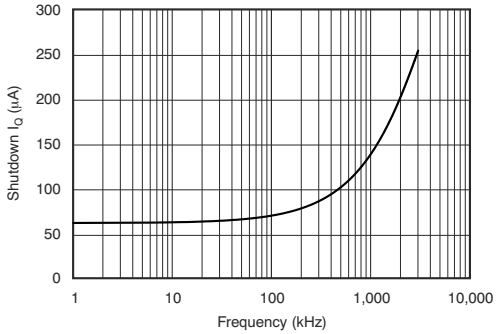


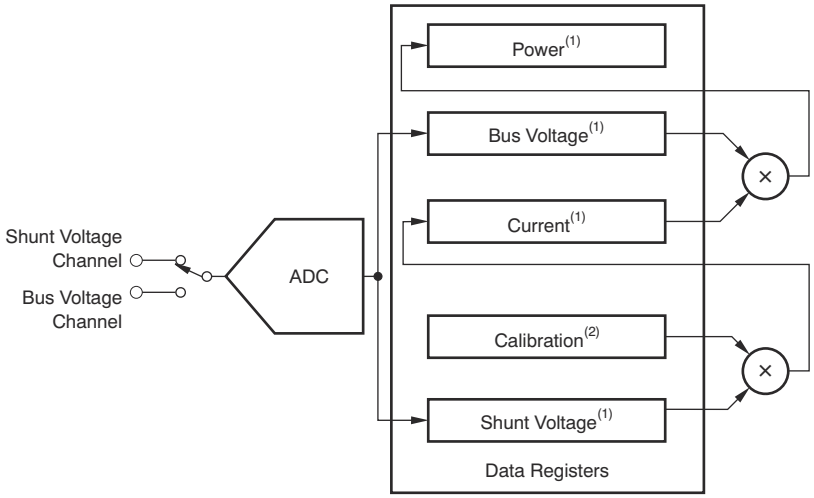
Figure 7-18. Shutdown I_Q vs. I^2C Clock Frequency

8 Detailed Description

8.1 Overview

The INA230 is a digital current sense amplifier with an I^{2}C- and SMBus-compatible interface. The device provides digital current, voltage, and power readings necessary for accurate decision-making in precisely-controlled systems. Programmable registers allow flexible configuration for measurement resolution as well as continuous-versus-triggered operation. Detailed register information appears at the end of this data sheet, beginning with Table 8-3. See the *Functional Block Diagram* for a block diagram of the INA230 device.

8.2 Functional Block Diagram



(1) Read-only

(2) Read/write

8.3 Feature Description

8.3.1 Basic ADC Functions

The INA230 device performs two measurements on the power-supply bus of interest. The voltage developed from the load current that flows through a shunt resistor creates a shunt voltage that is measured at the IN+ and IN– pins. The device can also measure the power supply bus voltage by connecting this voltage to the VBUS pin. The differential shunt voltage is measured with respect to the IN– pin while the bus voltage is measured with respect to ground.

The device is typically powered by a separate supply that can range from 2.7 V to 5.5 V. The bus that is being monitored can range in voltage from 0 V to 36 V. Based on the fixed 1.25-mV LSB for the Bus Voltage register, a full-scale register results in a 40.96-V value.

Note

Do not apply more than 36 V of actual voltage to the input pins.

There are no special considerations for power-supply sequencing because the common-mode input range and power-supply voltage are independent of each other, therefore the bus voltage can be present with the supply voltage off and vice-versa.

The device takes two measurements: shunt voltage and bus voltage. The device then converts these measurements to current, based on the Calibration register value, and then calculates power. Refer to the *Programming the Calibration Register* section for additional information on programming the Calibration register.

The device has two operating modes—continuous and triggered—that determine how the ADC operates following these conversions. When the device is in the normal operating mode (that is, MODE bits of the

Configuration register (00h) are set to '111'), the INA230 continuously converts a shunt voltage reading followed by a bus voltage reading. After the shunt voltage reading, the current value is calculated (based on Equation 3). This current value is then used to calculate the power result (using Equation 4). These values are subsequently stored in an accumulator, and the measurement/calculation sequence repeats until the number of averages set in the Configuration register (00h) is reached. Following every sequence, the present set of values measured and calculated are appended to previously collected values. After all of the averaging is complete, the final values for shunt voltage, bus voltage, current, and power are updated in the corresponding registers that can then be read. These values remain in the data output registers until they are replaced by the next fully completed conversion results. Reading the data output registers does not affect a conversion in progress.

The mode control in the Conversion register (00h) also permits selecting modes to convert only the shunt voltage or the bus voltage to further allow the user to configure the monitoring function to fit the specific application requirements.

All current and power calculations are performed in the background and do not contribute to conversion time.

In triggered mode, writing any of the triggered convert modes into the Configuration register (00h) (that is, MODE bits of the Configuration register (00h) are set to ‘001’, ‘010’, or ‘011’) triggers a single-shot conversion. This action produces a single set of measurements; thus, to trigger another single-shot conversion, the Configuration register (00h) must be written to a second time, even if the mode does not change.

In addition to the two operating modes (continuous and triggered), the device also has a power-down mode that reduces the quiescent current and turns off current into the device inputs, reducing the impact of supply drain when the device is not being used. Full recovery from power-down mode requires 40 µs. The registers of the device can be written to and read from while the device is in power-down mode. The device remains in power-down mode until one of the active modes settings are written into the Configuration register (00h).

Although the device can be read at any time, and the data from the last conversion remain available, the Conversion Ready flag bit (Mask/Enable register, CVRF bit) is provided to help coordinate one-shot or triggered conversions. The Conversion Ready flag (CVRF) bit is set after all conversions, averaging, and multiplication operations are complete.

The Conversion Ready flag (CVRF) bit clears under these conditions:

- Writing to the Configuration register (00h), except when configuring the MODE bits for power-down mode; or
- Reading the Mask/Enable register (06h)

8.3.2 Power Calculation

The Current and Power are calculated following shunt voltage and bus voltage measurements (see Figure 8-1). Current is calculated following a shunt voltage measurement based on the value set in the Calibration register. If there is no value loaded into the Calibration register, the current value stored is zero. Power is calculated following the bus voltage measurement based on the previous current calculation and bus voltage measurement. If there is no value loaded in the Calibration register, the power value stored is also zero. Again, these calculations are performed in the background and do not add to the overall conversion time. These current and power values are considered intermediate results (unless the averaging is set to 1) and are stored in an internal accumulation register, not the corresponding output registers. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register until all of the samples have been measured and averaged based on the number of averages set in the Configuration register (00h).

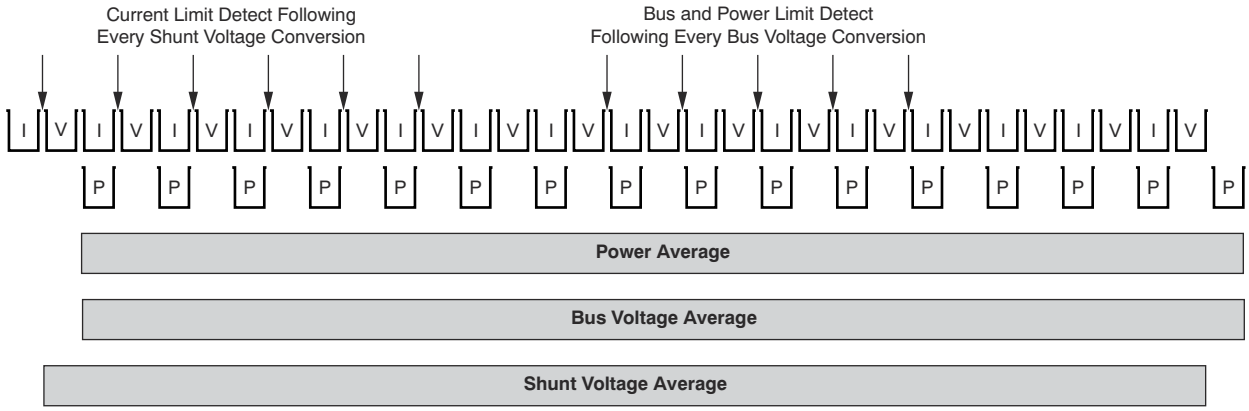


Figure 8-1. Power Calculation Scheme

In addition to the current and power accumulating after every sample, the shunt and bus voltage measurements are also collected. After all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers, where they can then be read.

8.3.3 Alert Pin

The INA230 has a single Alert Limit register (07h), that allows the Alert pin to be programmed to respond to a single user-defined event or to a Conversion Ready notification if desired. The Mask/Enable register allows the user to select from one of the five available functions to monitor and/or set the Conversion Ready bit to control the response of the Alert pin. Based on the function being monitored, the user would then enter a value into the Alert Limit register to set the corresponding threshold value that asserts the Alert pin.

The Alert pin allows for one of several available alert functions to be monitored to determine if a user-defined threshold has been exceeded. The five alert functions that can be monitored are:

- Shunt Voltage Over-Limit (SOL)
- Shunt Voltage Under-Limit (SUL)
- Bus Voltage Over-Limit (BOL)
- Bus Voltage Under-Limit (BUL)
- Power Over-Limit (POL)

The Alert pin is an open-drain output. This pin is asserted when the alert function selected in the Mask/Enable register exceeds the value programmed into the Alert Limit register. Only one of these alert functions can be enabled and monitored at a time. If multiple alert functions are enabled, the selected function in the highest significant bit position takes priority and responds to the Alert Limit register value. For example, if the Shunt Voltage Over-Limit function and the Shunt Voltage Under-Limit function are both selected, the Alert pin asserts when the Shunt Voltage register exceeds the value in the Alert Limit register.

The Conversion Ready state of the device can also be monitored at the Alert pin to inform the user when the device has completed the previous conversion and is ready to begin a new conversion. Conversion Ready can be monitored at the Alert pin along with one of the alert functions. If an alert function and the Conversion Ready are both enabled to be monitored at the Alert pin, after the Alert pin is asserted, the Mask/Enable register must be read following the alert to determine the source of the alert. By reading the Conversion Ready Flag (CVRF, bit 3), and the Alert Function Flag (AFF, bit 4) in the Mask/Enable register, the source of the alert can be determined. If the Conversion Ready feature is not desired and the CNVR bit is not set, the Alert pin only responds to an exceeded alert limit based on the alert function enabled.

If the alert function is not used, the Alert pin can be left floating without impacting the operation of the device.

Refer to Figure 8-1 to see the relative timing of when the value in the Alert Limit register is compared to the corresponding converted value. For example, if the alert function that is enabled is Shunt Voltage Over-Limit (SOL), following every shunt voltage conversion the value in the Alert Limit register is compared to the measured shunt voltage to determine if the measurements has exceeded the programmed limit. The AFF, bit 4 of the

Mask/Enable register, asserts high any time the measured voltage exceeds the value programmed into the Alert Limit register. In addition to the AFF being asserted, the Alert pin is asserted based on the Alert Polarity Bit (APOL, bit 1 of the Mask/Enable register). If the Alert Latch is enabled, the AFF and Alert pin remain asserted until either the Configuration register (00h) is written to or the Mask/Enable register is read.

The Bus Voltage alert functions compare the measured bus voltage to the Alert Limit register following every bus voltage conversion and assert the AFF bit and Alert pin if the limit threshold is exceeded.

The Power Over-Limit alert function is also compared to the calculated power value following every bus voltage measurement conversion and asserts the AFF bit and Alert pin if the limit threshold is exceeded.

8.4 Device Functional Modes

8.4.1 Averaging and Conversion Time Considerations

The INA230 device offers programmable conversion times (t_{CT}) for both the shunt voltage and bus voltage measurements. The conversion times for these measurements can be selected from as fast as 140 µs to as long as 8.244 ms. The conversion time settings, along with the programmable averaging mode, allow the device to be configured to optimize the available timing requirements in a given application. For example, if a system requires that data be read every 5 ms, the device could be configured with the conversion times set to 588 µs for both shunt and bus voltage measurements and the averaging mode set to 4. This configuration results in the data updating approximately every 4.7 ms. The device could also be configured with a different conversion time setting for the shunt and bus voltage measurements. This type of approach is common in applications where the bus voltage tends to be relatively stable. This situation can allow for the time focused on the bus voltage measurement to be reduced relative to the shunt voltage measurement. The shunt voltage conversion time could be set to 4.156 ms with the bus voltage conversion time set to 588 µs, with the averaging mode set to 1. This configuration also results in data updating approximately every 4.7 ms.

There are trade-offs associated with the settings for conversion time and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal. This approach allows the device to reduce any noise in the measurement that may be caused by noise coupling into the signal. A greater number of averages enables the device to be more effective in reducing the noise component of the measurement.

The conversion times selected can also have an impact on the measurement accuracy. Figure 8-2 shows multiple conversion times to illustrate the impact of noise on the measurement. To achieve the highest accuracy measurement possible, use a combination of the longest allowable conversion times and highest number of averages based on the timing requirements of the system.

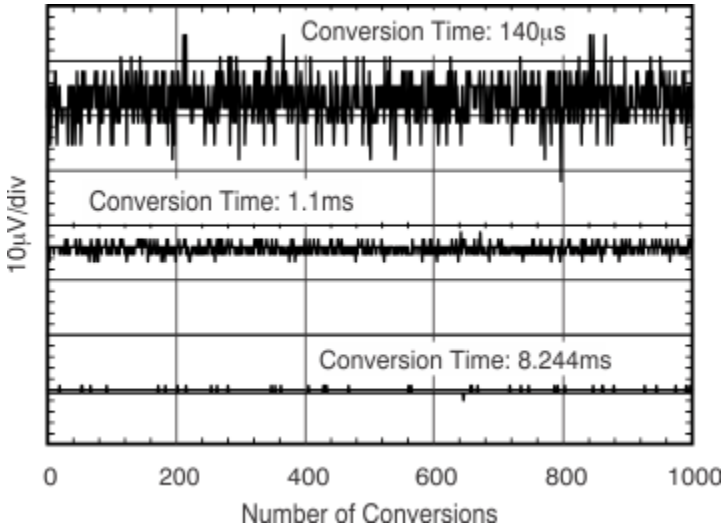


Figure 8-2. Noise vs. Conversion Time

8.4.2 Filtering and Input Considerations

Measuring current is often noisy, and such noise can be difficult to define. The INA230 device offers several options for filtering by allowing the conversion times and number of averages to be selected independently in the Configuration register (00h). The conversion times can be set independently for the shunt voltage and bus voltage measurements to allow added flexibility in configuring the monitoring of the power-supply bus.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500 kHz (±30%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1 MHz and higher, they can be managed by incorporating filtering at the input of the device. The high frequency enables the use of low-value series resistors on the filter with negligible effects on measurement accuracy. In general, filtering the device input is only necessary if there are transients at exact harmonics of the 500 kHz (±30%) sampling rate (greater than 1 MHz). Filter using the lowest possible series resistance (typically 10 Ω or less) and a ceramic capacitor. Recommended values for this capacitor are between 0.1 µF and 1 µF. Figure 8-3 shows the device with a filter added at the input.

Overload conditions are another consideration for the device inputs. The device inputs are specified to tolerate 40 V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). Removing a short to ground can result in inductive kickbacks that could exceed the 40-V differential and common-mode rating of the device. Inductive kickback voltages are best controlled by Zener-type transient-absorbing devices (commonly called *transzorbs*) combined with sufficient energy storage capacitance. See the TI Design *Transient Robustness for Current Shunt Monitors* (TIDU473) which describes a high-side current shunt monitor used to measure the voltage developed across a current-sensing resistor when current passes through it.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, particularly in applications with no large electrolytics present. This problem occurs because an excessive dV/dt can activate the ESD protection in the device in systems where large currents are available. Testing demonstrates that the addition of 10-Ω resistors in series with each input of the device sufficiently protects the inputs against this dV/dt failure up to the 40-V rating of the device. Selecting these resistors in the range noted has minimal effect on accuracy.

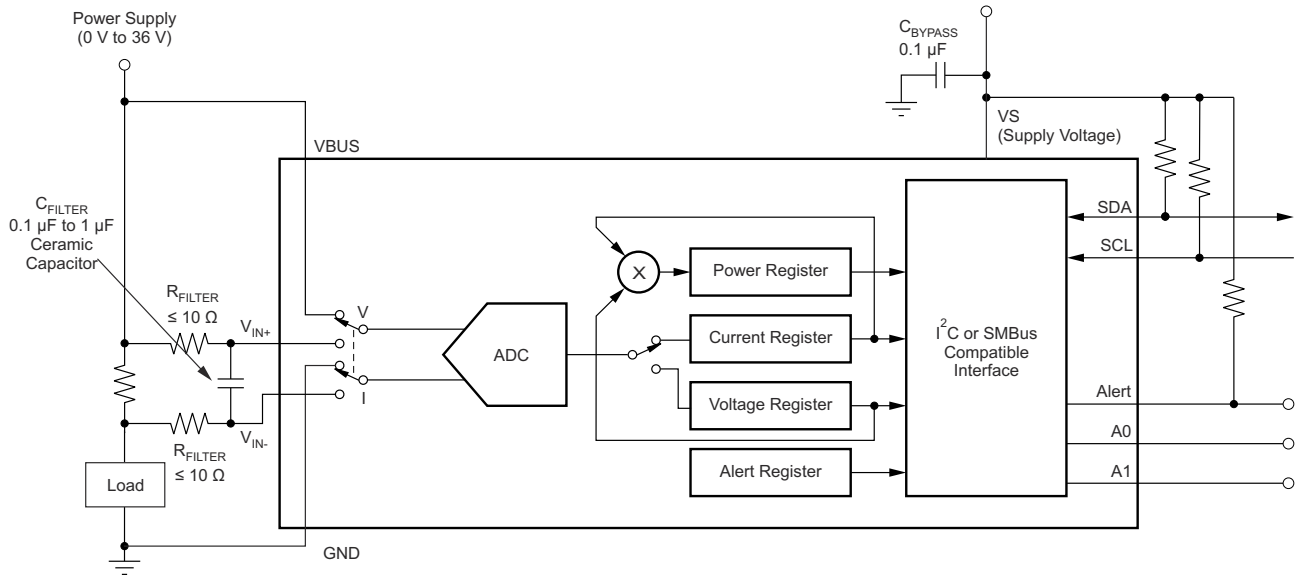


Figure 8-3. Input Filtering

8.5 Programming

An important aspect of the INA230 is that it does not necessarily measure current or power. The INA230 measures both the differential voltage applied between the IN+ and IN– input pins and the voltage applied to the BUS pin. For the INA230 to report both current and power values, both the Current register resolution and the value of the shunt resistor present in the application that resulted in the differential voltage being developed must be programmed. The Power register is internally set to be 25 times the programmed least significant bit of the current register (Current_LSB). Both the Current_LSB and shunt resistor value are used when calculating the Calibration register value. The INA230 uses this value to calculate the corresponding current and power values based on the measured shunt and bus voltages.

The Calibration register is calculated based on Equation 1. This equation includes the term Current_LSB, the programmed value for the LSB for the Current register. This is the value used to convert the value in the Current register to the actual current in amps. The highest resolution for the Current register can be obtained by using the smallest allowable Current_LSB based on the maximum expected current, as shown in Equation 2. While this value yields the highest resolution, it is common to select a value for the Current_LSB to the nearest round number above this value to simplify the conversion of the Current register and Power register to amps and watts respectively. R_{SHUNT} is the value of the external shunt used to develop the differential voltage across the input pins. The 0.00512 value in Equation 1 is an internal fixed value used to ensure scaling is maintained properly.

$$CAL = \frac{0.00512}{Current\_LSB \bullet R_{SHUNT}} \quad (1)$$

$$Current\_LSB = \frac{Maximum\ Expected\ Current}{2^{15}} \quad (2)$$

After the Calibration register has been programmed, the Current register and Power register are updated accordingly based on the corresponding shunt voltage and bus voltage measurements. Until the Calibration register is programmed, the Current and Power registers remain at zero.

8.5.1 Programming the Calibration Register

Figure 9-1 shows a nominal 10-A load that creates a differential voltage of 20 mV across a 2-mΩ shunt resistor. The bus voltage for the INA230 is measured at the external VBUS input pin, which in this example is connected to the IN– pin to measure the voltage level delivered to the load. For this example, the VBUS pin measures less than 12 V because the voltage at the IN– pin is 11.98 V as a result of the voltage drop across the shunt resistor.

For this example, assuming a maximum expected current of 15 A, the Current_LSB is calculated to be 457.7 µA/bit using Equation 2. Using a value for the Current_LSB of 500 µA/bit or 1 mA/bit would significantly simplify the conversion from the Current register (04h) and Power register (03h) to amperes and watts. For this example, a value of 1 mA/bit was chosen for the Current_LSB. Using this value for the Current_LSB does trade a small amount of resolution for having a simpler conversion process on the user side. Using Equation 1 in this example with a Current_LSB value of 1 mA/bit and a shunt resistor of 2 mΩ results in a Calibration register value of 2560, or A00h.

The Current register (04h) is then calculated by multiplying the decimal value of the Shunt Voltage register (01h) contents by the decimal value of the Calibration register and then dividing by 2048, as shown in Equation 3. For this example, the Shunt Voltage register contains a value of 8,000 (representing 20 mV), which is multiplied by the Calibration register value of 2560 and then divided by 2048 to yield a decimal value for the Current register (04h) of 10000, or 2710h. Multiplying this value by 1 mA/bit results in the original 10-A level stated in the example.

$$Current = \frac{ShuntVoltage \bullet CalibrationRegister}{2048} \quad (3)$$

The LSB for the Bus Voltage register (02h) is a fixed 1.25 mV/bit, which means that the 11.98 V present at the VBUS pin results in a register value of 2570h, or a decimal equivalent of 9584. Note that the MSB of the Bus Voltage register (02h) is always zero because the VBUS pin is only able to measure positive voltages.

The Power register (03h) is then calculated by multiplying the decimal value of the Current register, 10000, by the decimal value of the Bus Voltage register (02h), 9584, and then dividing by 20,000, as defined in Equation 4. For this example, the result for the Power register (03h) is 12B8h, or a decimal equivalent of 4792. Multiplying this result by the power LSB (25 times the [1 × 10^{-3} Current_LSB]) results in a power calculation of (4792 × 25 mW/bit), or 119.82 W. The power LSB has a fixed ratio to the Current_LSB of 25. For this example, a programmed 1 mA/bit Current_LSB results in a power LSB of 25 mW/bit. This ratio is internally programmed to ensure that the scaling of the power calculation is within an acceptable range. A manual calculation for the power being delivered to the load would use a bus voltage of 11.98 V (12 V_{CM} – 20 mV shunt drop) multiplied by the load current of 10 A to give a result of 119.8 W.

$$\text{Power} = \frac{\text{Current} \bullet \text{BusVoltage}}{20{,}000} \tag{4}$$

Table 8-1 lists the steps for configuring, measuring, and calculating the values for current and power for this device.

Table 8-1. Calculating Current and Power(1)

STEP	REGISTER NAME	ADDRESS	CONTENTS	DEC	LSB	VALUE
Step 1	Configuration register	00h	4127h	—	—	—
Step 2	Shunt register	01h	1F40h	8000	2.5 µV	20 mV
Step 3	Bus Voltage register	02h	2570h	9584	1.25 mV	11.98 V
Step 4	Calibration register	05h	A00h	2560	—	—
Step 5	Current register	04h	2710	10000	1 mA	10 A
Step 6	Power register	03h	12B8h	4792	25 mW	119.82 W

(1) Conditions: Load = 10 A, V_{CM} = 12 V, R_{SHUNT} = 2 mΩ, and V_{VBUS} = 12 V.

8.5.2 Programming the INA230 Power Measurement Engine

8.5.2.1 Calibration Register and Scaling

The Calibration register makes it possible to set the scaling of the Current and Power registers to the values that are most useful for a given application. One strategy may be to set the Calibration register so that the largest possible number is generated in the Current register or Power register at the expected full-scale point. This approach yields the highest resolution based on the previously calculated minimum Current_LSB in the equation for the Calibration register (Equation 1). The Calibration register can also be selected to provide values in the Current and Power registers that either provide direct decimal equivalents of the values being measured, or yield a round LSB value for each corresponding register. After these choices have been made, the Calibration register also offers possibilities for end-user, system-level calibration. By physically measuring the current with an external ammeter, the exact current is known. The value of the Calibration register can then be adjusted based on the measured current result of the INA230 to cancel the total system error, as shown in Equation 5.

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left[\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{INA230\_Current}}\right] \tag{5}$$

8.5.3 Simple Current Shunt Monitor Usage (No Programming Necessary)

The INA230 can be used without any programming if it is only necessary to read a shunt voltage drop and bus voltage with the default power-on reset configuration and continuous conversion of shunt and bus voltage.

Without programming the INA230 Calibration register, the device is unable to provide either a valid current or power value, because these outputs are both derived using the values loaded into the Calibration register.

8.5.4 Default INA230 Settings

The default power-up states of the registers are shown in the *Register Maps* section of this data sheet. These registers are volatile, and if programmed to a value other than the default values shown in Table 8-3, they must be reprogrammed at every device power up. Detailed information on programming the Calibration register is given in the *Programming* section and calculated based on Equation 1.

8.5.5 Bus Overview

The INA230 offers compatibility with both I^2C and SMBus interfaces. The I^2C and SMBus protocols are essentially compatible with one another.

The I^2C interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is discussed. Two bidirectional lines, SCL and SDA, connect the INA230 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates a data transfer is called a *controller*, and the devices controlled by the controller are *target* devices. The bus must be controlled by a controller device that generates the serial clock (SCL), controls the bus access, and generates start and stop conditions.

To address a specific device, the controller initiates a start condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All target devices on the bus shift in the target address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target device being addressed responds to the controller by generating an *Acknowledge* bit (ACK) and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an ACK. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

Once all data have been transferred, the controller generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The INA230 includes a 28-ms timeout on its interface to prevent locking up the bus.

8.5.5.1 Serial Bus Address

To communicate with the INA230, the controller must first address target devices using a corresponding target address byte. The target address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The INA230 has two address pins: A0 and A1. Table 8-2 describes the pin logic levels for each of the 16 possible addresses. The state of pins A0 and A1 is sampled on every bus communication and should be set before any activity on the interface occurs.

Table 8-2. INA230 Address Pins and Target Addresses

A1	A0	TARGET ADDRESS
GND	GND	1000000
GND	V_S	1000001
GND	SDA	1000010
GND	SCL	1000011
V_S	GND	1000100
V_S	V_S	1000101
V_S	SDA	1000110
V_S	SCL	1000111
SDA	GND	1001000
SDA	V_S	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V_S	1001101

Table 8-2. INA230 Address Pins and Target Addresses (continued)

A1	A0	TARGET ADDRESS
SCL	SDA	1001110
SCL	SCL	1001111

8.5.5.2 Serial Interface

The INA230 operates only as a target device on both the I^2C bus and the SMBus. Connections to the bus are made through the open-drain I/O lines, SDA, and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although there is spike suppression integrated into the digital I/O lines, proper layout should be used to minimize the amount of coupling into the communication lines. This noise introduction could occur from capacitively coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a printed circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielding communication lines in general is recommended to reduce to possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted as start or stop commands.

The INA230 supports the transmission protocol for Fast (1 kHz to 400 kHz) and High-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted most significant byte first.

8.5.6 Writing to and Reading From the I^2C Serial Interface

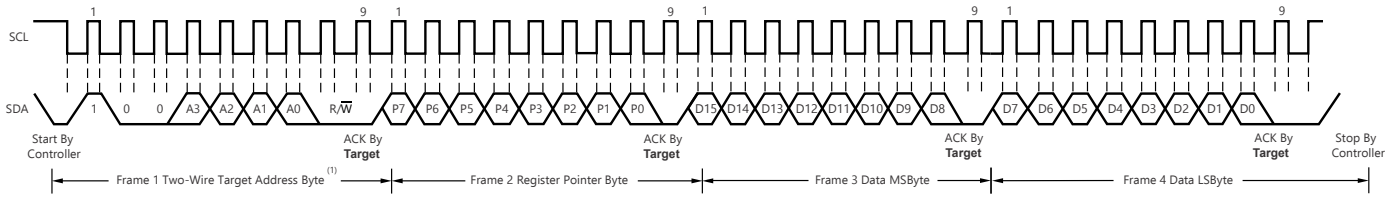
Accessing a specific register on the INA230 is accomplished by writing the appropriate value to the register pointer. Refer to *Register Maps* for a complete list of registers and corresponding addresses. The value for the register pointer (see Figure 8-7) is the first byte transferred after the target address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the controller. This byte is the target address, with the R/$\overline{W}$ bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the controller is the address of the register to be accessed. This register address value updates the register pointer to the desired internal device register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The controller may terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a target address byte with the R/$\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The controller then generates a start condition and sends the address byte for the target with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the target and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the controller, then the target transmits the least significant byte. The controller may or may not acknowledge receipt of the second data byte. The controller may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the device retains the register pointer value until it is changed by the next write operation.

Figure 8-4 shows the write operation timing diagram. Figure 8-5 shows the read operation timing diagram. These diagrams are shown for reading/writing to 16-bit registers.

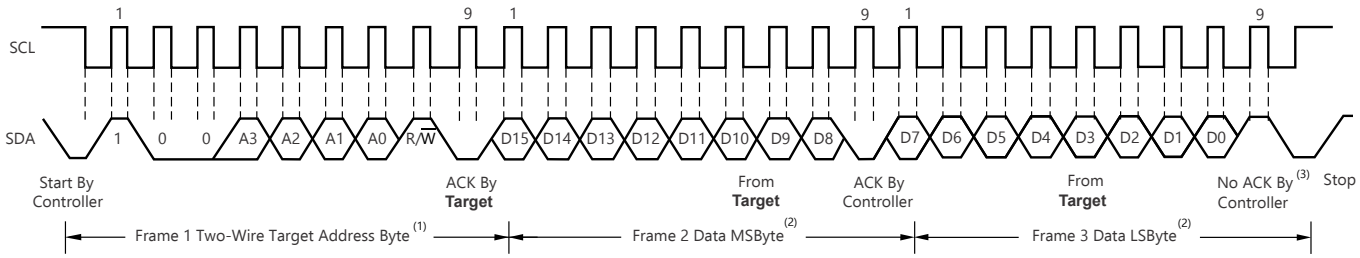
Register bytes are sent most-significant byte first, followed by the least significant byte.



(1) The value of the Target Address byte is determined by the setting of the address pins. Refer to Table 8-2.

(2) The device does not support packet error checking (PEC) or perform clock stretching.

Figure 8-4. Timing Diagram for Write Word Format



(1) The value of the Target Address byte is determined by the setting of the address pins. Refer to Table 8-2.

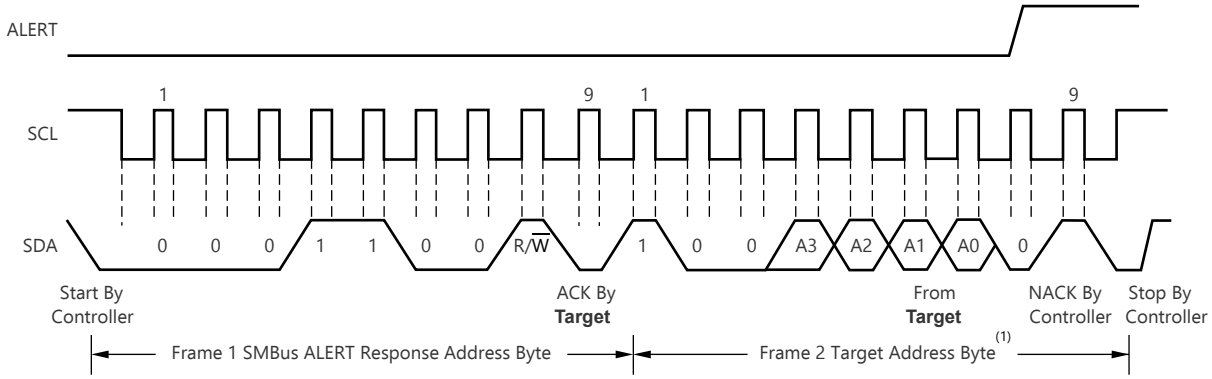
(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 8-7.

(3) ACK by the controller can also be sent.

(4) The device does not support packet error checking (PEC) or perform clock stretching.

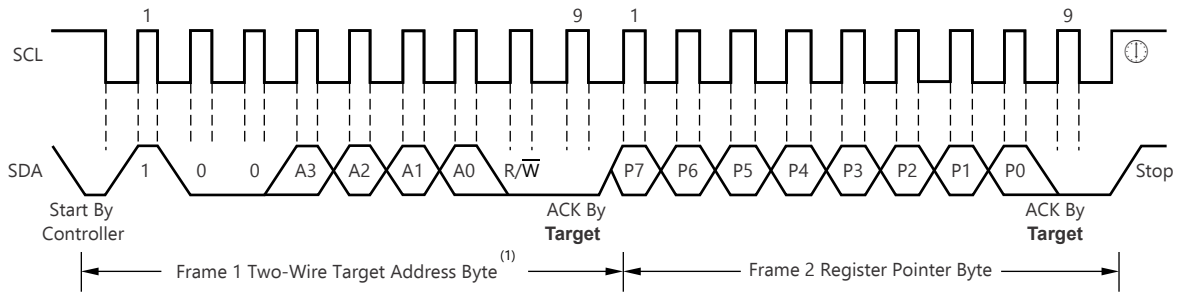
Figure 8-5. Timing Diagram for Read Word Format

Figure 8-6 shows the timing diagram for the SMBus Alert response operation. Figure 8-7 shows a typical register pointer configuration.



(1) The value of the Target Address byte is determined by the setting of the address pins. Refer to Table 8-2.

Figure 8-6. Timing Diagram for SMBus ALERT



(1) The value of the Target Address byte is determined by the setting of the address pins. Refer to Table 8-2.

Figure 8-7. Typical Register Pointer Set

8.5.6.1 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup devices. The controller generates a start condition followed by a valid serial byte containing High-Speed (HS) controller code *00001XXX*. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The INA230 does not acknowledge the HS controller code, but does recognize it and switches its internal filters to support 3.4-MHz operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 MHz are allowed. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. A stop condition ends the HS mode and switches all the internal filters of the INA230 to support the F/S mode.

8.5.7 SMBus Alert Response

The INA230 is designed to respond to the SMBus alert response address. The SMBus alert response provides a quick fault identification for simple target devices. When an alert occurs, the controller can broadcast the alert response target address (0001 100) with the Read/Write bit set high. Following this alert response, any target devices that generated an alert identify themselves by acknowledging the alert response and sending their respective address on the bus.

The alert response can activate several different target devices simultaneously, similar to the I²C general call. If more than one target attempts to respond, bus arbitration rules apply. The losing device does not generate an acknowledge and continues to hold the ALERT line low until the interrupt is cleared.

8.6 Register Maps

The INA230 uses a bank of registers for holding configuration settings, measurement results, minimum and maximum limits, and status information. Table 8-3 summarizes the INA230 registers; refer to the *Functional Block Diagram* for an illustration of the registers.

All 16-bit INA230 registers are two 8-bit bytes through the I²C interface.

Table 8-3. Summary of Register Set

POINTER ADDRESS			POWER-ON RESET		
HEX	REGISTER NAME	FUNCTION	BINARY	HEX	TYPE(1)
00	Configuration	All-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode	01000001 00100111	4127	R/ W
01	Shunt Voltage	Shunt voltage measurement data	00000000 00000000	0000	R
02	Bus Voltage	Bus voltage measurement data	00000000 00000000	0000	R
03	Power(2)	Contains the value of the calculated power being delivered to the load.	00000000 00000000	0000	R

Table 8-3. Summary of Register Set (continued)

POINTER ADDRESS	REGISTER NAME	FUNCTION	POWER-ON RESET		TYPE(1)
HEX			BINARY	HEX	
04	Current(2)	Contains the value of the calculated current flowing through the shunt resistor.	00000000 00000000	0000	R
05	Calibration	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/ $\overline{W}$
06	Mask/Enable	Alert configuration and conversion ready flag	00000000 00000000	0000	R/ $\overline{W}$
07	Alert Limit	Contains the limit value to compare to the selected alert function.	00000000 00000000	0000	R/ $\overline{W}$
FF	Die ID	Contains unique die identification number.	ASCII	ASCII	R

(1) Type: R = read-only, R/ $\overline{W}$ = read/write.
(2) The Current register defaults to '0' because the Calibration register defaults to '0', yielding a zero current and power value until the Calibration register is programmed.

8.6.1 Configuration Register (00h, Read/Write)

Table 8-4. Configuration Register (00h, Read/Write) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	—	—	AVG2	AVG1	AVG0	V_{BUS}CT2	V_{BUS}CT1	V_{BUS}CT0	V_{SH}CT2	V_{SH}CT1	V_{SH}CT0	MODE3	MODE2	MODE1
POR VALUE	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1

The Configuration register settings control the operating modes for the INA230. This register controls the conversion time settings for both the shunt and bus voltage measurements, as well as the averaging mode used. The operating mode that controls which signals are selected to be measured is also programmed in the Configuration register.

The Configuration register can be read from at any time without impacting or affecting the device settings or a conversion in progress. Writing to the Configuration register halts any conversion in progress until the write sequence is complete, resulting in the start of a new conversion based on the new contents of the Configuration register. This feature prevents any uncertainty in the conditions used for the next completed conversion.

RST: **Reset Bit**

Bit 15 Setting this bit to '1' generates a system reset that is the same as a power-on reset; all registers are reset to default values. This bit self-clears.

AVG: **Averaging Mode**

Bits 9–11 Sets the number of samples that are collected and averaged together. *Table 8-5* summarizes the AVG bit settings and related number of averages for each bit.

8.6.2 AVG Bit Settings [11:9]

Table 8-5. AVG Bit Settings [11:9](1) Description

AVG2 (D11)	AVG1 (D10)	AVG0 (D9)	NUMBER OF AVERAGES
0	0	0	1
0	0	1	4
0	1	0	16
0	1	1	64
1	0	0	128
1	0	1	256

Table 8-5. AVG Bit Settings [11:9](1) Description (continued)

AVG2 (D11)	AVG1 (D10)	AVG0 (D9)	NUMBER OF AVERAGES
1	1	0	512
1	1	1	1024

(1) Shaded values are default.

V_{BUS} CT: **Bus Voltage Conversion Time**

Bits 6–8 Sets the conversion time for the bus voltage measurement. *Table 8-6* shows the V_{BUS} CT bit options and related conversion times for each bit.

8.6.3 V_{BUS} CT Bit Settings [8:6]

Table 8-6. V_{BUS} CT Bit Settings [8:6](1) Description

V_{BUS} CT2 (D8)	V_{BUS} CT1 (D7)	V_{BUS} CT0 (D6)	CONVERSION TIME
0	0	0	140 µs
0	0	1	204 µs
0	1	0	332 µs
0	1	1	588 µs
1	0	0	1.1 ms
1	0	1	2.116 ms
1	1	0	4.156 ms
1	1	1	8.244 ms

(1) Shaded values are default.

V_{SH} CT: **Shunt Voltage Conversion Time**

Bits 3–5 Sets the conversion time for the shunt voltage measurement. *Table 8-7* shows the V_{SH} CT bit options and related conversion times for each bit.

8.6.4 V_{SH} CT Bit Settings [5:3]

Table 8-7. V_{SH} CT Bit Settings [5:3](1) Description

V_{SH} CT2 (D5)	V_{SH} CT1 (D4)	V_{SH} CT0 (D3)	CONVERSION TIME
0	0	0	140 µs
0	0	1	204 µs
0	1	0	332 µs
0	1	1	588 µs
1	0	0	1.1 ms
1	0	1	2.116 ms
1	1	0	4.156 ms
1	1	1	8.244 ms

(1) Shaded values are default.

MODE: **Operating Mode**

Bits 0–2 Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in *Table 8-8*.

8.6.5 Mode Settings [2:0]

Table 8-8. Mode Settings [2:0](1) Description

MODE3 (D2)	MODE2 (D1)	MODE1 (D0)	MODE
0	0	0	Power-Down
0	0	1	Shunt Voltage, triggered
0	1	0	Bus Voltage, triggered
0	1	1	Shunt and Bus, triggered
1	0	0	Power-Down
1	0	1	Shunt Voltage, continuous
1	1	0	Bus Voltage, continuous
1	1	1	Shunt and Bus, continuous

(1) Shaded values are default.

8.6.6 Data Output Register

8.6.6.1 Shunt Voltage Register (01h, Read-Only)

The Shunt Voltage register stores the current shunt voltage reading, V_{SHUNT}. Negative numbers are represented in twos complement format. Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting the MSB = '1'.

Example: For a value of V_{SHUNT} = –80 mV:

1. Take the absolute value: 80 mV
2. Translate this number to a whole decimal number (80 mV ÷ 2.5 µV) = 32000
3. Convert this number to binary = 111 1101 0000 0000
4. Complement the binary result = 000 0010 1111 1111
5. Add '1' to the complement to create the twos complement result = 000 0011 0000 0000
6. Extend the sign and create the 16-bit word: 1000 0011 0000 0000 = 8300h

If averaging is enabled, this register displays the averaged value. Full-scale range = 81.9175 mV (decimal = 7FFF); LSB: 2.5 µV.

Table 8-9. Shunt Voltage Register (01h, Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.6.6.2 Bus Voltage Register (02h, Read-Only)(1)

The Bus Voltage register stores the most recent bus voltage reading, V_{BUS}.

If averaging is enabled, this register displays the averaged value. Full-scale range = 40.95875 V (decimal = 7FFF); LSB = 1.25 mV. Do not apply more than 36 V on the BUS pin.

Table 8-10. Bus Voltage Register (02h, Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	BD14	BD13	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) D15 is always zero because bus voltage can only be positive.

8.6.6.3 Power Register (03h, Read-Only)

If averaging is enabled, this register displays the averaged value.

Table 8-11. Power Register (03h, Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Power register LSB is internally programmed to equal 25 times the programmed value of the Current_LSB.

The Power register records power in watts by multiplying the decimal values of the current register with the decimal value of the bus voltage register according to Equation 4.

8.6.6.4 Current Register (04h, Read-Only)

If averaging is enabled, this register displays the averaged value.

Table 8-12. Current Register (04h, Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value of the Current register is calculated by multiplying the decimal value in the Shunt Voltage register with the decimal value of the Calibration register, according to Equation 3.

8.6.6.5 Calibration Register (05h, Read/Write)

This register provides the INA230 with the shunt resistor value that was present to create the measured differential voltage. This register also sets the resolution of the Current register. The Current register LSB and Power register LSB are set through the programming of this register. This register is also used for overall system calibration. See the *Section 8.5.1* for more information on programming this register.

Table 8-13. Calibration Register (05h, Read/Write) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.6.6.6 Mask/Enable Register (06h, Read/Write)

The Mask/Enable register selects the function that controls the ALERT pin, as well as how that pin functions. If multiple functions are enabled, the highest significant bit position alert function (D15:D11) takes priority and responds to the Alert Limit register.

Table 8-14. Mask/Enable Register (06h, Read/Write) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SOL	SUL	BOL	BUL	POL	CNVR	—	—	—	—	—	AFF	CVRF	OVF	APOL	LEN
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SOL: **Shunt Voltage Overvoltage**

Bit 15 Setting this bit high configures the ALERT pin to be asserted when the shunt voltage conversion exceeds the value in the Alert Limit register.

SUL: **Shunt Voltage Undervoltage**

Bit 14 Setting this bit high configures the ALERT pin to be asserted when the shunt voltage conversion drops below the value in the Alert Limit register.

BOL: **Bus Voltage Overvoltage**

Bit 13 — Setting this bit high configures the ALERT pin to be asserted when the bus voltage conversion exceeds the value in the Alert Limit register.

BUL: **Bus Voltage Undervoltage**

Bit 12 — Setting this bit high configures the ALERT pin to be asserted when the bus voltage conversion drops below the value in the Alert Limit register.

POL: **Over-Limit Power**

Bit 11 — Setting this bit high configures the ALERT pin to be asserted when the power calculation exceeds the value in the Alert Limit register.

CNVR: **Conversion Ready**

Bit 10 — Setting this bit high configures the ALERT pin to be asserted when the Conversion Ready Flag bit (CVRF, bit 3) is asserted, indicating that the device is ready for the next conversion.

AFF: **Alert Function Flag**

Bit 4 — Although only one alert function at a time can be monitored at the ALERT pin, the Conversion Ready bit (CNVR, bit 10) can also be enabled to assert the ALERT pin. Reading the Alert Function Flag bit after an alert can help determine if the alert function was the source of the alert.
When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared after the next conversion that does not result in an alert condition.

CVRF: **Conversion Ready Flag**

Bit 3 — Although the INA230 can be read at any time, and the data from the last conversion are available, this bit is provided to help coordinate single-shot or triggered conversions. This bit is set after all conversions, averaging, and multiplications are complete. This bit clears under the following conditions in single-shot mode:
1) Writing to the Configuration register (except for power-down or disable selections)
2.) Reading the Mask/Enable register

OVF: **Math Overflow Flag**

Bit 2 — This bit is set to '1' if an arithmetic operation results in an overflow error; it indicates that current and power data may be invalid.

APOL: **Alert Polarity**

Bit 1 — Configures the latching feature of the ALERT pin and the flag bits.
1 = Inverted (active-high open collector)
0 = Normal (active-low open collector) (default)

LEN: **Alert Latch Enable**

Bit 0 — Configures the latching feature of the ALERT pin and flag bits.
1 = Latch enabled
0 = Transparent (default)
When the Alert Latch Enable bit is set to Transparent mode, the ALERT pin and flag bits reset to their idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the ALERT pin and flag bits remain active following a fault until the Mask/Enable register has been read.

8.6.6.7 Alert Limit Register (07h, Read/Write)

The Alert Limit register contains the value used to compare to the register selected in the Mask/Enable register to determine if a limit has been exceeded.

Table 8-15. Register Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The INA230 measures the voltage developed across a current-sensing resistor (R_{SHUNT}) when current passes through it. The device also measures the bus supply voltage and can calculate power when calibrated. It comes with alert capability where the alert pin can be programmed to respond to a user-defined event or to a conversion ready notification. This design illustrates the ability of the alert pin to respond to a set threshold.

9.2 Typical Applications

9.2.1 High-Side Sensing Circuit Application

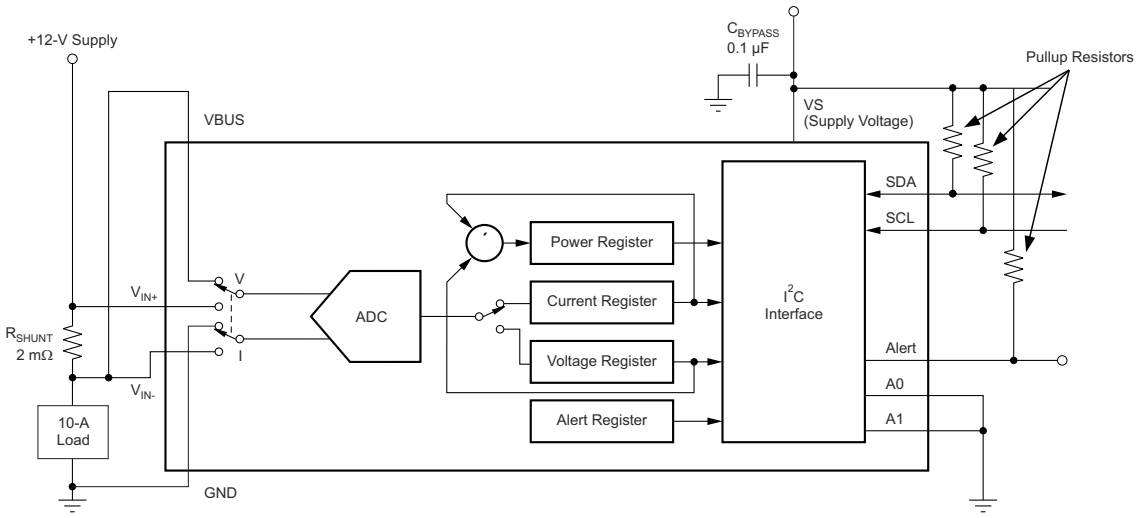


Figure 9-1. Typical Circuit Configuration, INA230

9.2.1.1 Design Requirements

Table 9-1 lists the design requirements for the circuit shown in Figure 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	3.3 V
Bus supply rail (V_{CM})	12 V
R_{SHUNT}	2 mΩ
Nominal Load Current	10 A
Overcurrent fault threshold	40 A

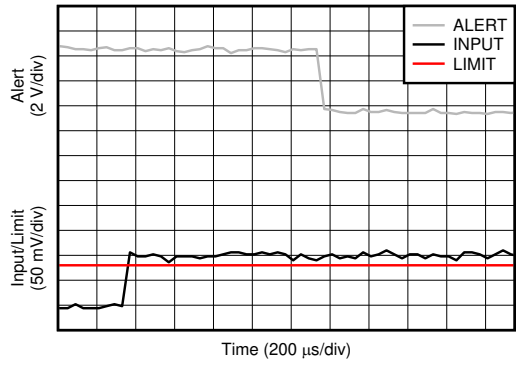
9.2.1.2 Detailed Design Procedure

The Alert pin can be configured to respond to one of the five alert functions described in the *Alert Pin* section. The alert pin must to be pulled up to the VS pin voltage through the pullup resistors. The configuration register is set based on the required conversion time and averaging. The Mask/Enable register is set to identify the required alert function and the Alert Limit register is set to the limit value used for comparison.

For this example the desired over current trip point is when the load current exceeds 40 A. To detect the over current condition the Mask/Enable register must to be configured to detect a shunt voltage over voltage condition. With a shunt resistor value of 2 mΩ the corresponding shunt voltage threshold is calculated to be 80 mV (2 mΩ × 40 A). Values for the Mask/Enable register and Alert Limit registers are shown in Section 9.2.1.3.

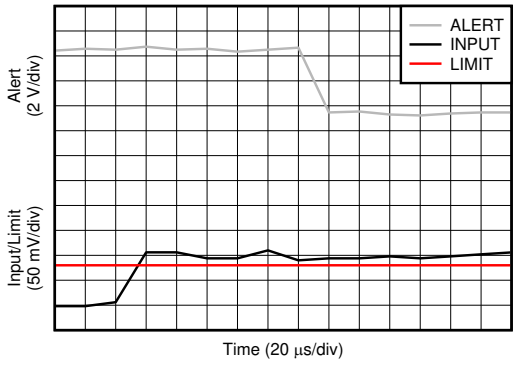
9.2.1.3 Application Curves

Figure 9-2 shows the Alert pin response to a shunt voltage over-limit of 80 mV for a conversion time (t_{CT}) of 1.1 ms and averaging set to 1. Figure 9-3 shows the response for the same limit but with the conversion time reduced to 140 µs.



See Table 9-2 t_{CT} = 1.1 ms
See Table 9-4 See Table 9-5

Figure 9-2. Alert Response



See Table 9-3 t_{CT} = 140 µs
See Table 9-4 See Table 9-5

Figure 9-3. Alert Response

Table 9-2. Configuration register (00h) Settings for Figure 9-2 (Value = 4025h)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	—	—	AVG2	AVG1	AVG0	VBUSCT 2	VBUSCT 1	VBUSCT 0	V_{SH}CT2	V_{SH}CT1	V_{SH}CT0	MODE3	MODE2	MODE1
VALUE	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1

Table 9-3. Configuration register (00h) Settings for Figure 9-3 (Value = 4005h)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	—	—	AVG2	AVG1	AVG0	VBUSCT 2	VBUSCT 1	VBUSCT 0	V_{SH}CT2	V_{SH}CT1	V_{SH}CT0	MODE3	MODE2	MODE1
VALUE	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Table 9-4. Mask/Enable register (06h) Settings for Figure 9-2 and Figure 9-3 (Value = 8000h)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SOL	SUL	BOL	BUL	POL	CNVR	—	—	—	—	—	AFF	CVRF	OVF	APOL	LEN
VALUE	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 9-5. Alert Limit register (07h) Settings for Figure 9-2 and Figure 9-3 (Value = 7D00)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
VALUE	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0

10 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power supply voltage, V_S. For example, the voltage applied to the VS pin can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as 36 V. Note also that the device can withstand the full 0-V to 36-V range at the input terminals, regardless of whether the device has power applied or not.

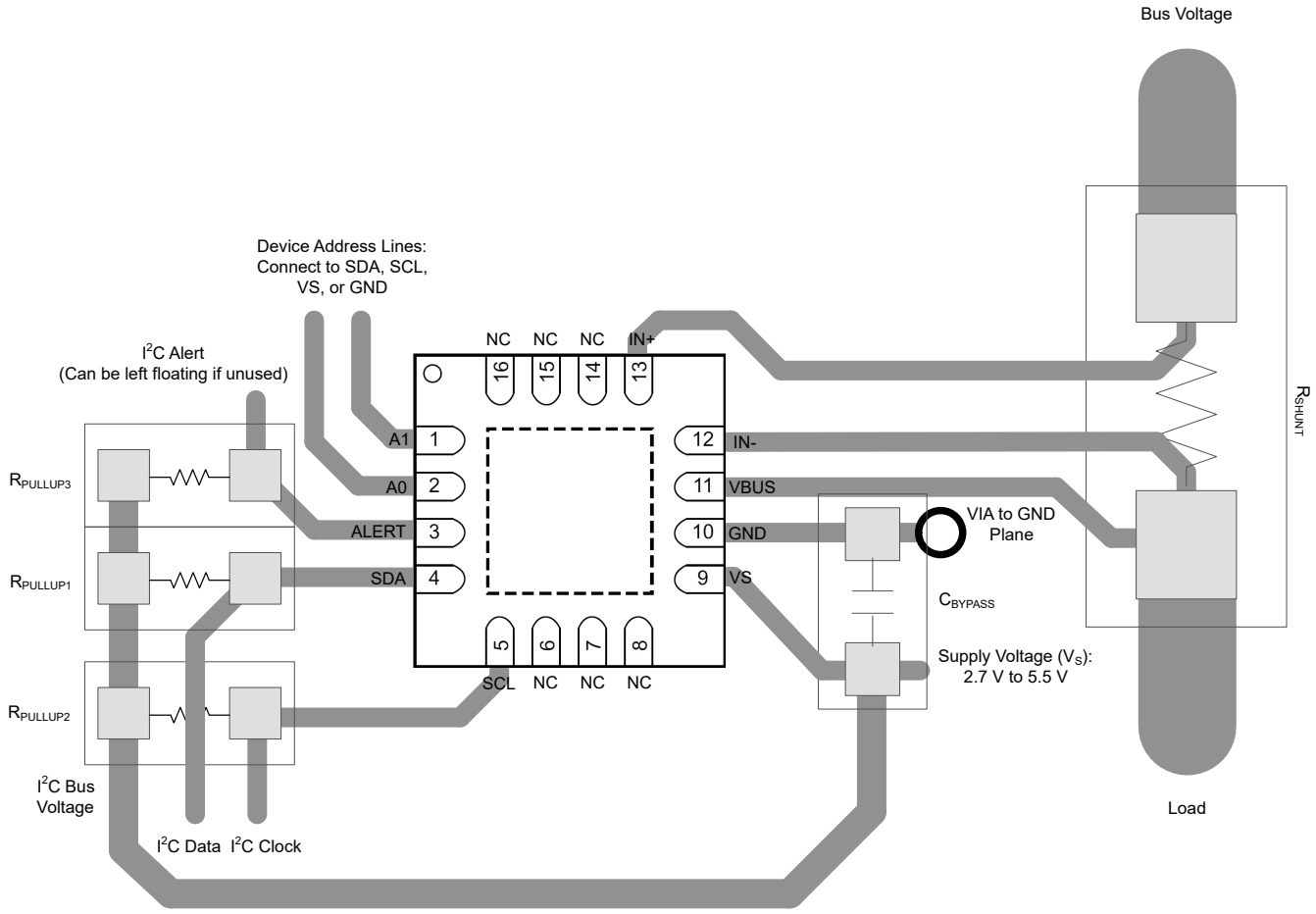
Place the required power-supply bypass capacitors as close to the supply and ground terminals of the device as possible to ensure stability. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

11 Layout

11.1 Layout Guidelines

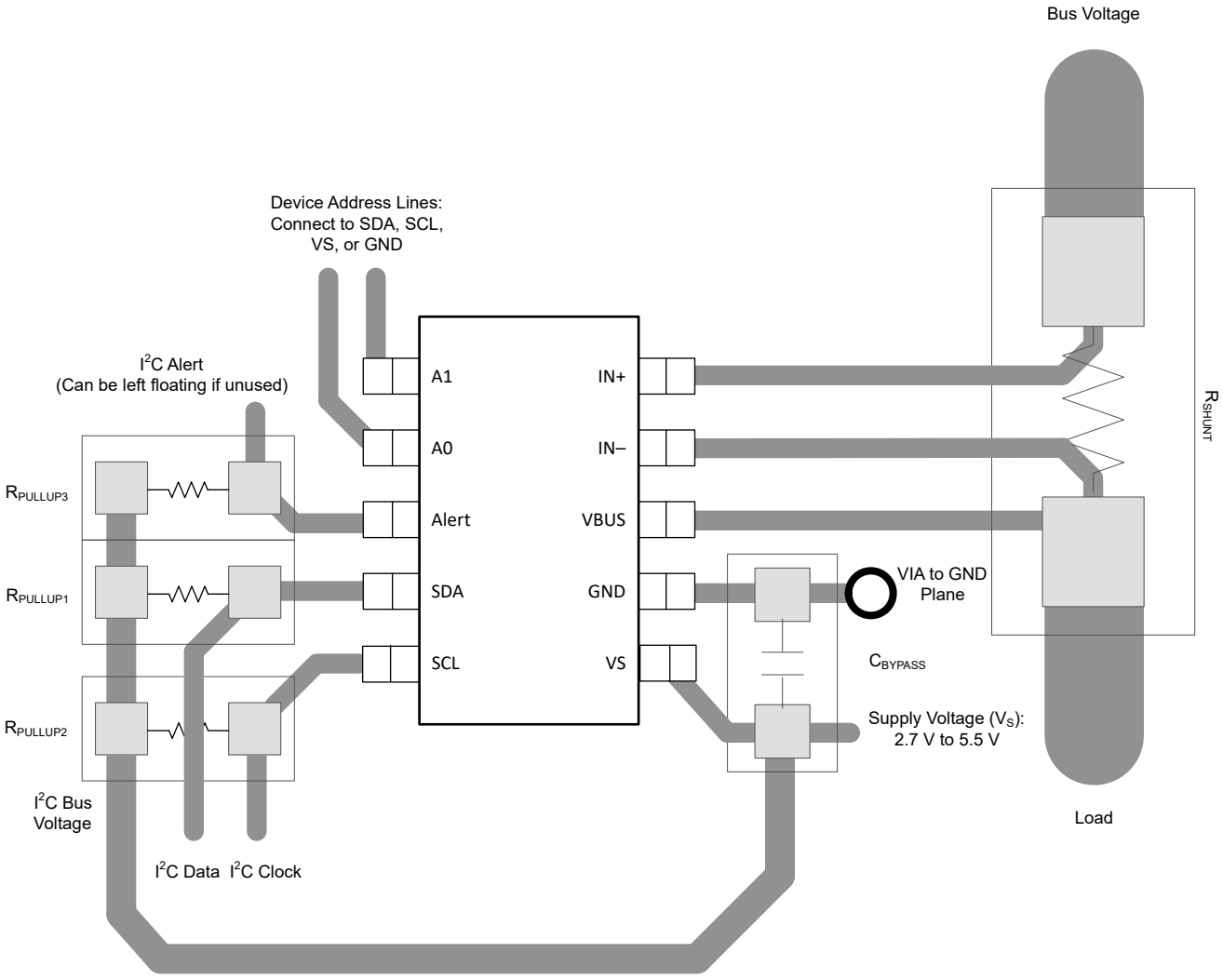
Connect the input pins (IN+ and IN–) to the sensing resistor using a Kelvin connection or a 4-wire connection. These connection techniques ensure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close to the supply and ground pins as possible.

11.2 Layout Example



(1) connect the VBUS pin to the power supply rail.

Figure 11-1. Layout Example (RGT Package)



(1) connect the VBUS pin to the power supply rail.

Figure 11-2. Layout Example (DGS Package)

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Transient Robustness for Current Shunt Monitors* reference design

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA230AIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2K5Q	Samples
INA230AIDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2K5Q	Samples
INA230AIRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I230	Samples
INA230AIRGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I230	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

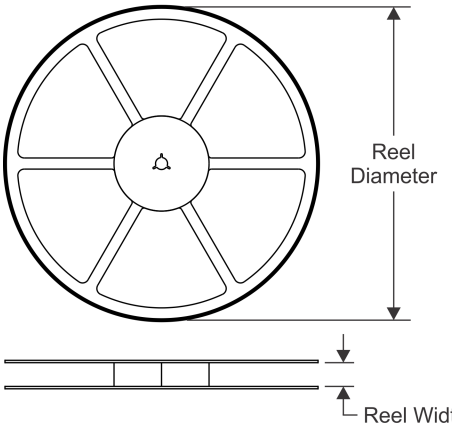
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

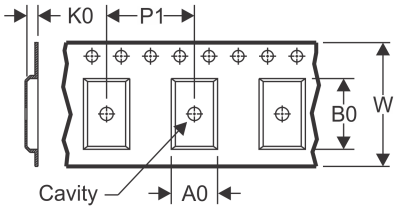
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

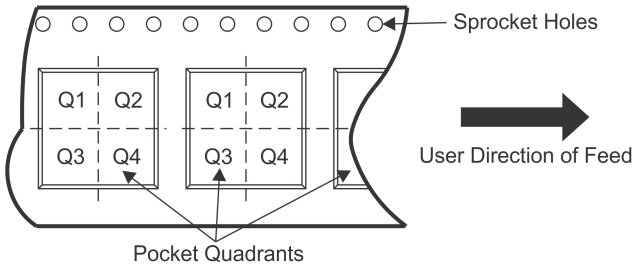


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

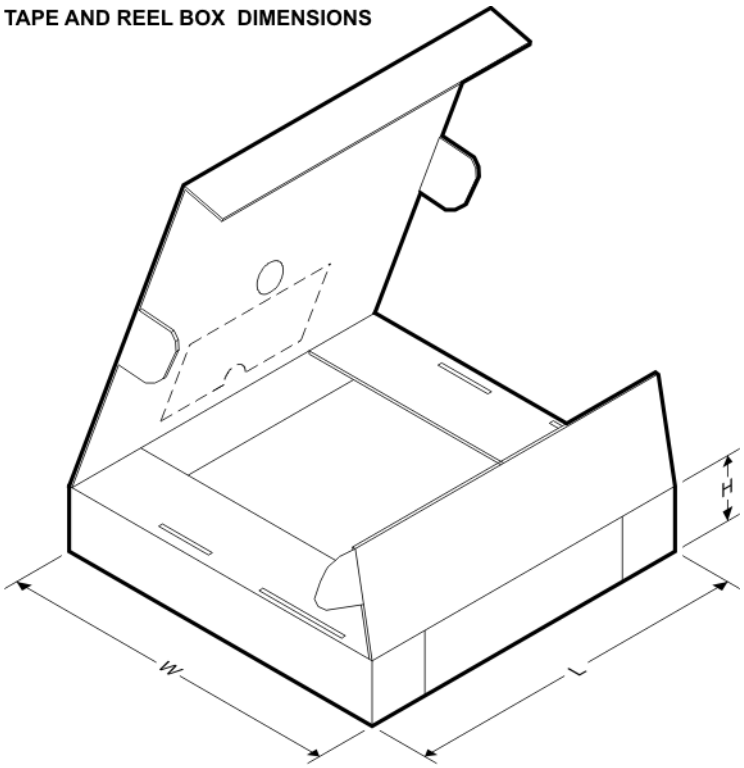
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA230AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA230AIDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA230AIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA230AIRGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

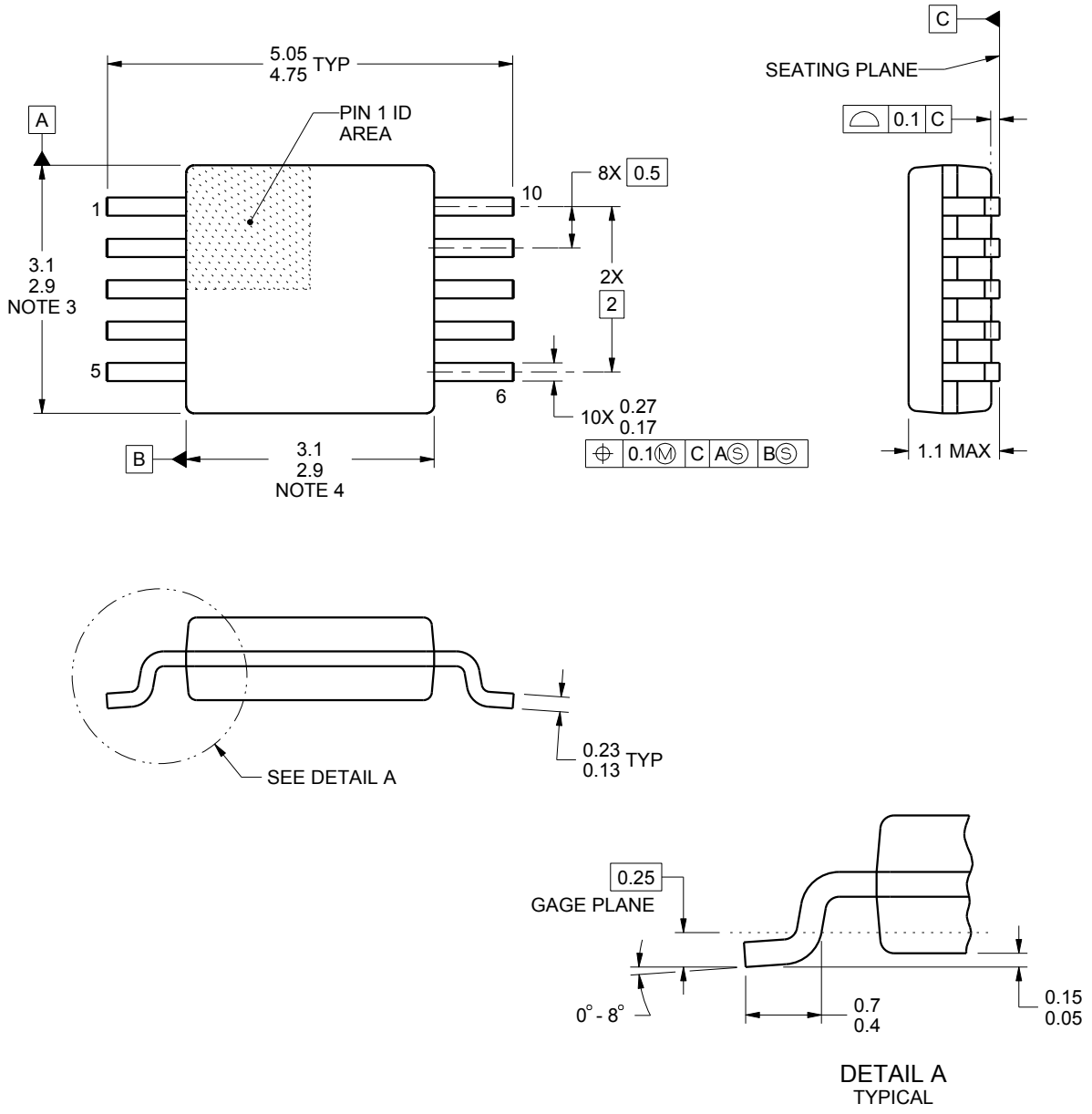
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA230AIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA230AIDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
INA230AIRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
INA230AIRGTT	VQFN	RGT	16	250	210.0	185.0	35.0

PACKAGE OUTLINE

DGS0010A

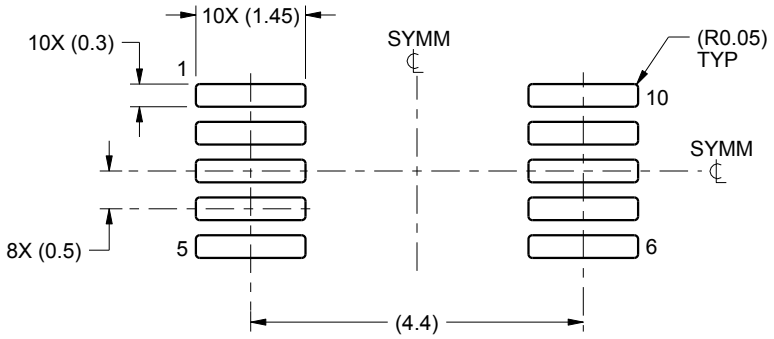
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

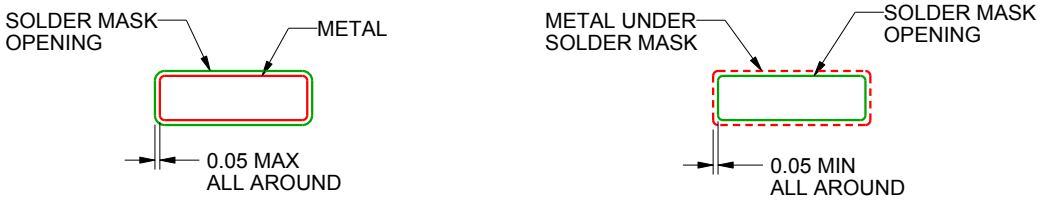


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

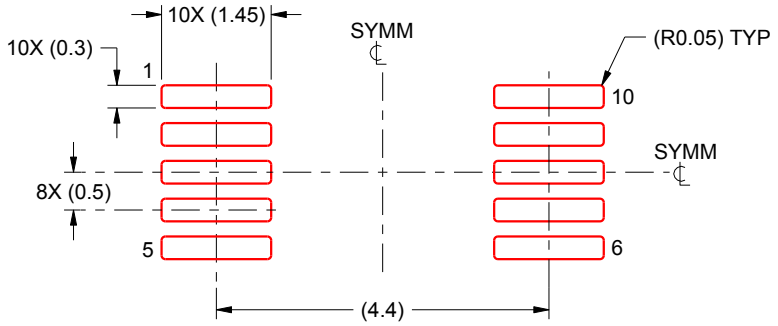


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

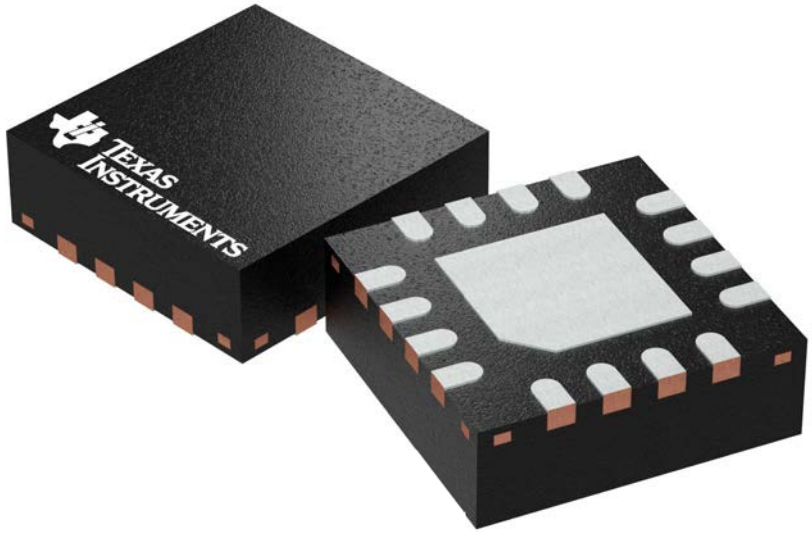
4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



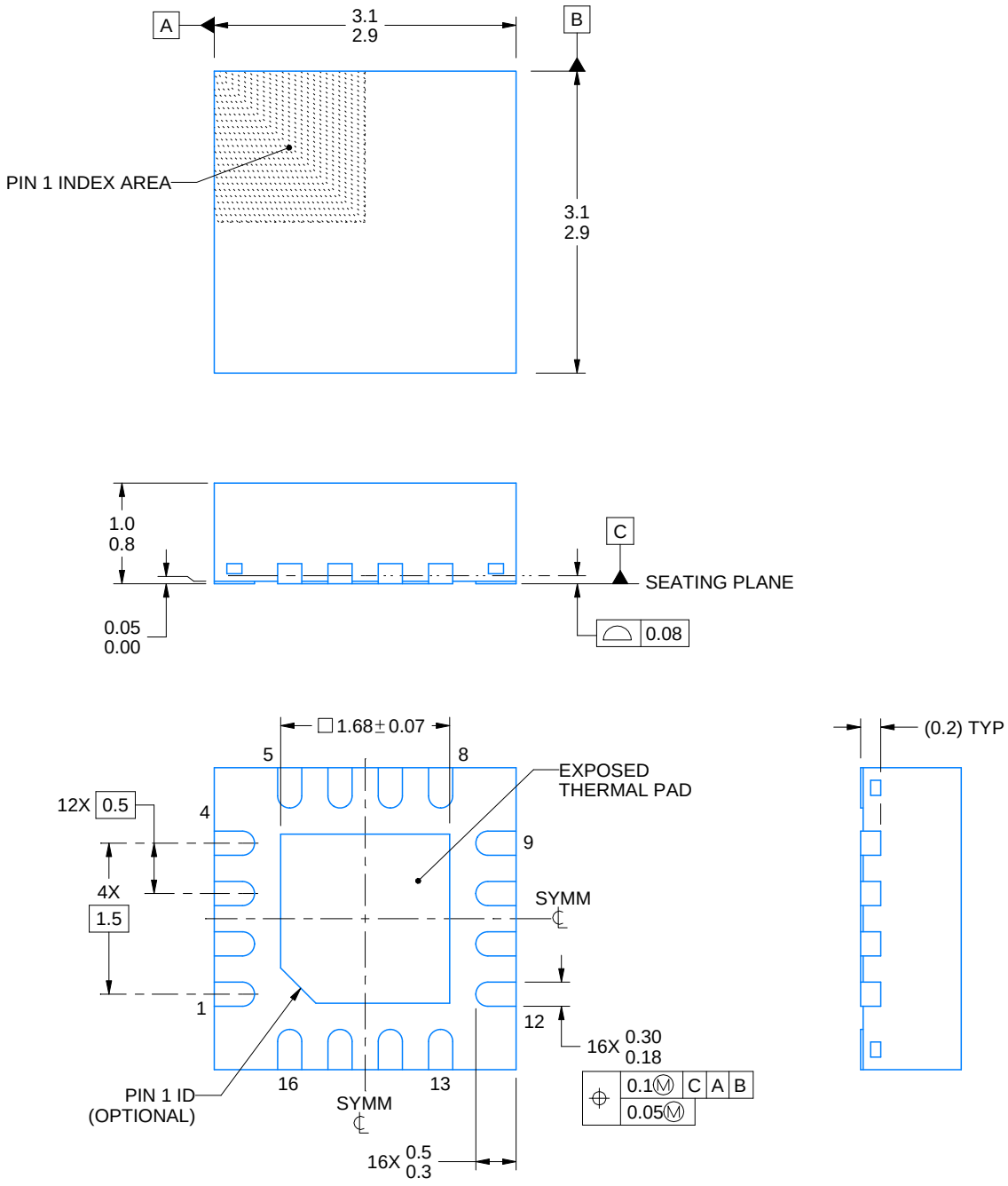
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016C

PACKAGE OUTLINE

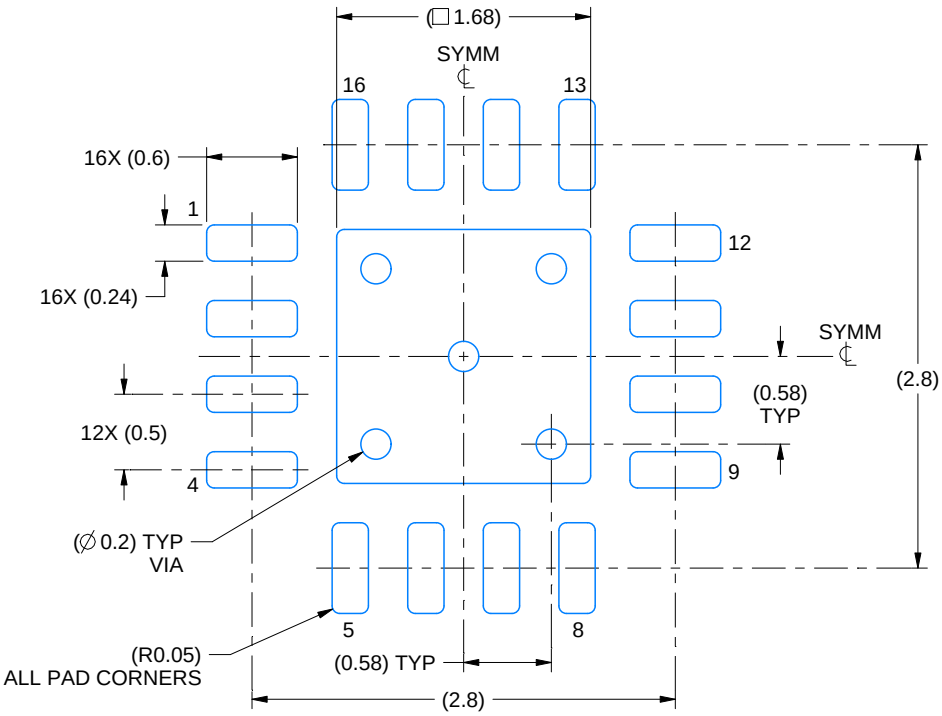
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

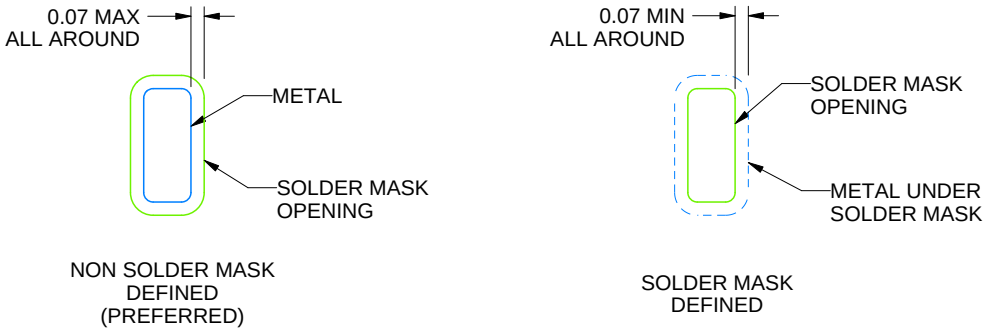


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

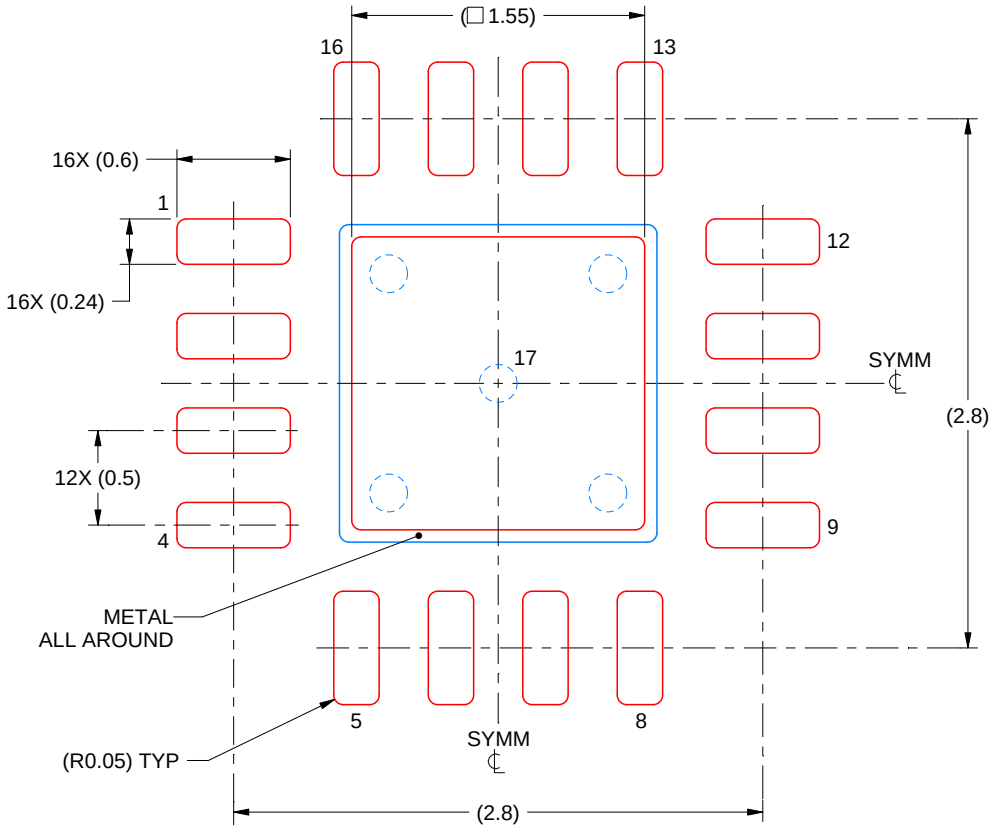


SOLDER MASK DETAILS

4222419/C 04/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/C 04/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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