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S32K1xx Product Brief

Supports all S32K1xx devices

Contents

1 S32K1xx Product Series

The S32K1xx Product Series further extends the highly scalable portfolio of ARM® Cortex®-M0+/M4F MCUs in the automotive industry. It builds on the legacy of the KEA series, whilst introducing higher memory options alongside a richer peripheral set extending capability into a variety of automotive applications. With a 2.7 –5.5 V supply and focus on automotive environment robustness, the S32K series devices are well suited to a wide range of applications in electrical harsh environments, and are optimized for cost-sensitive applications offering low pin-count options. The S32K series offers a broad range of memory, peripherals, and package options. They share common peripherals and pin counts allowing developers to migrate easily within an MCU family or among the MCU families to take advantage of more memory or feature integration. This scalability allows developers to standardize on the S32K series for their end product platforms, maximizing hardware and software reuse, and reducing time-to-market.

Following are the general features of the S32K series MCUs:

- 32-bit ARM Cortex-M0+/M4F core with IEEE-754 compliant FPU, executing up to 112 MHz
- Scalable memory footprints up to 2 MB flash and up to 256 KB SRAM
- Precision mixed-signal capability with on chip analog comparators and multiple 12-bit ADCs

- Powerful timers for a broad range of applications including motor control, lighting control, and body applications.
- Serial communication interfaces such as LPUART, LPSPI, LPI^{2}C, FlexCAN, ISO CAN-FD, FlexIO, etc.
- SHE+ specification compliant security module.
- Single power supply (2.7–5.5 V) with full functional flash program/erase/read operations.
- Functional safety compliance with ISO26262, with internal watchdog, voltage monitors, clock monitors, memory protection, ECC on memories, and cyclic redundancy checking.
- Ambient operation temperature range: –40 °C to 125°C.
- Software solutions: S32 Software Development Kit (SDK), S32 Design Studio (S32DS).
- The S32K series of devices are pin compatible within the same Product Series, allowing complete scalability.

2 Block diagram

The following figure shows the S32K1xx Product Series block diagram[1] :

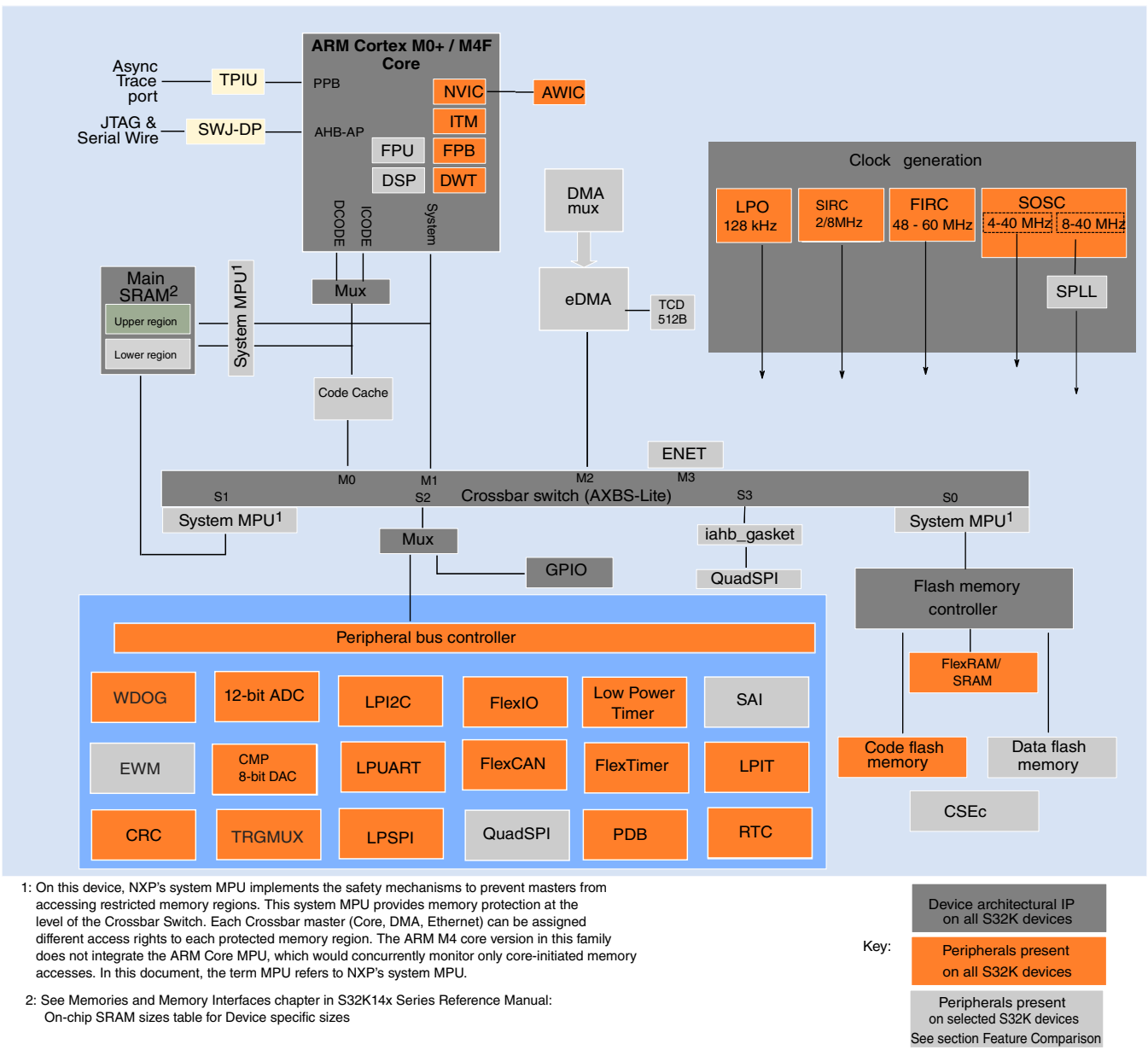

Figure 1. S32K1xx Product Series high-level architecture diagram

1. Please refer to the Feature comparison for Device specific values.

3 Features

3.1 Feature comparison

The following figure summarizes the memory and package options for the S32K product series and demonstrates where this device fits within the overall series. All devices which share a common package are pin-to-pin compatible.

		S32K11x		S32K14x			
	Parameter	K116	K118	K142	K144	K146	K148
System	Core	ARM® Cortex™-M0+		ARM® Cortex™-M4F			
	Frequency	48 MHz		up to 112 MHz			
	IEEE-754 FPU	o		●			
	HW security module (CSEc)	●		●			
	CRC module	1x		1x			
	ISO 26262	capable up to ASIL-B		capable up to ASIL-B			
	Peripheral speed	up to 60 MHz		up to 112 MHz			
	Crossbar	●		●			
	DMA	o		●			
	EWM	o		●			
	Memory protection unit	●		●			
	Watchdog	1x		1x			
	Real time clock	o		●			
	Low power modes	●		●			
	Number of I/Os	up to 42	up to 58	up to 89		up to 128	up to 156
	Single supply voltage	2.7 - 5.5 V		2.7 - 5.5 V			
	Operating temperature (T_a) Temperature ambient	-40 to +85ºC / +105ºC / +125ºC		-40 to +85ºC / +105ºC / +125ºC			
Memory	Flash	128 KB	256 KB	256 KB	512 KB	1 MB	2 MB
	Error correction code (ECC)	●		●			
	System RAM (including FlexRAM)	16 KB	24 KB	32 KB	64 KB	128 KB	256 KB
	FlexRAM (also available as system RAM)	2 KB		4 KB			
	Cache	o		4 KB			
	EEPROM emulated by FlexRAM	2 KB (up to 32 KB D-Flash)		4 KB (up to 64 KB D-Flash)			4 KB (up to 512 KB D-Flash)
	External memory interface	o		o			QuadSPI incl. HyperBus™
Timer	Low power interrupt timer	1x		1x			
	FlexTimer (16-bit counter) 8 channels	2x (16)		4x (32)		6x (48)	8x (64)
	Low power timer (LPTMR)	1x		1x			
	Real time counter (RTC)	1x		1x			
	Programmable delay block (PDB)	1x		2x			
Analog	Trigger mux (TRGMUX)	1x (16)		1x (64)		1x (73)	1x (81)
	12-bit SAR ADC (1 MSPS each)	1x (16)		2x (16)		2x (24)	2x (32)
	Comparator with 8-bit DAC	1x		1x			
Communication	100 Mbit IEEE-1588 ethernet MAC	o		o			1x
	Serial audio interface (AC97, TDM, I2S)	o		o			2x
	Low power UART/LIN	1x		2x	3x		
	Low power SPI	1x	2x	2x	3x		
	Low power I2C	1x		1x			2x
	FlexCAN (CAN-FD ISO/CD 11898-1)	1x (1x with FD)		2x (1x with FD)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		1x			
IDEs	Debug & trace	SWD, JTAG		SWD, JTAG (ITM, SWV, SWO)			SWD, JTAG (ITM, SWV, SWO),ETM
	Ecosystem (IDE, compiler, debugger)	NXP S32 Design Studio (GCC) + SDK, IAR, GHS, COSMIC, Lauterbach, iSystems		NXP S32 Design Studio (GCC) + SDK, IAR, GHS, COSMIC, Lauterbach, iSystems			
Other	Packages	QFN-32 LQFP-48	LQFP-48 LQFP-64	LQFP-64 LQFP-100	LQFP-64 LQFP-100 MAPBGA-100	MAPBGA-100 LQFP-100 LQFP-144	MAPBGA-100 LQFP-144 LQFP-176

LEGEND:
- o Not implemented.
- ● Available on the device.

Figure 2. S32K1xx product series comparison

3.2 Feature summary

The S32K1xx device series will have the following features:

Table 1. S32K1xx system peripherals

Core and Architecture S32K14x Devices(M4F Core)	• ARM Cortex M4F core running up to 80 MHz at 125 °C • ARM Core based on the ARMv7 Architecture & Thumb®-2 ISA with 1.25 DMIPS/MHz • 4 k data / instruction cache for optimizing wait state execution from memories • Single Precision Floating Point Unit (SPFPU), IEEE 754 compliant • Harvard bus architecture implementing dedicated instruction and data path • 3-stage pipeline with branch speculation • Integrated cross bar unit with System Memory Protection Unit (SMPU) • Integrated Digital Signal Processor (DSP) • Embedded Trace Macrocell supporting instruction trace (ETM) • ARM third-party ecosystem support: Software and tools to help minimize development time/cost • Optional high speed Run, further increasing frequency to 112 MHz
Core and Architecture S32K11x Devices(M0+ Core)	• ARM Cortex M0+ core running up to 48 MHz at 125 °C. • Single cycle 32 x 32 bits multiply • 2-stage pipeline for further reduced power consumption. • Serial Wire Debug (SWD) • Binary compatible instruction set with the ARM Cortex M4F
DMA	• 16 channel, extended up to 64 channel with DMA MUX
System and power management	• Low power ARM Cortex-M4F core with excellent energy efficiency • Supports multiple power modes: High speed Run (optional), Run, VLPR, VLPS (Very Low Power Stop) • Supports clock gating for unused modules, and specific peripherals remain working in low power modes • Fully independent CPU and peripheral clocking scheme • Rapid start-up from an internal independent 48 MHz Internal RC oscillator (FIRC) • Various low power oscillators such as the 128 kHz LPO and the 8 MHz Internal RC (SIRC) • Power management module (PMC) with low voltage detect (LVD) and selectable trip points • No output supply decoupling required • Programmable Low Voltage warning (LVW) system

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Table 1. S32K1xx system peripherals (continued)

	• POR / Reset • Support for multiple power modes • Non-maskable interrupt (NMI)
Memory and Memory Interfaces	• Upto 2 MB program flash, 512 K data flash / 4 KB EEPROM, up to 252 KB SRAM, all with ECC • up to 4 KB FlexRAM

Clocks	• External 8 MHz - 40 MHz crystal oscillator or resonator
	• Up to DC- 60 MHz external square wave input clock
	• Internal clock references
	  • 48 MHz FIRC, +/-1%
	  • 8 MHz SIRC, +/- 3%
	  • 128 kHz LPO +/- 10%
	• System Clock Generator (SCG), with in-built PLL

Security and integrity	• Cyclic Redundancy Check (CRC) generation module
	• External Watchdog Monitor (EWM)
	• HW Security Engine (CSEc)
	  • fully SHE/SHE+ and EVITA-Low specification compliant
	  • AES-128 hardware cipher block
	  • Secure Key storage
	  • Random number generator (TRNG and PRNG)
	  • 120-bit unique identification (UID) number

Safety ISO26262	• Windowed Watchdog (WDOG) with independent clock source • 120-bit unique identification (ID) number • FTTI of 100 ms • Voltage Monitors • Bandgap available as ADC input • Monitoring of external clock source using independent reference • PLL Lock and Loss of lock protection • System Memory Protection unit (SMPU) • ECC on code flash, data flash and system RAM • ADC self-test feature • Internal analog monitoring of all supplies available

Analog	• 12-bit analog-to-digital converter (ADCs)
	  • up to 64 external analog inputs
	  • with 1 µs conversion time
	  • internal bandgap reference channel, supporting automatic compare, optional hardware trigger and operating in Stop mode
	  • up to five internal reference inputs
	  • Automatic compare with interrupt
	  • Self-test and self-calibration scheme
	• Analog comparator (ACMP) with internal 8-bit digital-to-analog converter (DAC)

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Table 1. S32K1xx system peripherals (continued)

	• ACMP with both positive and negative inputs, separately selectable interrupt on rising and falling comparator output • Ability to cross trigger the timers from both the ADC and ACMP outputs

Timers	• 16-bit Flex Timers (FTM), offering up to 64 standard channels
	  • Input capture, output compare, and PWM modes
	  • Fault input support with global fault control
	  • Multiple features such as deadtime insertion, configurable polarity, quadrature decoding, etc
	• 16-bit Programmable Delay Blocks (PDB), offering extended triggering in electrical motor control applications
	• 32-bit low power interrupt timer (LPIT) with four channels, for RTOS task scheduler time base or trigger source for ADC conversion and timer modules
	• 16-bit Low Power Timer (LPTMR)
	• Advanced Motor Control using combination of ADC, FTM, and PDB

Communications	• Serial peripheral interfaces (LPSPI) with DMA support and low power availability. With full-duplex or single-wire bidirectional and master or slave mode. • Inter-integrated circuit (LPI^{2}C) modules with DMA support, low power availability, master / slave support, system management bus • Universal asynchronous receiver/transmitter (LPUART) modules with DMA support, with optional 13-bit break, full duplex non-return to zero (NRZ) and LIN 2.1 extension support and low power availability • FlexCAN modules (FlexCAN), many with ISO-CAN-FD, all with DMA support • Synchronous Audio Interface (SAI) capable of supporting stereo audio channels • ENET complex (10/100 Ethernet) that supports 1588 and MII/RMII,VLAN and DMA Timer
Human-machine interface	• Up to 152 GPIO pins, depending on package type • Each pin is programmable as rising edge or falling edge • Each I/O pin is configurable to have pull-up, pull-down or tristate capability • Up to 12 GPIO pins with high drive capability
Debug	• Serial wire JTAG debug Port (SWJ-DP), with 2 pin serial wire debug (SWD) for external debugger • Debug Watchpoint and Trace (DWT), with four configurable comparators as hardware watchpoints • Serial wire output (SWO)-synchronous trace data support

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Table 1. S32K1xx system peripherals (continued)

	• Instrumentation Trace Macrocell (ITM) with software and hardware trace, plus time stamping • Flash Patch and Breakpoints (FPB) with ability to patch code and data from code space to system space • Serial Wire Viewer (SWV): A trace capability providing displays of reads, writes, exceptions, PC Samples and printf.
I/O and package	• Up to 152 GPIO pins with interrupt functionality and wakeup capability • Up to 12 high drive pins of 20 mA capability • Up to 2 open-drain output pins supporting the LPI2C • Package options of 32-pin, 48-pin, 64-pin, 100-pin, 144-pin, 176-pin LQFP, and 100 MAPBGA

4 Applications

Following table provides the applications available across devices in S32K1xx product series.

Table 2. S32K1xx Applications

Applications	K116	K118	K142	K144	K146	K148
Touch Interface	Available					
Audio streaming	Not Available		Not Available			Available
Over the air update support[1]	Available					
BLDC/PMSM motor control	Not Available		Available			
Ethernet connected edge node with support for BroadR-Reach®	Not Available		Not Available			Available
Audio streaming over ethernet	Not Available		Not Available			Available
Secure data transmission over ethernet includes VLAN support and ISO CAN-FD with security engine support	Not Available					Available
Serial audio streaming (in and output) for radio, amplifier and microphone applications	Not Available					Available
Large 256 KB internal SRAM enabling usage of standard TCP/IP stacks	Not Available					Available
CAN to CAN or ethernet to CAN firewall	Not Available		Available			

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Table 2. S32K1xx Applications (continued)

Applications	K116	K118	K142	K144	K146	K148
External memory extension by a dedicated QuadSPI interface, e.g. for hand writing recognition applications	Not Available					Available
Human machine interface applications	Not Available		Available			

1. See S32K Architecture and Capabilities to Enable Over the Air Updates

5 Power modes

The power management controller (PMC) provides the user with multiple power options. The different modes of operation are supported to allow the user to optimize power consumption for the level of functionality needed.

The device supports Run, VLPR, Stop, and VLPS modes which are easy to use for customers both from the perspectives of different power consumption levels and functional requirement. In all power modes, all I/O states are maintained, all SRAM content is retained and all registers are retained. Depending on the device family member, high speed RUN is also supported.

NOTE

As an example, the supported Power Modes for S32K144 is provided in the table. The values are only indicative. For the actual detailed values on the S32K1xx Power Modes, please refer to the S32K1xx Data Sheet.

Table 3. S32K1xx Product Series power modes (At 25 °C)

Power Mode	Description	Target Typical Idd	Normal recover methods
High Speed Run	Allows increased maximum performance of device (if available)	37 mA	N/A
Run	Allows default maximum performance of device. CPU clocks can be run at full speed and the internal supply is fully regulated	26 mA	N/A
Stop	Places device in static state with the majority of peripherals able to continue operation. Voltage regulator is in standby.	250 µA	Interrupt
VLPR	Very Low Power RUN mode: CPU clocks can only be run at reduced speed using reduced power SIRC	TBD	N/A
VLPS	Very Low Power STOP mode: places device in static state with reduced peripheral availability: only LPTimer, RTC, CMP can be used	25 µA	wakeup

6 Revision History

The following table provides a revision history for this document.

Table 4. Revision History

Revision Number	Date	Substantial Changes
Rev. 1	10 Nov 2016	• Initial Release

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