

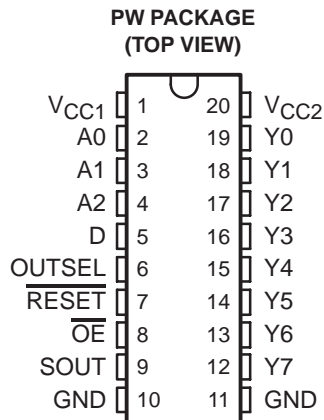
## DESCRIPTION

The SN74LV8153 is a serial-to-parallel data converter. It accepts serial input data and outputs 8-bit parallel data.

The automatic data-rate detection feature of the SN74LV8153 eliminates the need for an external oscillator and helps with cost and board real-estate savings.

The OUTSEL pin is used to choose between open collector and push-pull outputs. The open-collector option is suitable when this device is used in applications such as LED interface, where high drive current is required. SOUT is the output that acknowledges reception of the serial data.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC1}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



## FEATURES

- **Qualified for Automotive Applications**
- **Single-Wire Serial Data Input**
- **Compatible With UART Serial-Data Format**
- **Up to Eight Devices (64-Bit Parallel) Can Share the Same Bus by Using Different Combinations of A0, A1, A2**
- **Up to 40 mA Current Drive in Open-Collector Mode for Driving LEDs**
- **Outputs Can be Configured as Open-Collector or Push-Pull**
- **Internal Oscillator and Counter for Automatic Data-Rate Detection**
- **Output Levels Are Referenced to  $V_{CC2}$  and Can Be Configured From 3 V to 12 V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

## SUMMARY OF RECOMMENDED OPERATING CONDITIONS

PARAMETER	
$V_{CC1}$	3 V to 5.5 V
$V_{CC2}$	3 V to 13.2 V
$I_{OL}$	40 mA @ $V_{CC2} = 4.5$ V (open-collector mode)
$I_{OH}$	–24 mA @ $V_{CC2} = 12$ V (push-pull mode)
Maximum Data Rate	24 Kbps



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLE**  
 (each buffer)

INPUTS				OUTPUT Yn	OUTPUT STRUCTURE
OUTSEL	RESET	OE	Dn		
L	H	L	H	L	Open collector
L	H	L	L	H	
L	X	H	X	H	
L	L	X	X	H	
H	H	L	H	H	Push-pull
H	H	L	L	L	
H	X	H	X	Z	
H	L	L	X	L	

In the open-collector mode (OUTSEL = L), the outputs are inverted, e.g., Y1 = I, when D1 = H

**ORDERING INFORMATION†**

TA	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	TSSOP – PW	Tape and reel	SN74LV8153QPWRQ1	LV8153Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

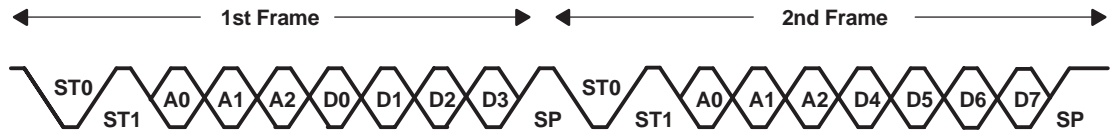
‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

**PIN DESCRIPTION**

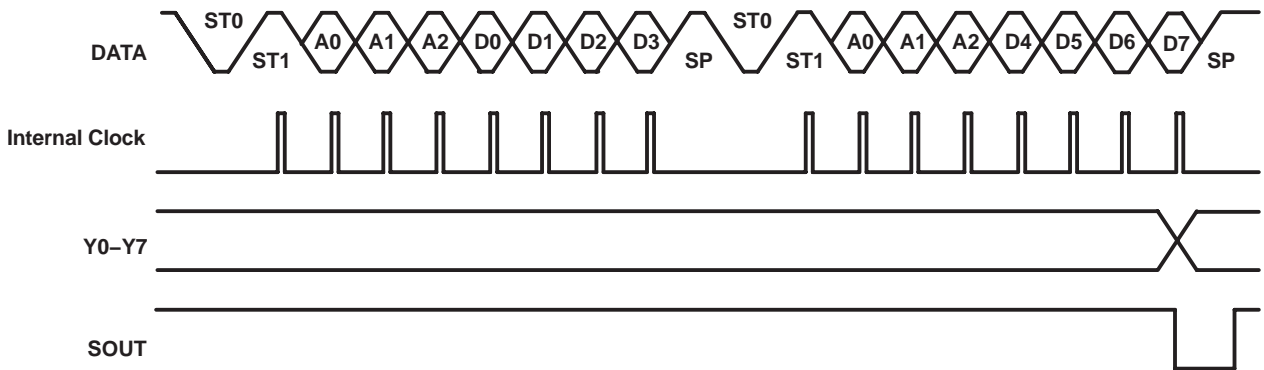
PIN #	PIN NAME	I/O	PIN FUNCTION
1	VCC1		Power-supply pin (all inputs and outputs except for Y0-Y7)
2-4	A0, A1, A2	In	The address pins are used to program the address of the device and allow up to eight devices to share the same bus.
5	D	In	Serial data input
6	OUTSEL	In	Choose between open-collector and push-pull type outputs (Y0-Y7).
7	RESET	In	Initialize register status
8	OE	In	Force Y0-Y7 to Hi-Z
9	SOUT	Out	Outputs a pulse when latch data is changed. Supplied by VCC1.
12-19	Y0-Y7	Out	Push-pull or open collector parallel data outputs. Supplied by VCC2.
20	VCC2		Power-supply pin for outputs (Y0-Y7). VCC2 can range from 3 V to 13.2 V.

**data transmission protocol**

- The serial data should be sent as 2START-3ADDRESS-4DATA-1STOP. Two consecutive serial-data frames transmit 8 bits of data. The first frame includes the lower four bits of data (D0-D3), and the second frame includes the upper four bits (D4-D7).
- The three address bits (in the consecutive frame) must be the same as those in the first frame; otherwise, the data will be dropped.
- The order of the two start bits must be 0, then 1 in any frame; otherwise, the data rate will not be detected correctly. The period between the falling edge of the first start bit (ST0) and the rising edge of the second start bit (ST1) is measured to generate an internal-clock synchronized data stream.



Example of Serial-Data Format

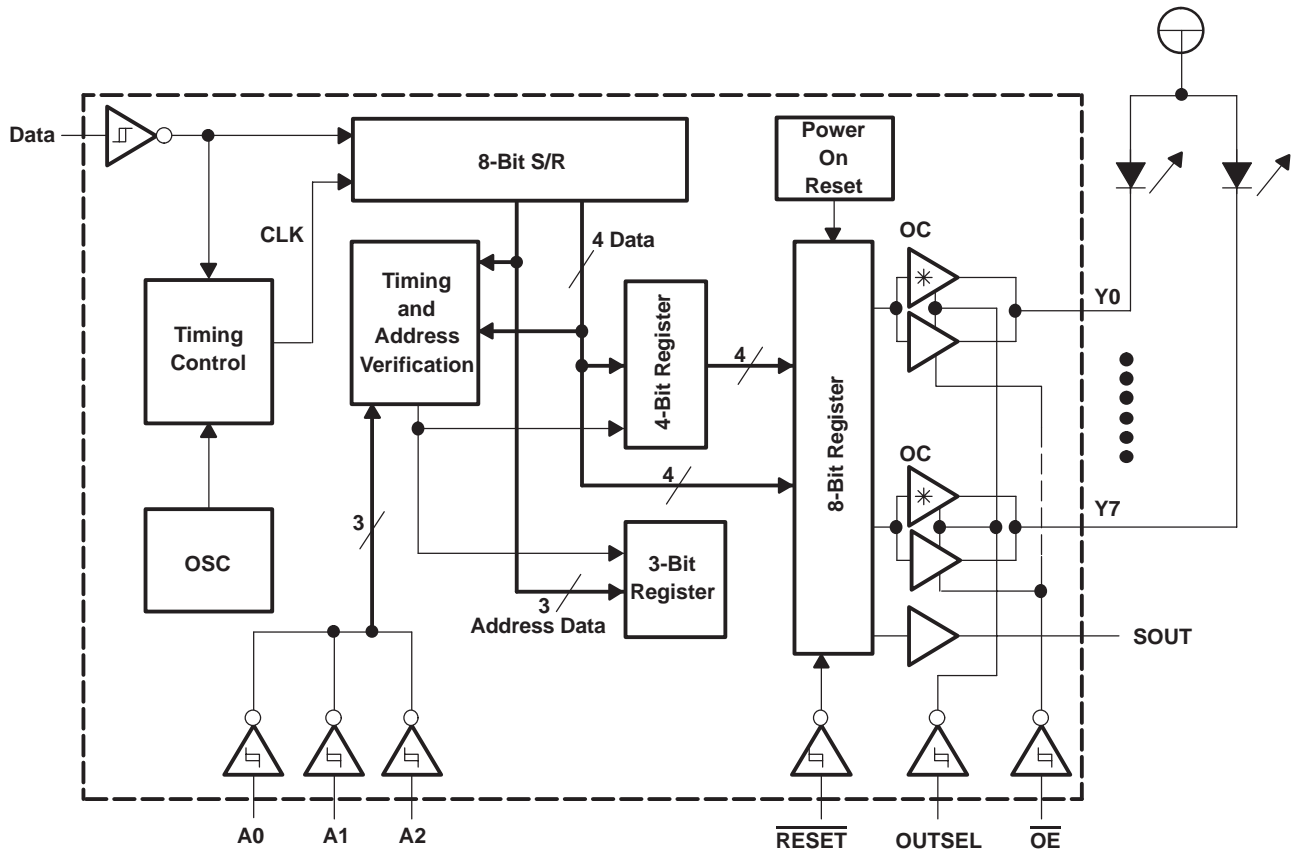


Timing Chart

(1) Internal clock cannot be observed.

(1) D0 is LSB and D7 is MSB. The data stream should be LSB first.

**logic diagram**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>**

Supply voltage range, $V_{CC1}$ .....	-0.5 V to 7 V
Supply voltage range, $V_{CC2}$ .....	-0.5 V to 14.5 V
Input voltage range, $V_I$ <sup>(2)</sup> .....	-0.5 V to 7 V
Voltage range applied to any output in the high or low state, $V_O$ (SOUT) <sup>(2)(3)</sup> .....	-0.5 V to $V_{CC1} + 0.5$ V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (SOUT) <sup>(2)</sup> .....	-0.5 V to 7 V
Voltage range, applied to any output in the high or low state, $V_O$ (Y0-Y7) <sup>(2)(3)</sup> .....	-0.5 V to $V_{CC2} + 0.5$ V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (Y0-Y7) <sup>(2)</sup> .....	-0.5 V to 14.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	25 mA
Continuous current, $I_O$ (OUTSEL = L, Y0-Y7 = L) .....	60 mA
Package thermal impedance, $\theta_{JA}$ <sup>(4)</sup> .....	83°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.  
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
(3) The value of  $V_{CC}$  is provided in the recommended operating condition table.  
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions<sup>(1)</sup>**

			V <sub>CC1</sub>	V <sub>CC2</sub>	MIN	MAX	UNIT
V <sub>CC1</sub>	Supply voltage				3	5.5	V
V <sub>CC2</sub>	Supply voltage				3	13.2	V
V <sub>IH</sub>	High-level input voltage		3 V	3 V	V <sub>CC</sub> × 0.7		V
			4.5 V	4.5 V	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage		3 V	3 V	V <sub>CC</sub> × 0.3		V
			4.5 V	4.5 V	V <sub>CC</sub> × 0.3		
V <sub>I</sub>	Input voltage				0	5.5	V
V <sub>O</sub>	Output voltage		4.5 V	4.5 V	0	5.5	V
				12 V	0	13.2	
I <sub>OH</sub>	Y <sub>n</sub>	OUTSEL = H	3 V	3 V	–2		mA
			4.5 V	4.5 V	–8		
			4.5 V	12 V	–24		
	SOUT		3 V	3 V	–4		mA
			4.5 V	4.5 V	–8		
I <sub>OL</sub>	Y <sub>n</sub>	OUTSEL = H	3 V	3 V	2		mA
			4.5 V	4.5 V	8		
		OUTSEL = L	3 V	3 V	20		
			4.5 V	4.5 V	40		
	SOUT		3 V	3 V	4		
			4.5 V	4.5 V	8		
T <sub>A</sub>	Operating free-air temperature				–40	125	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		VCC1	VCC2	MIN	TYP	MAX	UNIT
$V_{T+}$ Positive-going input threshold voltage	All inputs		3.3 V	3.3 V			2.31	V
			5 V	5 V			3.5	
$V_{T-}$ Negative-going input threshold voltage	All inputs		3.3 V	3.3 V	0.99			V
			5 V	5 V	1.5			
$\Delta V_T$ Hysteresis ( $V_{T+} - V_{T-}$ )	All inputs		3.3 V	3.3 V	0.33		1.32	V
			5 V	5 V	0.5		2	
$V_{OH}$	Yn	$I_{OH} = -2$ mA	3 V	3 V	2.38			V
		$I_{OH} = -8$ mA	4.5 V	4.5 V	3.8			
		$I_{OH} = -24$ mA	4.5 V	12 V	11			
	SOUT	$I_{OH} = -4$ mA	3 V	3 V	2.38			
		$I_{OH} = -8$ mA	4.5 V	4.5 V	3.8			
$V_{OL}$	Yn	$I_{OL} = 2$ mA (OUTSEL = H)	3 V	3 V			0.44	V
		$I_{OL} = 8$ mA (OUTSEL = H)	4.5 V	4.5 V			0.44	
		$I_{OL} = 40$ mA (OUTSEL = L)	4.5 V	4.5 V			0.5	
	SOUT	$I_{OL} = 4$ mA	3 V	3 V			0.44	
		$I_{OL} = 8$ mA	4.5 V	4.5 V			0.44	
$I_I$	$V_I = 5.5$ V or GND		0 to 5.5 V				$\pm 1$	$\mu$ A
$I_{OZ}$	$V_O = V_{CC}$ or GND (OUTSEL = H)		5.5 V	5.5 V			$\pm 5$	$\mu$ A
$I_{OH}$	$V_O = 12$ V (OUTSEL = L)		5.5 V	5.5 V			5	$\mu$ A
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	OUTSEL = H	5.5 V	5.5 V			5	mA
		OUTSEL = L					20	
$I_{off}$ (except SOUT)	$V_I$ or $V_O = 0$ to 5.5 V, $V_{CC} = 0$		0	0			$\pm 50$	$\mu$ A
$C_i$	$V_I = V_{CC}$ or GND		5 V	5 V			5	pF

**switching characteristics over recommended operating free-air temperature range,  $V_{CC1} = V_{CC2} = 3.3$  V  $\pm$  0.3 V (unless otherwise noted) (see Figures 1 and 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{pd}$	D7	Y	$C_L = 50$ pF		$P_w/2$	(1)			ns
	D7	SOUT			$P_w/2$	(1)			
	$\overline{\text{RESET}}$	Y						220	
	$\overline{\text{OE}}$ (2)	Y						220	
$t_{en}$	$\overline{\text{OE}}$ (3)	Y						220	ns
$t_{dis}$	$\overline{\text{OE}}$ (3)	Y						220	ns
$t_w$		SOUT			$P_w$	(4)			ns
Data rate						2	24	Kbps	

(1) The  $t_{pd}$  is dependent on the data pulse width ( $P_w$ ), and Y outputs are changed after one-half of  $P_w$ , because the internal clock is synchronized at the middle of the data pulse. Not tested, but specified by design.

(2) When outputs are open collector (OUTSEL = L)

(3) When outputs are push-pull (OUTSEL = H)

(4) SOUT goes low when the data is received correctly and maintains a low level for one data-pulse period. Not tested, but specified by design.

switching characteristics over recommended operating free-air temperature range,  $V_{CC1} = V_{CC2} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT	
				MIN	TYP	MAX				
$t_{pd}$	D7	Y	$C_L = 50\text{ pF}$		Pw/2	(1)			ns	
	D7	SOUT			Pw/2	(1)				
	$\overline{\text{RESET}}$	Y						200		
	$\overline{\text{OE}}(2)$	Y						200		
$t_{en}$	$\overline{\text{OE}}(3)$	Y						200	ns	
$t_{dis}$	$\overline{\text{OE}}(3)$	Y						200	ns	
$t_w$		SOUT				Pw	(4)			ns
Data rate								2	24	Kbps

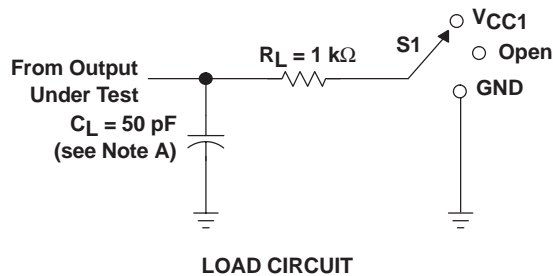
(1) The  $t_{pd}$  is dependent on the data pulse width (Pw), and Y outputs are changed after one-half of Pw, because the internal clock is synchronized at the middle of the data pulse. Not tested, but specified by design.

(2) When outputs are open collector (OUTSEL = L)

(3) When outputs are push-pull (OUTSEL = H)

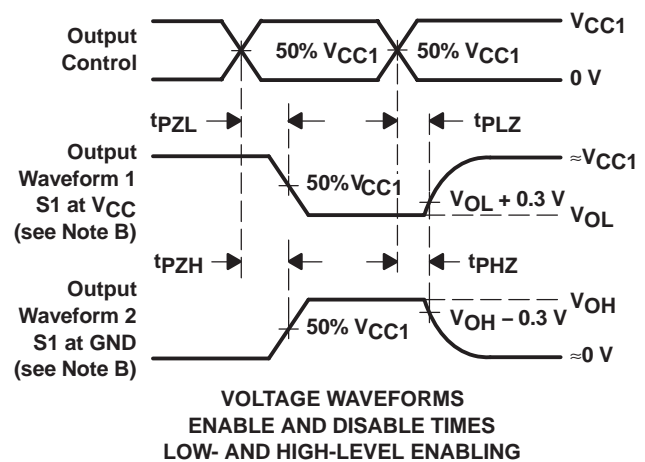
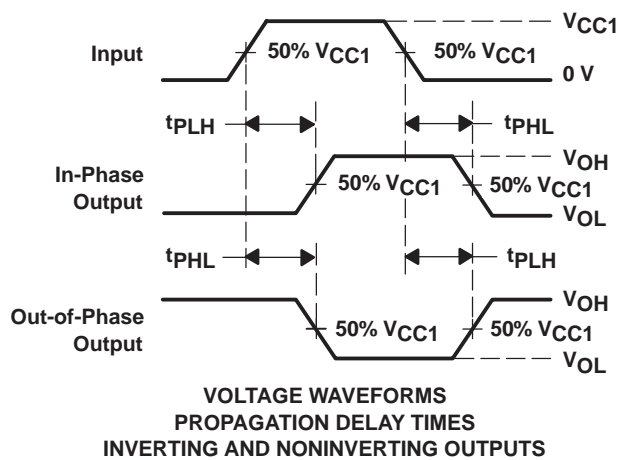
(4) SOUT goes low when the data is received correctly and maintains a low level for one data-pulse period. Not tested, but specified by design.

**PARAMETER MEASUREMENT INFORMATION**  
**(PUSH-PULL OUTPUT)**



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	VCC1
$t_{PHZ}/t_{PZH}$	GND

50% VCC1

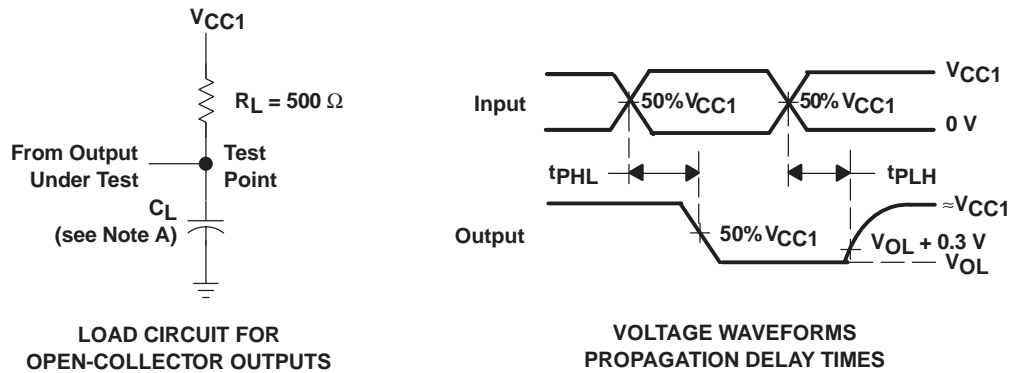


- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PZL}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**



**PARAMETER MEASUREMENT INFORMATION**  
**(OPEN-COLLECTOR OUTPUT)**



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - C. The outputs are measured one at a time, with one input transition per measurement.
  - D.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

**Figure 2. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV8153QPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV8153Q	<a href="#">Samples</a>
SN74LV8153QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV8153Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV8153-Q1 :**

- Catalog: [SN74LV8153](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV8153QPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV8153QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV8153QPWRG4Q1	TSSOP	PW	20	2000	853.0	449.0	35.0
SN74LV8153QPWRQ1	TSSOP	PW	20	2000	853.0	449.0	35.0

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated