TMP114 Ultra-Thin, 1.2-V to 1.8-V Supply, High Accuracy Digital Temperature Sensor with I²C Interface

1 Features

- High accuracy
  - TMP114:
    - ±0.3 °C maximum from –10 °C to 85 °C
    - ±0.5 °C maximum from –40 °C to 125 °C
  - TMP114N:
    - ±1 °C maximum from –40 °C to 125 °C
- Operating temperature range: –40 °C to 125 °C
- 16-bit resolution: 0.0078 °C (LSB)
- Low power consumption:
  - 0.7-µA average supply current
  - 0.16-µA shutdown current
- Supply range: 1.08 V to 1.98 V
- 1.2-V compatible logic inputs independent of supply voltage
- I²C and SMBus compatible interface
- 50-ns spike filter to coexist on I3C mixed bus
- Optional Cyclic Redundancy Check (CRC)
- 300-ms response time
- Adjustable averaging
- Adjustable conversion time and period
- Continuous or one-shot conversion mode
- Temperature alert status with hysteresis
- NIST traceability
- Ultra-thin 4-ball PicoStar (DSBGA) package with 0.15-mm height

2 Applications

- Mobile phones
- Solid state drives (SSDs)
- Wearable fitness & activity monitors
- Portable electronics
- Set-top boxes (STBs)
- Notebooks
- IP Camera
- Digital Still Camera

3 Description

The TMP114 is a high accuracy, I²C-compatible digital temperature sensor in an ultra-thin (0.15 mm) 4-pin package. The small size and low height of the TMP114 package optimizes volume constrained systems and enables novel placement of the sensor under other surface mount components for the fastest and most accurate temperature measurement.

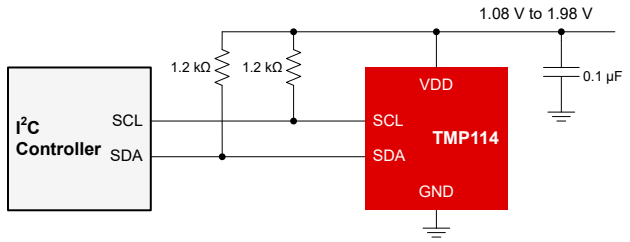
The TMP114 has an accuracy of ±0.3 °C and offers an on-chip 16-bit analog-to-digital converter (ADC) that provides a temperature resolution of 0.0078 °C. The TMP114 is 100% tested on a production setup that is NIST traceable.

To maximize battery life, the TMP114 is designed to operate from a supply voltage range of 1.08 V to 1.98 V, with a low average supply current of less than 0.7 µA.

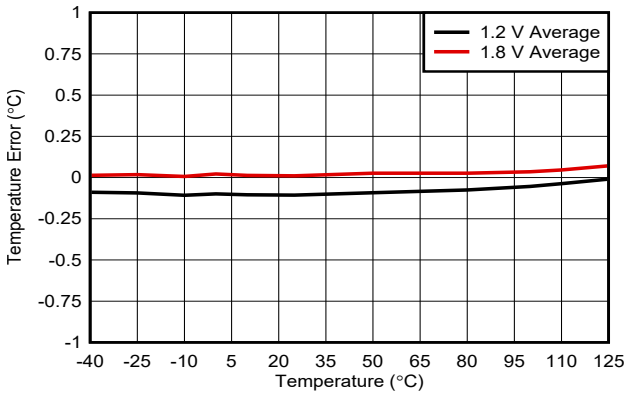
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TMP114	PicoStar (4)	0.758 mm × 0.758 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Schematic



Temperature Accuracy

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2022) to Revision C (May 2022)	Page
• Added new orderables to the *Device Comparison* table	3
• Added new orderables to the *Device Target Address* table	21

Changes from Revision A (September 2021) to Revision B (January 2022)	Page
• Changed TMP114N orderable status from Preview to Production Data	1
• Added TMP114NA to *Device Options* table	3
• Removed preview note for TMP114NB and TMP114NC	3
• Added TMP114NA to the *Device Target Address* table	21

Changes from Revision * (June 2021) to Revision A (September 2021)	Page
• Added TMP114N orderable preview information	1
• Changed the data sheet status from Advanced Information to Production Mixed	1
• Added *Device Options* table	3

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5 Device Comparison

Table 5-1. Device Options

PRODUCT	DEVICE ACCURACY	DEVICE TWO-WIRE ADDRESS
TMP114A	0.3 °C	1001000
TMP114B	0.3 °C	1001001
TMP114C	0.3 °C	1001010
TMP114D	0.3 °C	1001011
TMP114ND	1 °C	1001100
TMP114NC	1 °C	1001101
TMP114NB	1 °C	1001110
TMP114NA	1 °C	1001111

6 Pin Configuration and Functions

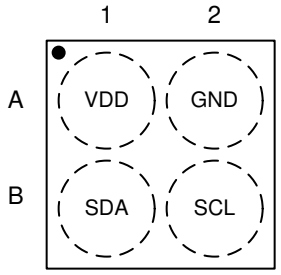

Figure 6-1. YMT Package 4-Pin PicoStar Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	A1	I	Supply voltage
GND	A2	—	Ground
SDA	B1	IO	Serial data input and open-drain output. Requires a pullup resistor
SCL	B2	I	Serial clock

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply, V_{DD}	-0.3	2.1	V
Input voltage SCL, SDA	-0.3	2.1	V
Output sink current SDA		15	mA
Junction temperature, T_J	-55	150	°C
Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DD}	1.08		1.98	V
I/O Voltage	SCL, SDA	0		1.98	V
I_{OL}	SDA	0		3	mA
Operating free-air temperature, T_A		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TMP114 YMT 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance	–	°C/W
M_T	Thermal mass	0.16	mJ/°C

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

Over free-air temperature range and V_{DD} = 1.08 V to 1.98 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 1.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
T_{ERR} (1)	Temperature Accuracy TMP114	Active Conversion time = 6.4 ms	T_A = -10 °C to 80 °C V_{DD} = 1.8 V	-0.3		0.3	°C
			T_A = -40 °C to 125 °C	-0.5		0.5	
	Temperature Accuracy TMP114N		T_A = -40 °C to 125 °C	-1		1	
T_{RES}	Temperature resolution	Including sign bit			16		Bits
		LSB			7.8125		m°C
PSR	DC power supply rejection	One-shot mode			0.17		°C/V
T_{REPEAT}	Repeatability(2)	V_{DD}= 1.2 V(3) T_A = 25 °C	Averaging off 6.4 ms conversion time		0.06		°C
T_{LTD}	Long-term drift(4)	1000 hours at 125 °C, 1.98 V			0.03		
t_{LIQUID}	Response Time (Stirred Liquid)	Single layer Flex PCB 0.2032 mm thickness	τ = 63% for step response from 25 °C to 75 °C		300		ms
		2-layer FR4 PCB 1.5748 mm thickness			980		
	Temperature cycling and hysteresis	T_{START} = -40 °C T_{FINISH} = 125 °C T_{TEST} = 25 °C 3 cycles			0.05		°C
t_{CONV}	Active conversion time	AVG = 0		5	6.4	7.5	ms
		AVG = 1		40	51.2	60	
t_{VAR}	Timing variation	Conversion Period Slew Rate Result Slew Rate Limit		-15		15	%
DIGITAL INPUT/OUTPUT							
C_{IN}	Input capacitance	f = 100 kHz			3	10	pF
V_{IH}	High-level input logic			0.84		1.98	V
V_{IL}	Low-level input logic			0		0.35	V
I_{IN}	Leakage input current			-0.2		0.2	µA
V_{OL}	Low-level output logic	SDA	I_{OL} = -2 mA	0	0.10	0.20	V

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Over free-air temperature range and V_{DD} = 1.08 V to 1.98 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 1.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD_ACTIVE}	Supply current during active conversion	Serial bus inactive	T_A = 25 °C		68	110	µA
			T_A = -40 °C to 125 °C			150	
I_{DD}	Average current consumption	Continuous Conversion cycle = 1 Hz Serial bus inactive AVG = 0	T_A = 25 °C		0.63	1.5	µA
			T_A = -40 °C to 125 °C			3.5	
		Continuous Conversion cycle = 1 Hz Serial bus inactive AVG = 1	T_A = 25 °C		3.5	6	
			T_A = -40 °C to 125 °C			8.5	
I_{SB}	Standby current	Continuous mode Serial bus inactive Between active conversions	T_A = 25 °C		0.26	0.7	µA
			T_A = -40 °C to 125 °C			3	
I_{SD}	Shutdown current	Serial bus inactive	T_A = 25 °C		0.16	0.5	uA
			T_A = -40 °C to 125 °C			2.5	
V_{POR}	Power supply thresholds		Supply rising, Power-on Reset		0.97		V
V_{BOR}	Power supply thresholds		Supply failing, Brown-out Detect		0.92		
t_{INIT}	Initialization time after Power-on Reset					1	ms
t_{RESET}	Reset recovery time		Soft Reset or General Call Reset			1	ms

(1) Temperature Accuracy guaranteed in both continuous conversion mode and one-shot mode with a conversion period greater than or equal to 31.25 ms. Averaging on or Averaging off.
(2) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(3) One-shot mode setup, 1 sample per minute for 24 hours.
(4) Long-term drift is determined using accelerated operational life testing at a junction temperature of 150°C. Temperature Cycling and Hysteresis effect is calculated out of final datasheet value.

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7.6 I²C Interface Timing

minimum and maximum specifications are over –40 °C to 125 °C and V_{DD} = 1.08 V to 1.98 V (unless otherwise noted)(1)

		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	1	400	1	1000	kHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	1.3		0.5		µs
$t_{(SUSTA)}$	Repeated START condition setup time	0.6		0.26		µs
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	0.6		0.26		µs
$t_{(SUSTO)}$	STOP condition setup time	0.6		0.26		µs
$t_{(HDDAT)}$	Data hold time(2)	12	900	12	150	ns
$t_{(SUDAT)}$	Data setup time	100		50		ns
$t_{(LOW)}$	SCL clock low period	1.3		0.5		µs
$t_{(HIGH)}$	SCL clock high period	0.6		0.26		µs
$t_{(VDAT)}$	Data valid time (data response time)(3)		0.9		0.45	µs
t_R	SDA, SCL rise time	20	300		120	ns
t_F	SDA, SCL fall time	20 x (V_{DD} / 5.5 V)	300	20 x (V_{DD} / 5.5 V)	120	ns
$t_{timeout}$	Timeout (SCL = GND or SDA = GND)	23	36	23	37	ms
t_{LPF}	Glitch suppression filter	50		50		ns

(1) The controller and device have the same V_{DD} value. Values are based on statistical analysis of samples tested during initial release.
(2) The maximum $t_{(HDDAT)}$ can be 0.9 µs for fast mode, and is less than the maximum $t_{(VDAT)}$ by a transition time.
(3) $t_{(VDAT)}$ = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

7.7 Two-Wire Timing Diagram

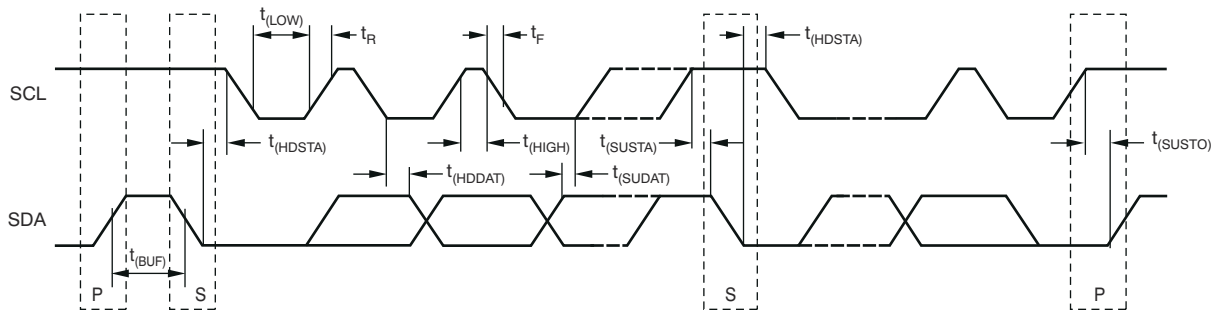
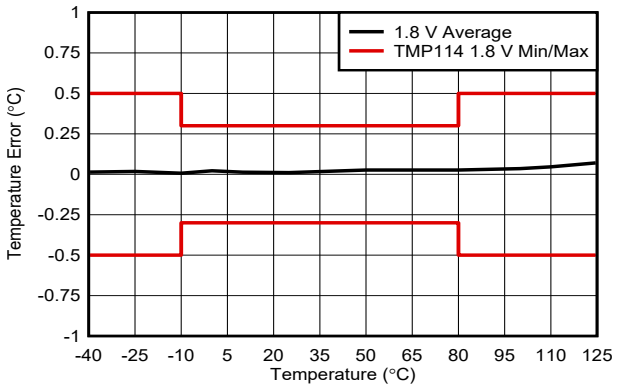


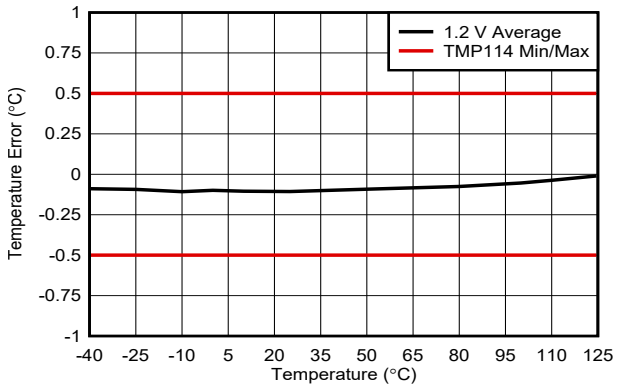
Figure 7-1. Two-Wire Timing Diagram

7.8 Typical Characteristics



V_{DD} = 1.8 V
Conversion Period 31.25 ms to 2 s
AVG = 0 or 8 Averages

Figure 7-2. Temperature Error vs. Temperature



V_{DD} = 1.2 V
Conversion Period 31.25 ms to 2 s
AVG = 0 or 8 Averages

Figure 7-3. Temperature Error vs. Temperature

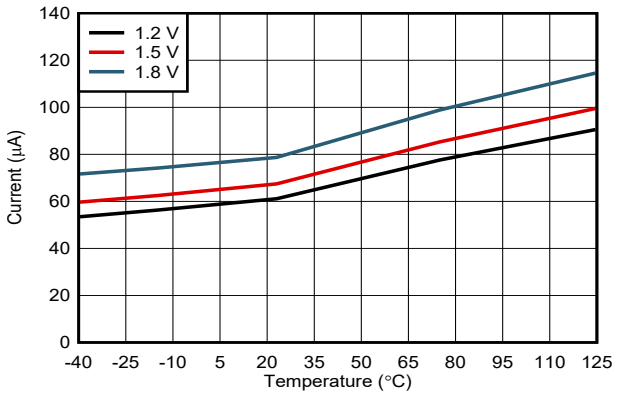


Figure 7-4. Active Current vs. Temperature

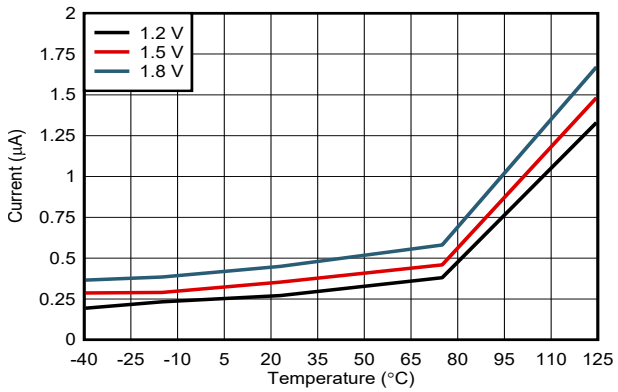


Figure 7-5. Standby Current vs. Temperature

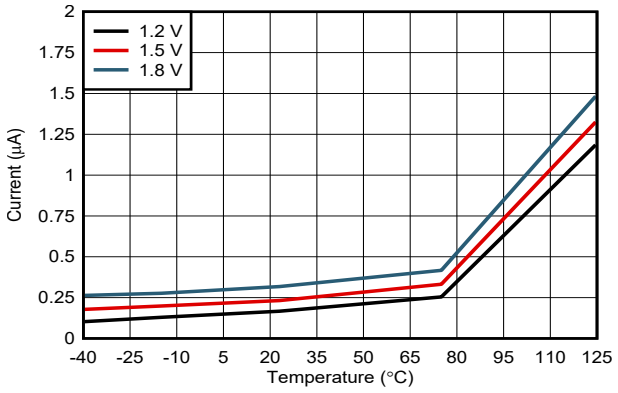
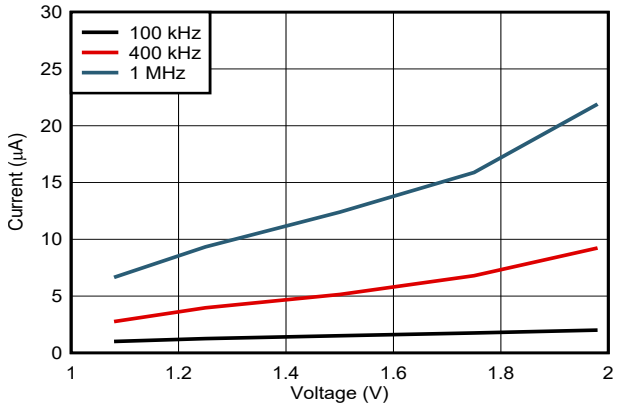


Figure 7-6. Shutdown Current vs. Temperature



T_A = –40 °C

Figure 7-7. Supply Current vs. V_{DD} With Toggling SCL

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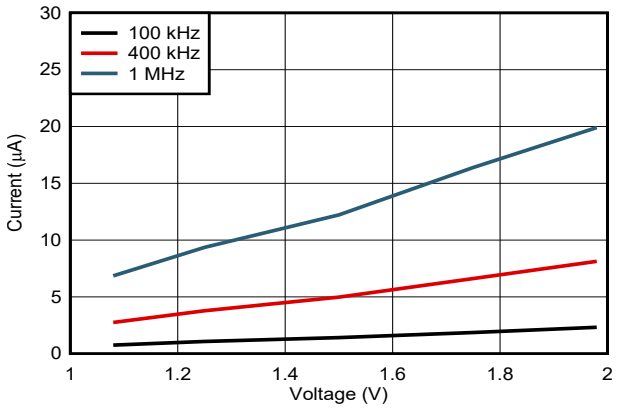
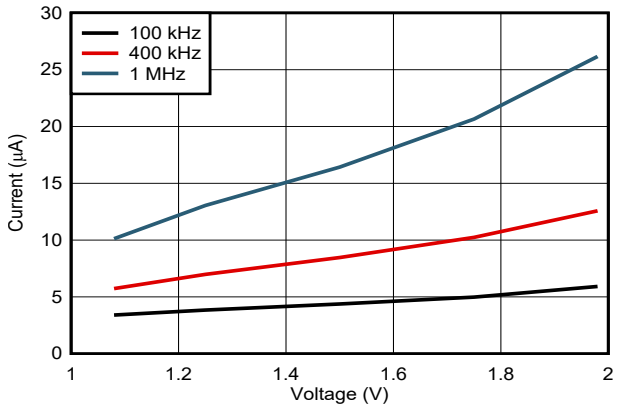
7.8 Typical Characteristics (continued)



T_A = 25 °C

Figure 7-8. Supply Current vs. V_{DD} With Toggling SCL



T_A = 125 °C

Figure 7-9. Supply Current vs. V_{DD} With Toggling SCL

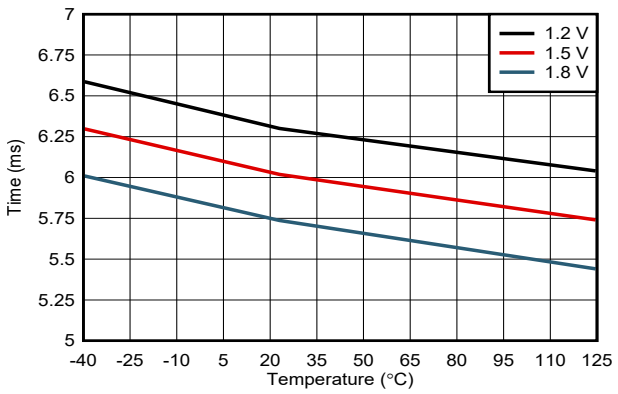


Figure 7-10. Conversion Time vs. Temperature

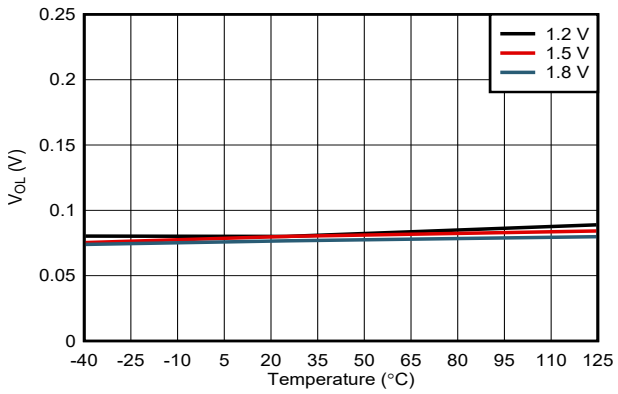
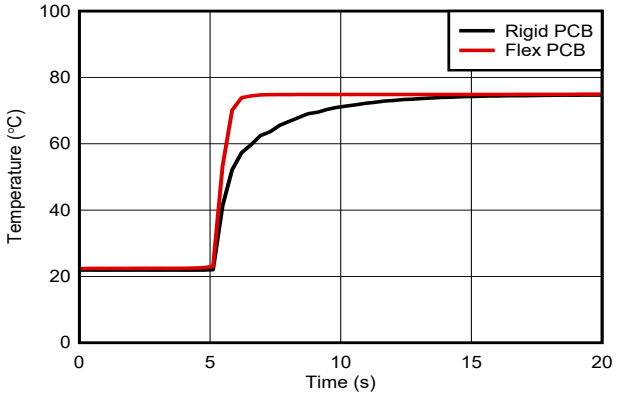
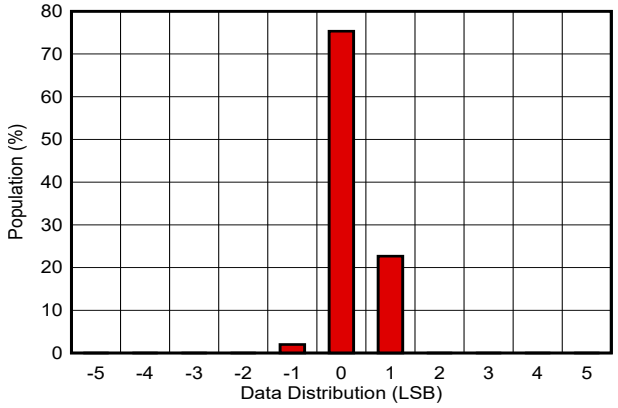


Figure 7-11. V_{OL} vs. Temperature



T_{START} = Room (25 °C), T_{FINISH} = 75 °C

Figure 7-12. Response Time



T_A = 25 °C

Figure 7-13. Data Distribution With 6.4-ms Conversion Time and Averaging On

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7.8 Typical Characteristics (continued)

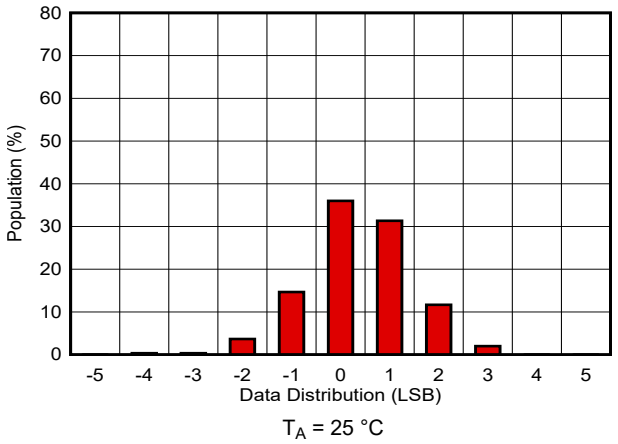

Figure 7-14. Data Distribution With 6.4-ms Conversion Time and Averaging Off

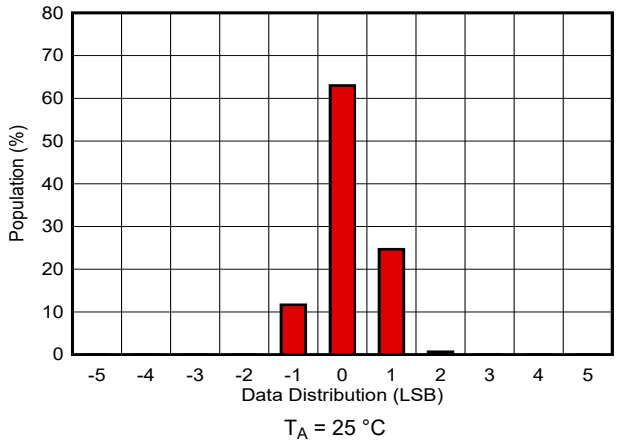

Figure 7-15. Data Distribution With 3.5-ms Conversion Time and Averaging On

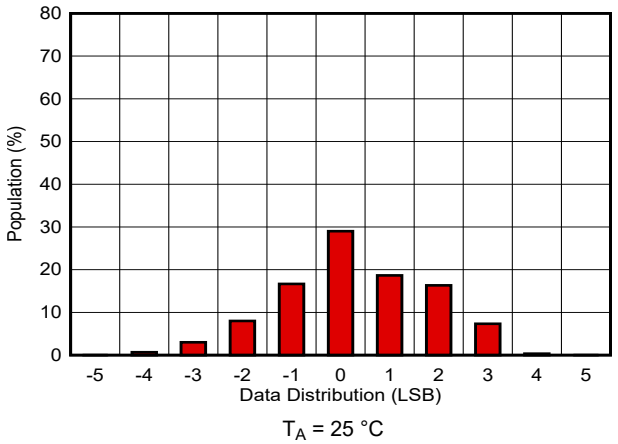

Figure 7-16. Data Distribution With 3.5-ms Conversion Time and Averaging Off

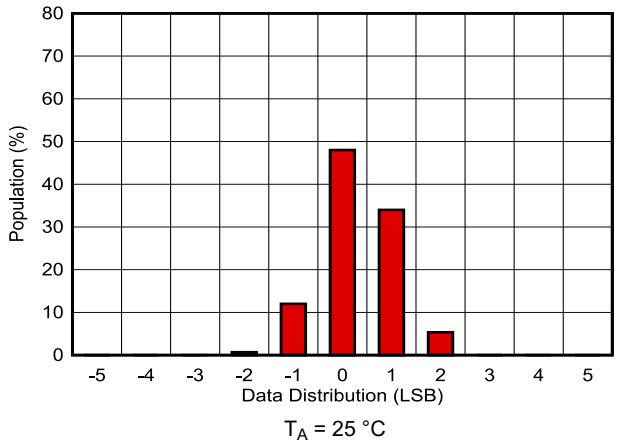

Figure 7-17. Data Distribution With 2-ms Conversion Time and Averaging On

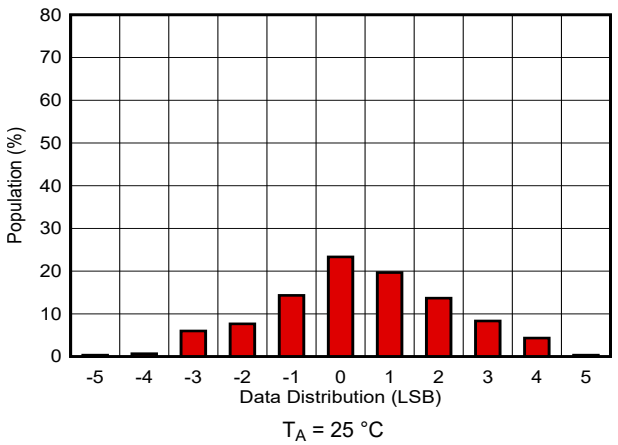

Figure 7-18. Data Distribution With 2-ms Conversion Time and Averaging Off

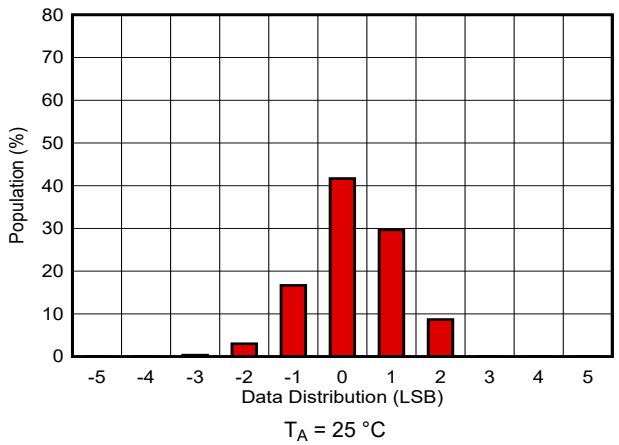

Figure 7-19. Data Distribution With 1.2-ms Conversion Time and Averaging On

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7.8 Typical Characteristics (continued)

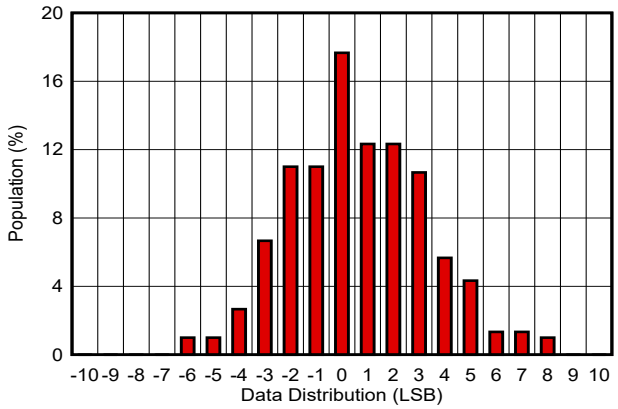


Figure 7-20. Data Distribution With 1.2-ms Conversion Time and Averaging Off

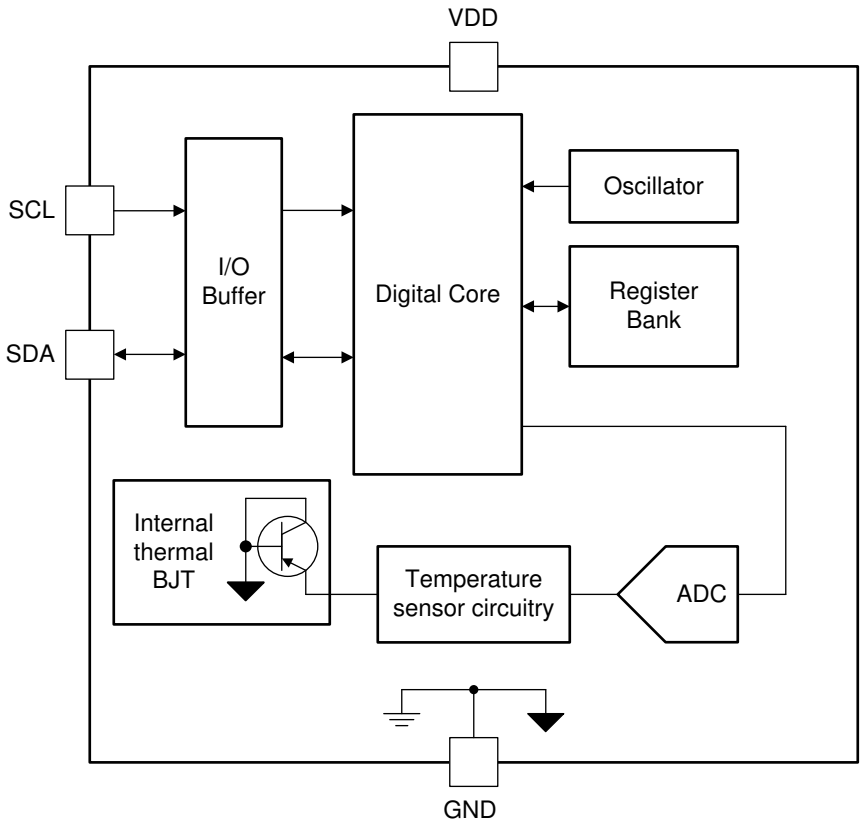
8 Detailed Description

8.1 Overview

The TMP114 is a digital output temperature sensor that comes factory calibrated on a NIST traceable setup. The device features a two-wire SMBus and I^2C interface-compatible interface with two modes of operation: continuous mode and shutdown mode designed for thermal management and thermal protection applications. The TMP114 also includes an alert status register with individual high and low thresholds along with adjustable hysteresis values.

Communication with the TMP114 has an integrated optional Cyclic Redundancy Check (CRC) module that will validate the data integrity of write and read operations.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 1.2 V Compatible Logic Inputs

The TMP114 features static input thresholds on the SCL and SDA pins independent of supply voltage. This allows the TMP114 to work with a 1.2 V or 1.8 V I^2C bus at any supported supply voltage.

8.3.2 Cyclic Redundancy Check (CRC)

The TMP114 implements an optional CRC function to improve data integrity and communication robustness using an 8-bit polynomial that is checked during communication. By default the feature is disabled and can be enabled by setting the CRC_EN bit in the Configuration register.

When enabled, the CRC function starts with the seed value of FFh at every start or repeated start condition on the bus and computes one CRC value. After transmitting or receiving a CRC value the TMP114, the next CRC will have the seed value reset to FFh.

When the TMP114 operates in target receive mode or during a write bus transaction, the CRC byte covers the device address, pointer address, and received data bytes. If the device detects a CRC error on the byte, it shall set the CRC_flag status bit in the Alert_Status register. If the CRC byte is not present, the transaction is discarded and the CRC flag is not set.

When the TMP114 operates in target transmit mode or during a read bus transaction, the CRC byte covers the device address and the sent data bytes.

8.3.3 Temperature Limits

TMP114 includes an on-board temperature limit warning. At the end of every completed conversion, the TMP114 compares the result against the limits stored in the low limit register and the high limit register. When the results exceed the THigh_Limit register value, the THigh_Status and THigh_Flag bits are set. Upon read, the THigh_Flag will clear but the THigh_Status bit will remain set. After the measured temperature crosses below the THigh_Limit - THigh_Hyst value, the THigh_Status bit will clear and the THigh_Flag bit is set again to indicate a change in the temperature with respect to the limits.

If the controller is unable to read the Temp_Result register for a prolonged period of time, the flag bits can be used to determine if a thermal limit was crossed during that time. The flag bits will only clear after a successful Alert_Status register read, therefore the high and low flags can help determine if the system crossed the thermal limit before an I2C read could be performed. The Status bits will automatically update with changing Temp_Result values. Figure 8-1 depicts this behavior.

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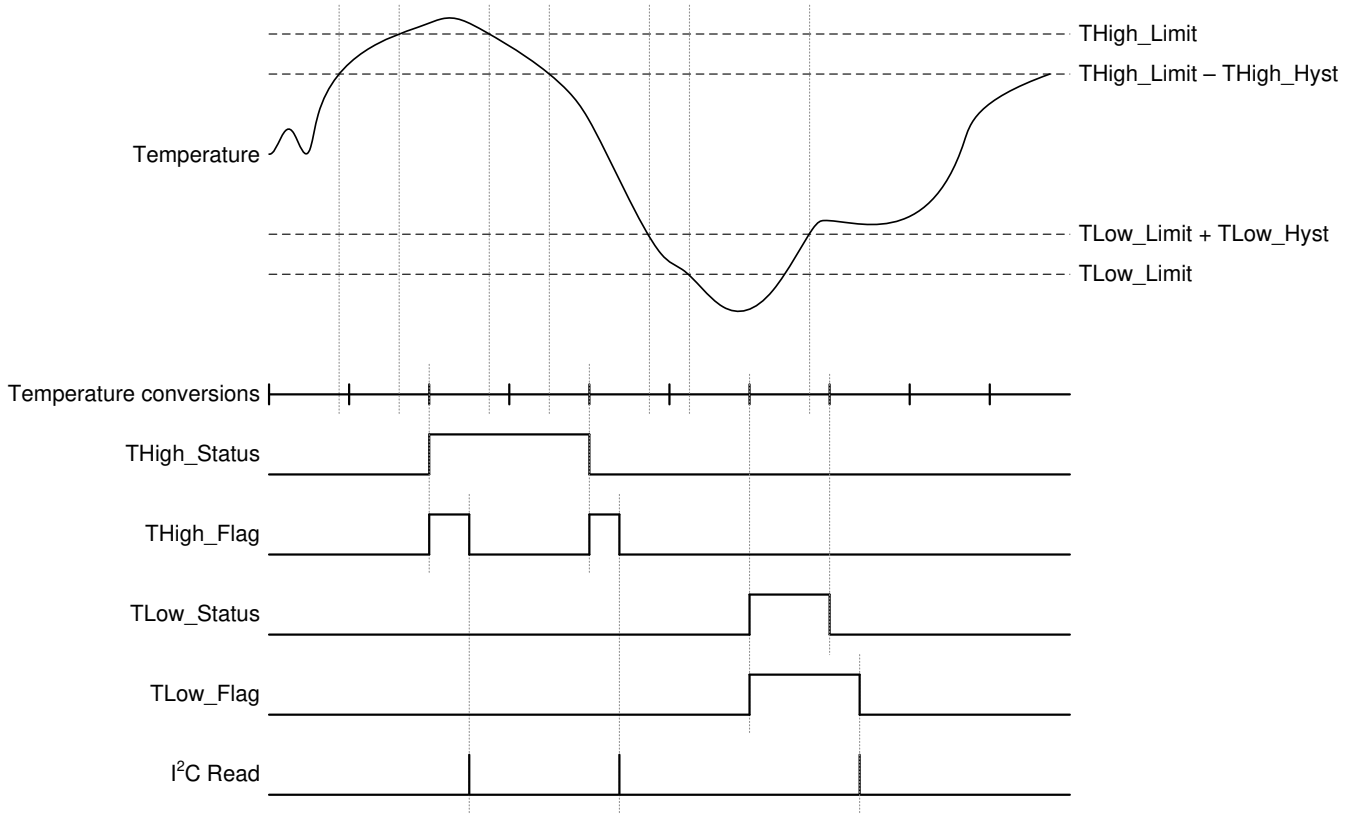

Figure 8-1. Alert Status Timing Diagram

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8.3.4 Slew Rate Warning

The slew warning alert is an alert option that can be adjusted with the Slew_Limit register. The slew rate warning will notify the system of rapid temperature changes as they occur, allowing the system to react and correct for the increase in temperature before reaching thermal operating limits. Compared to throttling a system after crossing a thermal limit, the slew rate warning will allow more safe system operation and greater reliability by not exceeding specified system operating conditions.

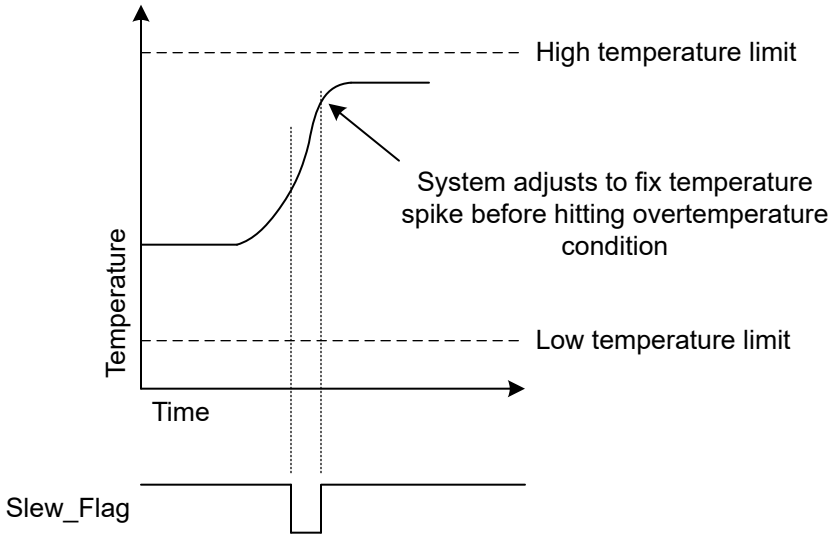

Figure 8-2. Slew Rate Alert

Calculating the slew rate requires a fixed time period to calculate and is only available in continuous mode. The Slew_Limit register is used to set the unsigned limit. The TMP114 will monitor the temperature slew rate and compare the positive change of temperature from the current conversion to the previous against the Slew_Limit. If the slew rate exceeds the Slew_Limit, the respective bits in the Alert_Status register will be set to indicate the warning. Figure 8-2 depicts the timing of the Slew Rate Warning relative to the temperature conversions. The slew rate check is always applied to the current temperature conversion and the previous temperature conversion.

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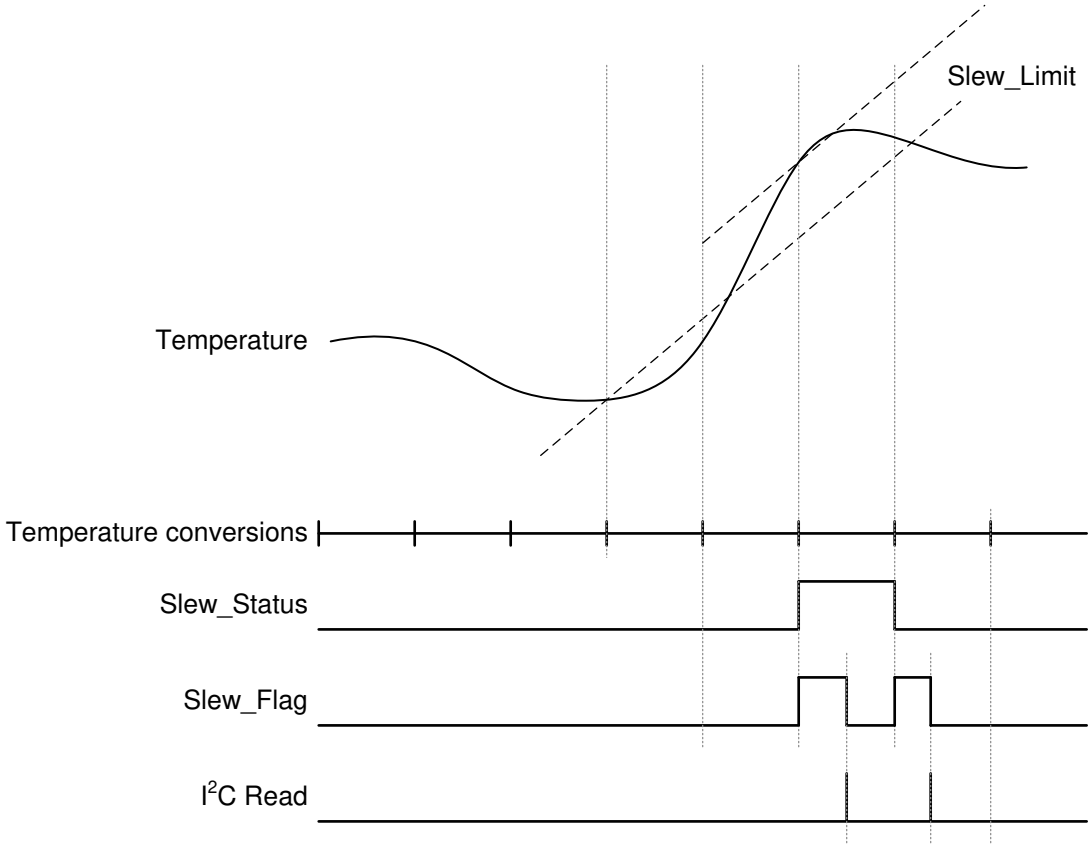

Figure 8-3. Slew Rate Warning Timing Diagram

The accuracy of the slew rate alert is ±15 % due to the dependence on the internal oscillator frequency variation for the calculation. Upon exiting continuous conversion mode, the slew rate alert will be automatically shut off. The register settings will not be altered. The feature will automatically turn on upon entering continuous conversion mode. The slew rate alert can only be set for positive slew rate limits.

8.3.5 NIST Traceability

The accuracy of temperature testing is verified with equipment that is calibrated by an accredited lab that complies with ISO/IEC 17025 policies and procedures. Each device is tested and trimmed to conform to its respective data sheet specification limits.

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8.4 Device Functional Modes

The TMP114 can be configured to operate in continuous or shutdown mode. This flexibility enables designers to balance the requirements of power efficiency and performance.

8.4.1 Continuous Conversion Mode

When the Mode bit is set to 0b in the configuration register, the device operates in continuous conversion mode. Figure 8-4 shows the device in a continuous conversion cycle. In this mode, the device can perform multiple conversions and updates the temperature result register and Data_Ready_Flag in the alert status register at the end of every active conversion. The typical active conversion time for the device is 6.4 ms with averaging disabled. When averaging is enabled, the device will convert 8 consecutive times at the beginning of every conversion period for a typical time of 51.2 ms.

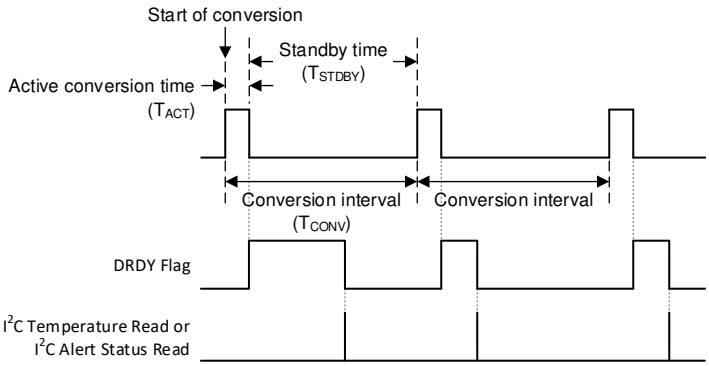

Figure 8-4. Continuous Conversion Cycle Timing Diagram

The Conv_Period[1:0] bits in the configuration register control the rate at which the conversions are performed. The device typically consumes 68 µA during conversion and 0.26 µA during the low power standby period. By decreasing the rate at which the conversions are performed, the application can benefit from reduced average current consumption in continuous mode.

Use Equation 1 to calculate the average current in continuous mode.

$$\text{Average Current} = ((I_{ACT} \times t_{ACTIVE}) + (I_{Standby} \times t_{Standby})) / t_{Conv\_Period} \quad (1)$$

Where

- t_{ACTIVE} = Active Conversion Time
- t_{Conv_Period} = Conversion Period
- $t_{Standby}$ = Standby time between conversions calculate as $t_{Conv\_Period} - t_{ACTIVE}$

8.4.2 Shutdown Mode

When the Mode bit is set to 1b in the Configuration register, the device immediately enters the low-power shutdown mode. If the TMP114 is performing a temperature conversion, the device will stop the conversion and discard the partial result. In this mode, the device powers down all active circuitry and can be used in conjunction with the One_Shot bit to perform One-Shot temperature conversions. Shutdown mode enables designers to extend battery life as the typical power consumption is only 0.16uA in this mode of operation.

Changing between continuous and shutdown modes will not clear any active. The slew rate alert will not be triggered again in shutdown mode, but previous active alerts will not clear until the alert register is read or a one-shot temperature conversion is triggered.

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8.4.2.1 One-Shot Temperature Conversions

When the OS bit is set to 1b in the Configuration register, the TMP114 immediately start a one-shot temperature conversion. If the TMP114 is performing a temperature conversion, the device will stop the active conversion and discard the partial result, then start a new one-shot conversion. After completing the one-shot conversion the TMP114 will enter shutdown mode, the OS bit will be cleared, and the Mode bit will be set to 1b. If a one-shot conversion is triggered in continuous mode the device will enter shutdown mode after the one-shot conversion completes.

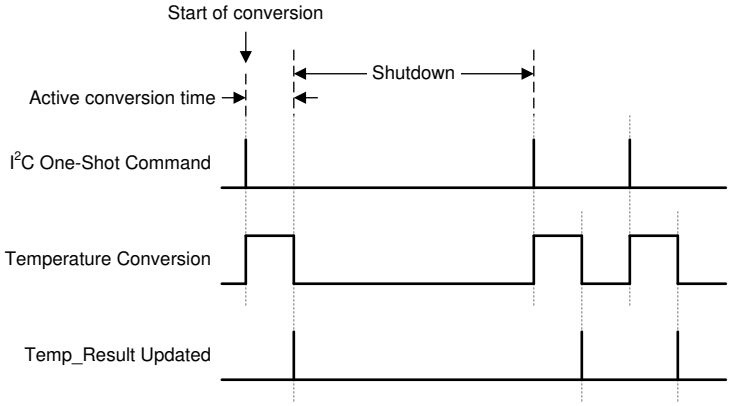

Figure 8-5. One-Shot Timing Diagram

If the One_Shot bit is continuously written as faster than the active conversion time of the TMP114, the device will continue to restart the temperature conversion with each new write to the One_Shot bit. TI recommends to avoid this behavior because the temperature result does not update until a conversion finishes. If the system triggers several continuous one-shot conversions, Figure 8-6 depicts how the device would continually partially finish new conversions and not update the Temp_Result register.

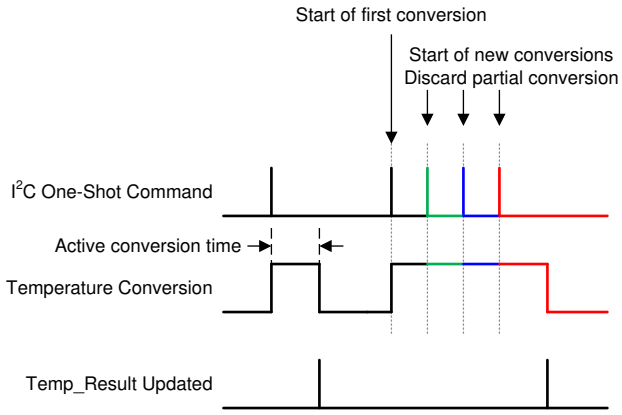

Figure 8-6. One-Shot Continuous Trigger Timing Diagram

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8.5 Programming

8.5.1 Temperature Data Format

Temperature data is represented by a 16-bit two's complement word with a Least Significant Bit (LSB) equal to 0.0078125 °C. The temperature output of the TMP114 has a range of -256 °C to 255 °C.

Table 8-1. 16-Bit Temperature Data Format

Temperature	Digital Output	
	Binary	Hex
+125 °C	0011 1110 1000 0000	3E80
+25 °C	0000 1100 1000 0000	0C80
+0.0078125 °C	0000 0000 0000 0001	0001
0 °C	0000 0000 0000 0000	0000
−0.0078125 °C	1111 1111 1111 1111	FFFF
−25 °C	1111 0011 1000 0000	F380
−40 °C	1110 1100 0000 0000	EC00

8.5.2 I²C and SMBus Interface

The TMP114 has a standard bidirectional I²C interface that is controlled by a controller device in order to be configured or read the status of this device. Each target on the I²C bus has a specific device address to differentiate between other target devices that are on the same I²C bus. Many target devices require configuration upon start-up to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. The TMP114 includes 50-ns glitch suppression filters, allowing the device to coexist on an I3C mixed bus. The TMP114 supports transmission data rates up to 1 MHz.

The physical I²C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to a supply through a pullup resistor. The size of the pullup resistor is determined by the amount of capacitance on the I²C lines and the communication frequency. For further details, see the I²C Pullup Resistor Calculation application report. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition (see Figure 8-7 and Figure 8-8).

The following is the general procedure for a controller to access a target device:

1. If a controller wants to send data to a target:
   - Controller-transmitter sends a START condition and addresses the target-receiver.
   - Controller-transmitter sends the requested register to write target-receiver.
   - Controller-transmitter sends data to target-receiver.
   - Controller-transmitter terminates the transfer with a STOP condition.
2. If a controller wants to receive or read data from a target:
   - Controller-receiver sends a START condition and addresses the target-transmitter.
   - Controller-receiver sends the requested register to read to target-transmitter.
   - Controller-receiver receives data from the target-transmitter.
   - Controller-receiver terminates the transfer with a STOP condition.

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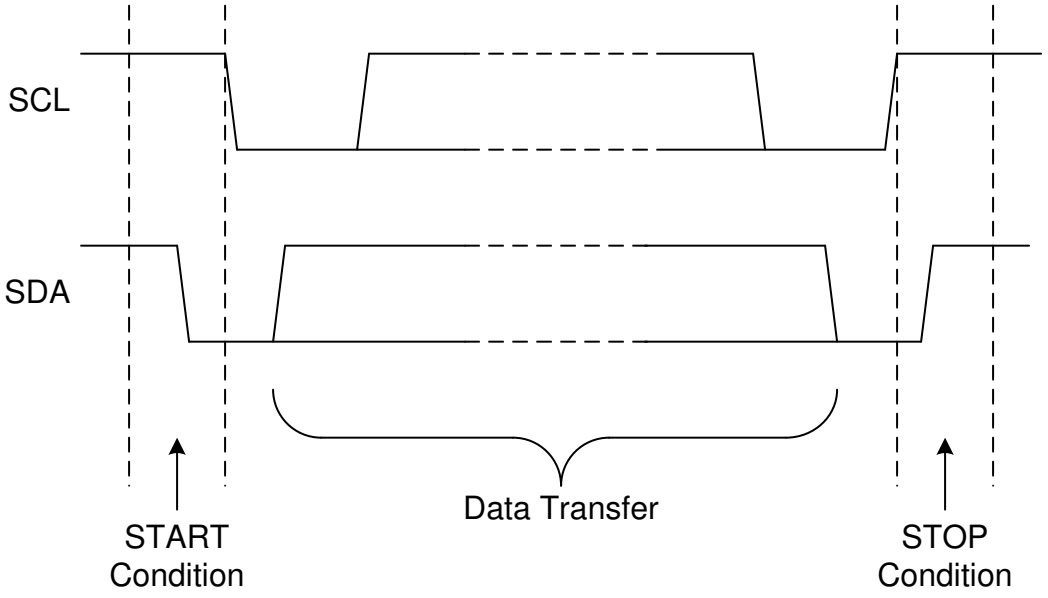

Figure 8-7. Definition of Start and Stop Conditions

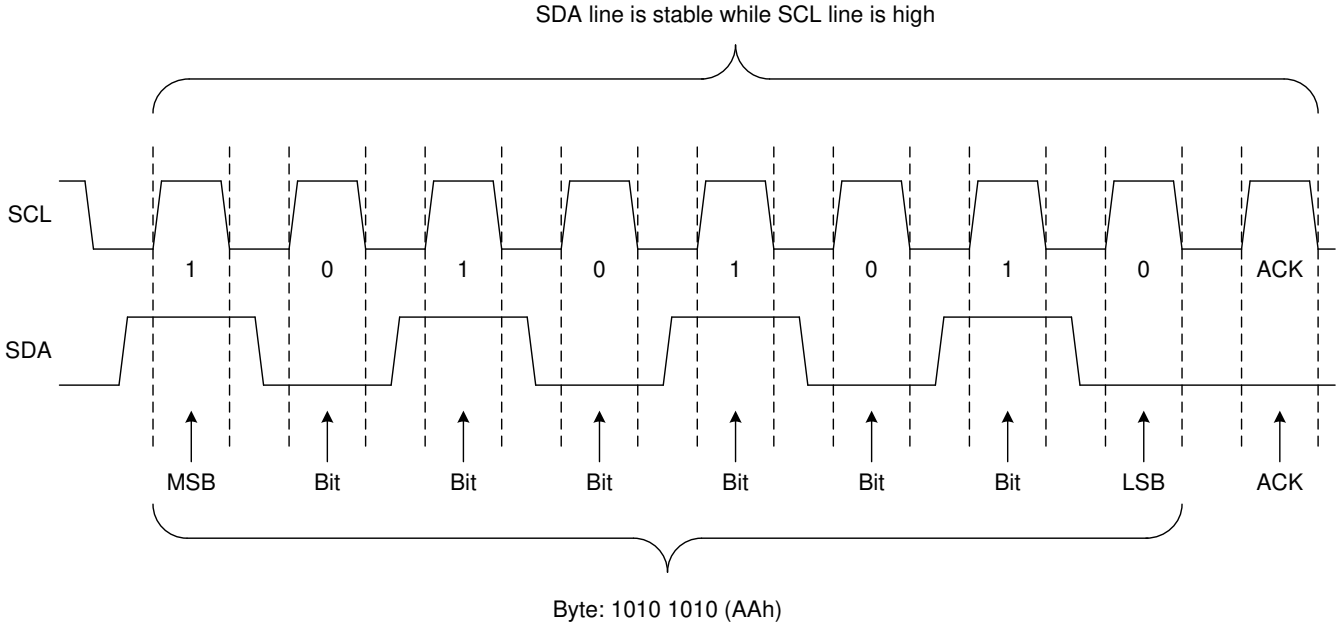

Figure 8-8. Bit Transfer

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8.5.3 Device Address

To communicate with the TMP114, the controller must first address target devices through an address byte. The address byte has seven address bits and a read-write (R/W) bit that indicates the intent of executing a read or write operation. Table 8-2 shows the TMP114 available in multiple versions, each with a different target address.

Table 8-2. Device Target Address

Product	Device Two-Wire Address
TMP114A	1001000
TMP114B	1001001
TMP114C	1001010
TMP114D	1001011
TMP114ND	1001100
TMP114NC	1001101
TMP114NB	1001110
TMP114NA	1001111

8.5.4 Bus Transactions

Data must be sent to and received from the target devices, and this is accomplished by reading from or writing to registers in the target device.

Registers are locations in the memory of the target which contain information, whether it be the configuration information or some sampled data to send back to the controller. The controller must write information to these registers in order to instruct the target device to perform a task.

8.5.4.1 Auto-Increment

The TMP114 supports the use of the auto-increment feature. In the control register byte of the I2C transaction, bit 7 is used as the auto-increment bit. If the bit is set to 0b, continuous reads or writes will only read and write to the register specified in the register pointer. If the Auto-increment bit is set to 1b, continuous reads and writes will increment the address pointer by 1 after every word of data has been read or written to the TMP114. This allows the controller to read or write to multiple registers with a single transaction for faster communication.

Figure 8-9 shows the structure of the Control Register.

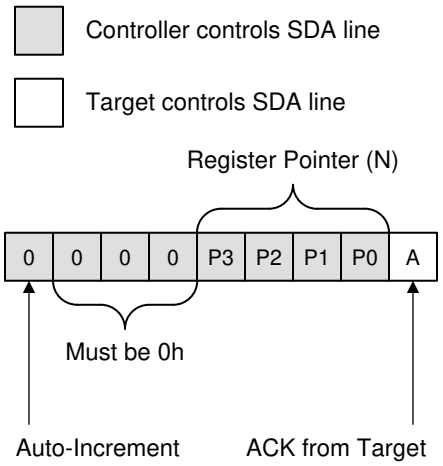

Figure 8-9. Control Register

8.5.4.2 Writes

To write on the I²C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/W bit) set to 0b, which signifies a write. The target acknowledges, letting the controller know it is ready. After this, the controller starts sending the control register data to the target until the controller has sent all the data necessary, and the controller terminates the transmission with a STOP condition.

Writes to read-only registers or register locations outside of the register map will be ignored. The TMP114 will still ACK when writing outside of the register map.

Figure 8-10 shows an example of writing a single word write communication.

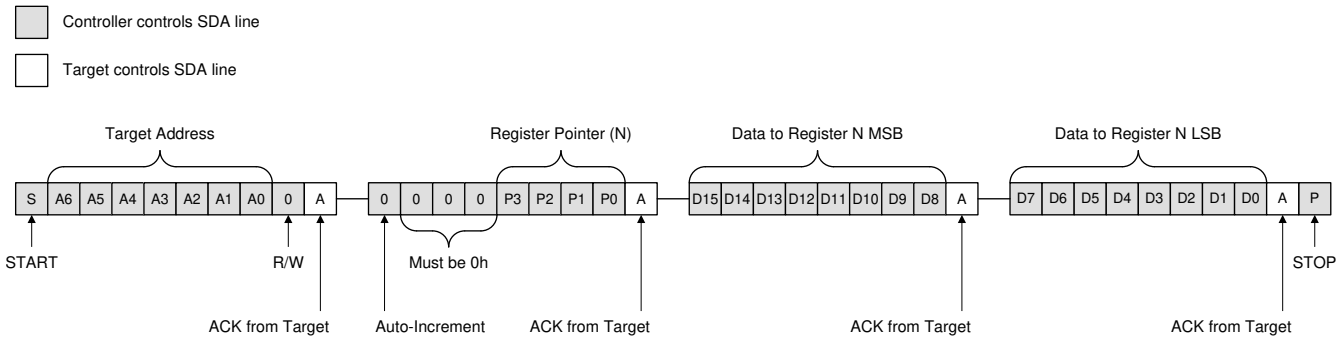

Figure 8-10. Write to Single Register

Multiple writes to the same register are also possible with the TMP114. Figure 8-11 shows how the controller can repeatedly write to the same register when the Auto-Increment bit in the control register is set to 0b.

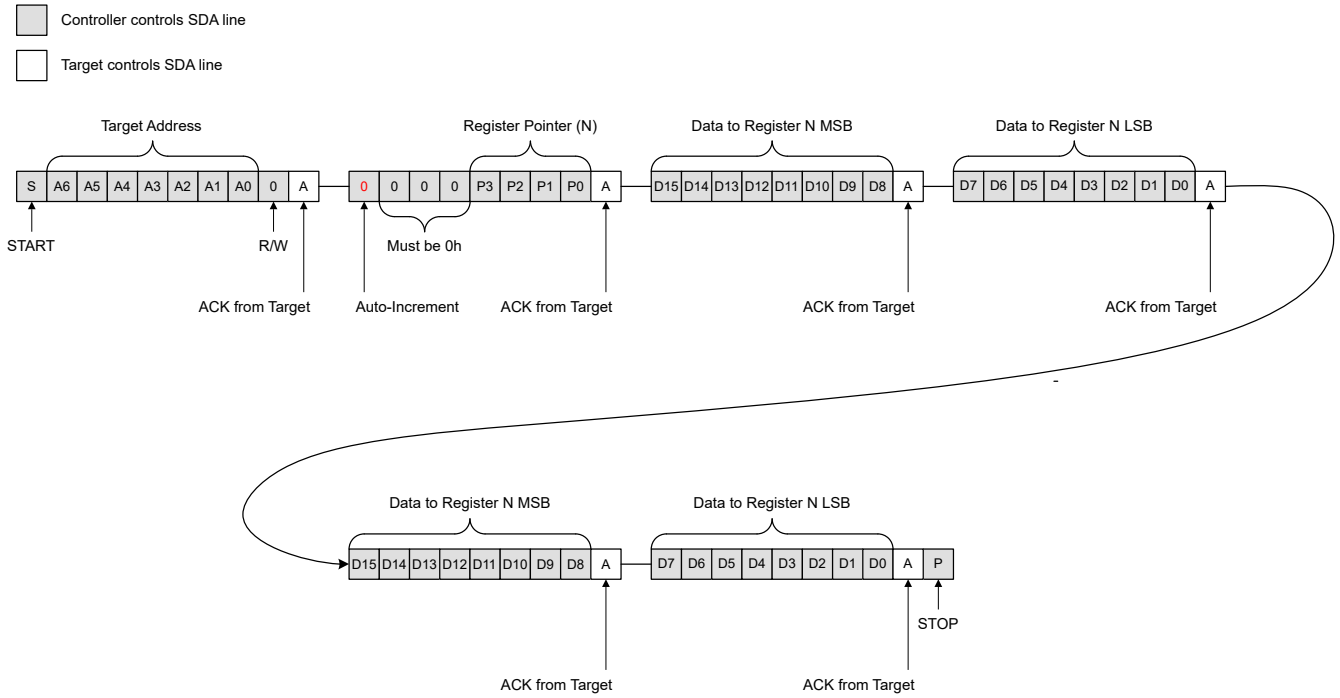

Figure 8-11. Repeated Write to Single Register

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The TMP114 also supports a continuous write to sequential registers. By setting the Auto-Increment bit in the control register to 1b, the TMP114 will increment the address pointer after each word of data is written to the device. This allows the controller to write multiple register values in the same transaction as shown in Figure 8-12. Currently this feature will not allow the controller to properly write to the Configuration register and it is recommended to use single register writes to the Configuration register.

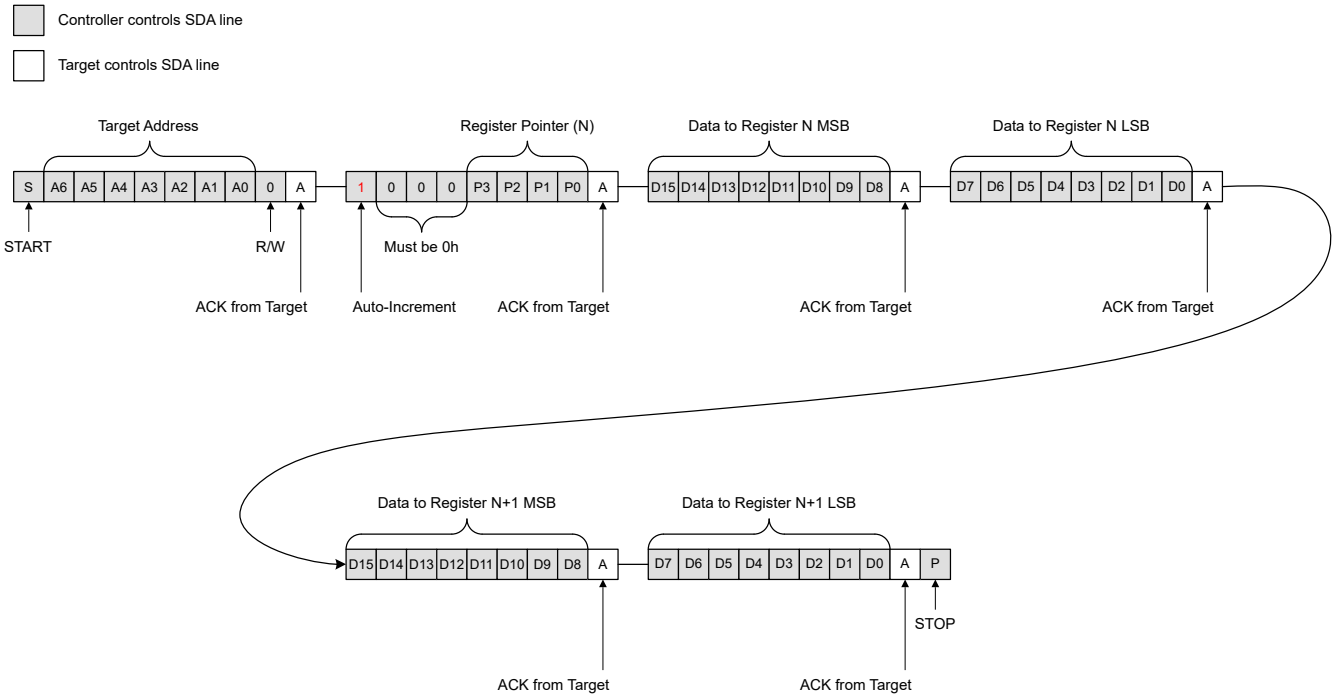

Figure 8-12. Burst Write to Multiple Registers

8.5.4.2.1 CRC Enabled Writes

The TMP114 supports the ability to check data integrity with an 8-bit CRC value for every transaction. By setting the CRC_Enable bit to 1b in the Configuration Register, the device will use CRC to validate any write transactions. During a CRC enabled write transaction, the TMP114 will check the Target Address, Control Register, MSB, and LSB of data against the CRC value. After the first CRC byte, each subsequent MSB and LSB of data sent to the TMP114 will have its own CRC byte for validation. If the first CRC byte fails, the TMP114 will discard the entire write transaction. If the first CRC passes, the TMP114 will only discard data if the associated CRC checksum fails. For example, consider the case where a controller tries to write values to registers 03h, 04h, and 05h. If the first and third CRC values are valid but the second CRC value is incorrect, the TMP114 will shift the 03h and 05h values into the registers and discard the 04h values. Figure 8-13shows an overview of a write transaction with CRC.

If the TMP114 determines the CRC failed, it will NACK on the CRC byte and the CRC_Flag bit in the Alert status register will be set. If the CRC byte is not included the TMP114 will interpret this as an incomplete transaction and discard the write contents and the status flag will not be set. Multiple writes to the same register in a single transaction with Auto-Increment set to 0b and CRC enabled is not supported.

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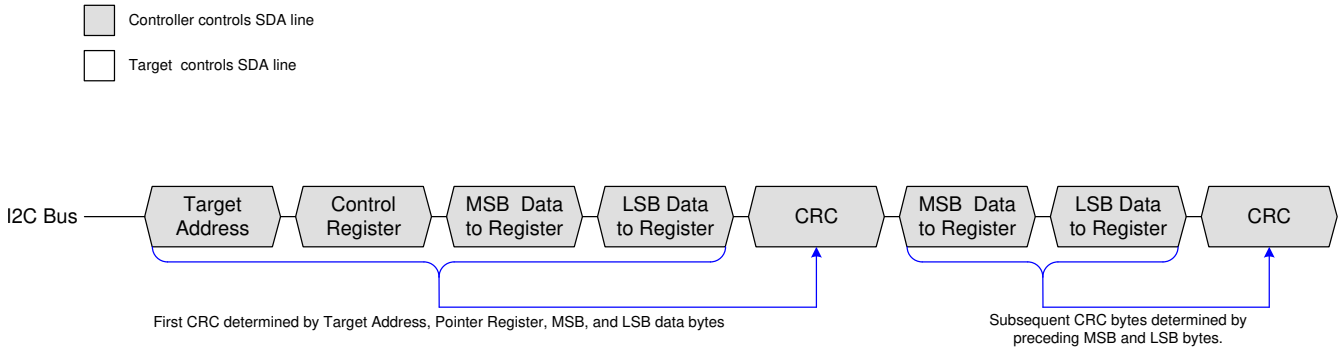

Figure 8-13. CRC Enabled Write

8.5.4.3 Reads

For a read operation the controller sends a START condition, followed by the target address with the R/W bit set to 0b (signifying a write). The target acknowledges the write request, and the controller sends the command byte with the Auto-Increment bit and Register Pointer. After the Control Register, the controller will initiate a restart followed by the target address with the R/W bit set to 1b (signifying a read). The controller will continue to send out clock pulses but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that it is ready for more data. Once the controller has received the number of bytes it is expecting, it sends a NACK, signaling to the target to halt communications and release the SDA line. The controller follows this up with a STOP condition. Reading from a non-indexed register location will return 00h.

Figure 8-14 shows an example of reading a single word from a target register.

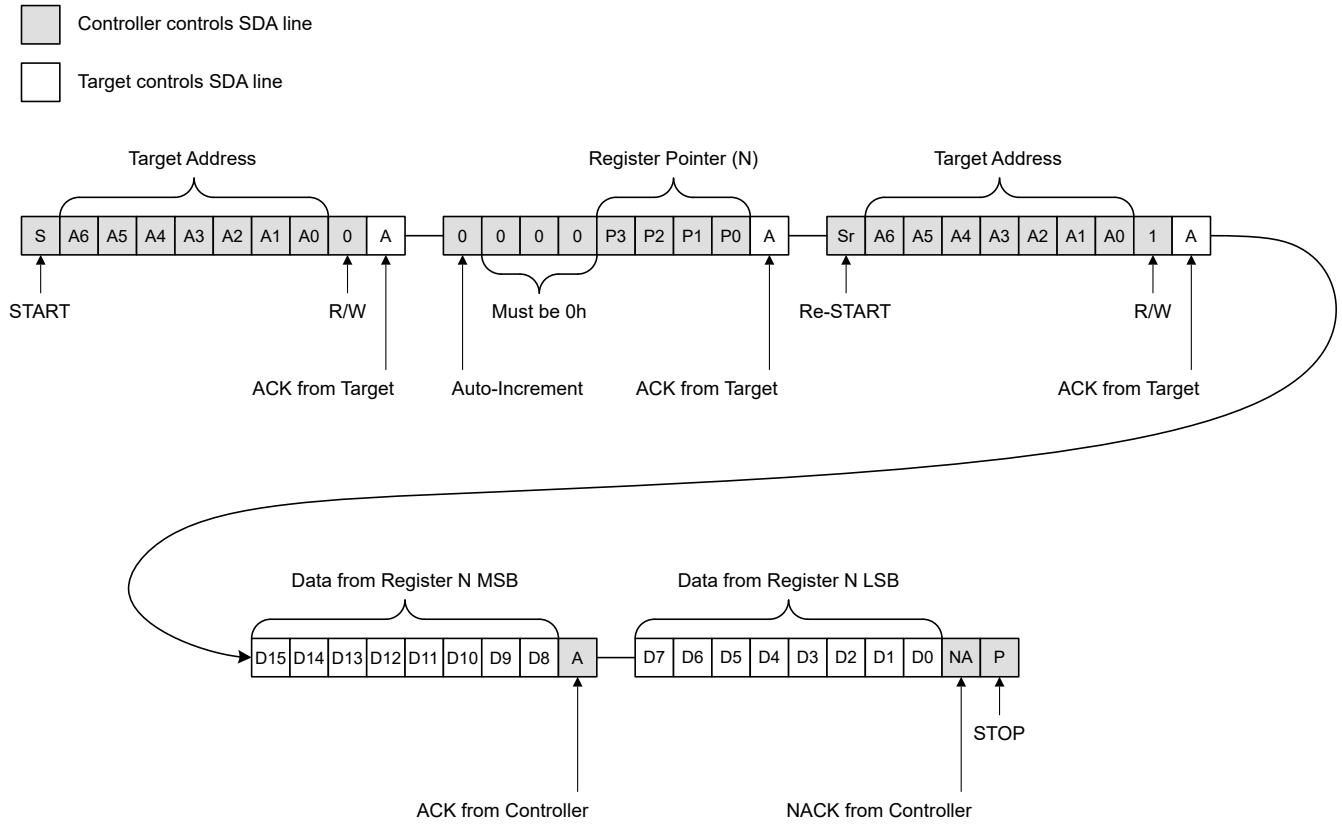

Figure 8-14. Read from Single Register

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Multiple reads from the same register are also possible with the TMP114. Figure 8-15 shows how the controller can repeatedly read from the same register when the Auto-Increment bit in the control register is set to 0b. When reading from the same register in the same transaction the device must be read faster than the I^2C timeout period.

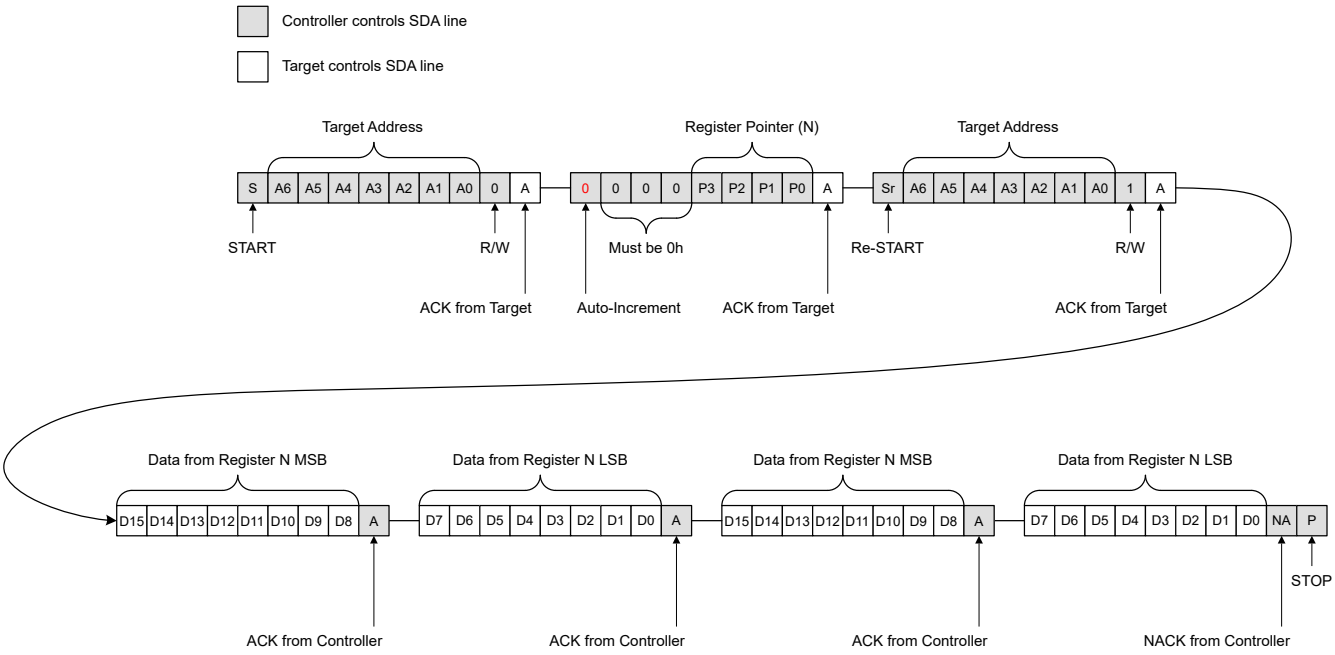

Figure 8-15. Repeated Read from Single Register

The TMP114 also supports a continuous read from sequential registers. By setting the Auto-Increment bit in the control register to 1b, the TMP114 will increment the address pointer after each word of data is read from the device. This allows the controller to read multiple register values in the same transaction as shown in Figure 8-16. Currently, using a burst read will not clear the Alert Status register. It is recommended to use single register reads to clear Alert Status register contents.

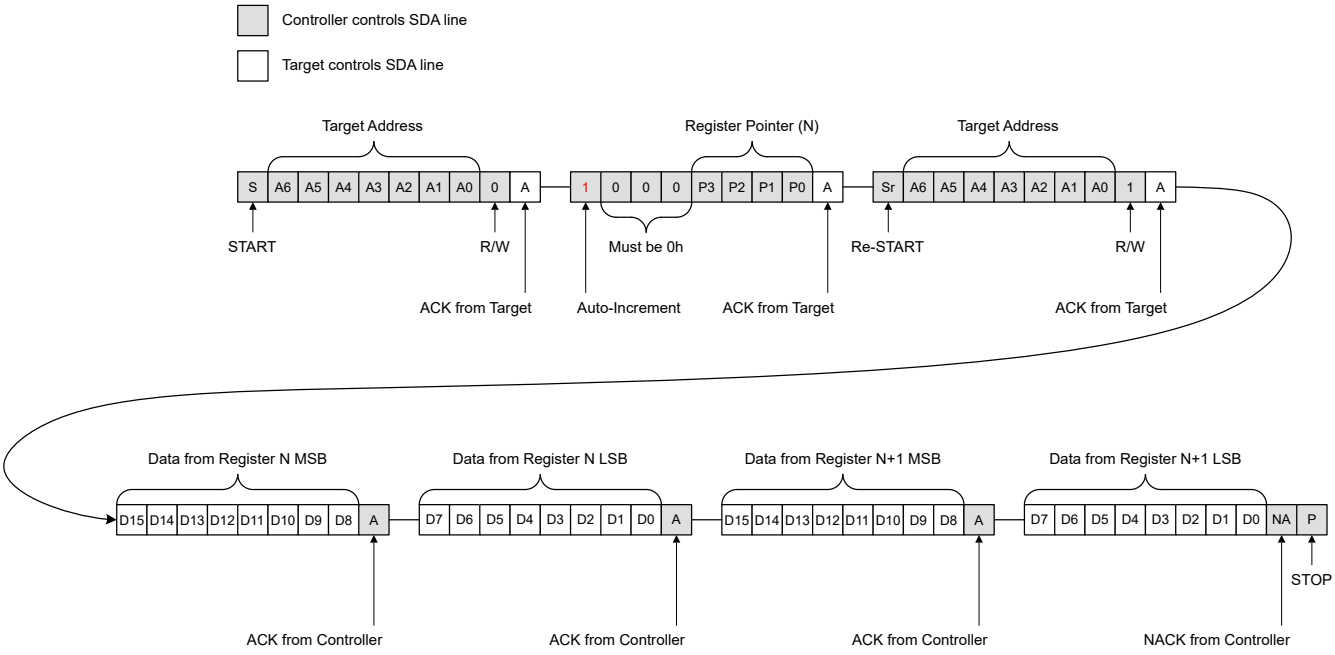

Figure 8-16. Burst Read from Multiple Registers

8.5.4.3.1 CRC Enabled Reads

The TMP114 supports the ability to check data integrity with an 8-bit CRC value for every read transaction. By setting the CRC_Enable bit to 1b in the Configuration Register, the device will use CRC to validate any read transactions. During a CRC enabled read, the TMP114 will check the Target Address and Control Register against the CRC value sent by the controller. The second CRC byte, after the restart, will be sent by the TMP114 and will check the Target Address, MSB, and LSB from the first register. All subsequent MSB and LSB bytes of data sent from the TMP114 will have their own CRC values. Figure 8-17shows an overview of a read transaction with CRC.

If the TMP114 determines the CRC failed, it will NACK on the CRC byte and the CRC_Flag bit in the Alert status register will be set. The TMP114 will NACK after the restart to its target address and send FFh if the controller continues clocking the SCL line until a STOP condition is sent and a new transaction started.

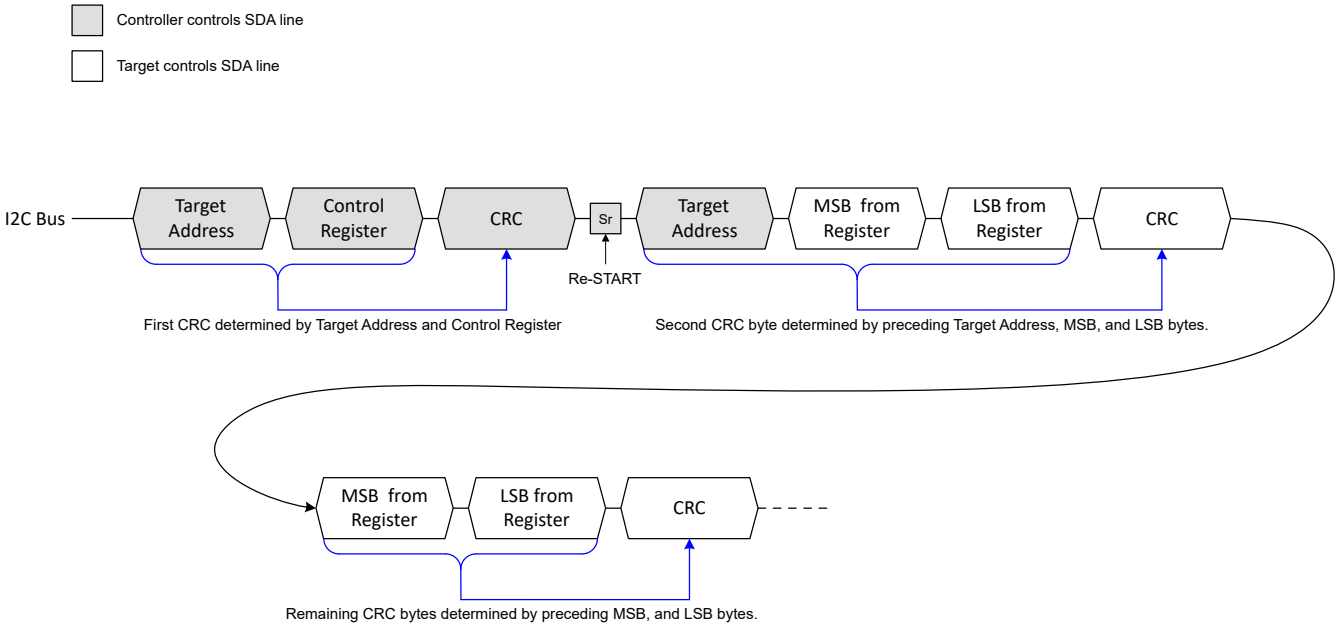

Figure 8-17. CRC Enabled Read

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8.5.4.4 General Call Reset Function

The TMP114 responds to a two-wire, general-call address (0000 000) if the eighth bit is 0b. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0000b 0110b, the TMP114 internal registers are reset to power-up values as shown in Figure 8-18. The serial address is unaffected by the general call reset.

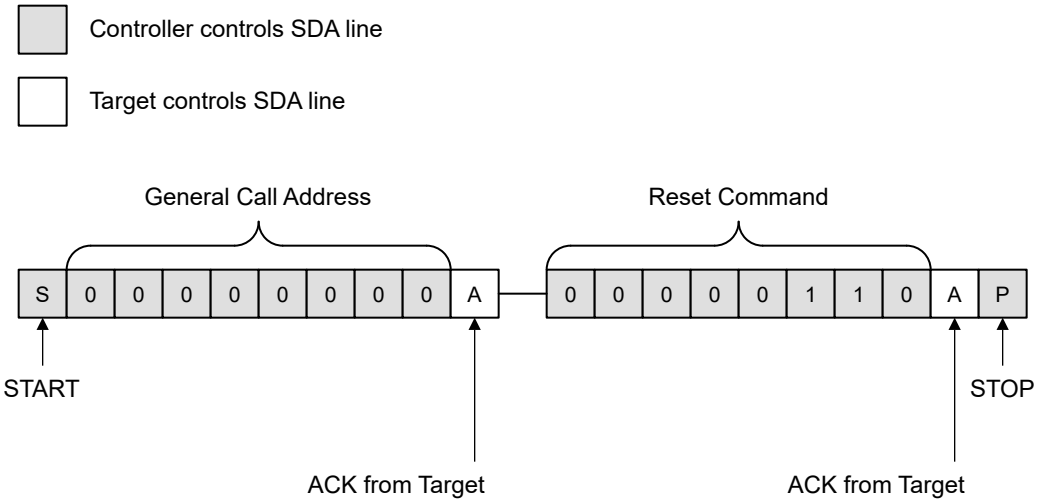

Figure 8-18. SMBus General Call Timing Diagram

8.5.4.5 Time-Out Function

The TMP114 resets the serial interface if the SCL line is held low by the controller or the SDA line is held low by the TMP114 for 30 ms (typical) between a START and STOP condition. The TMP114 releases the SDA line if the SCL pin is pulled low and waits for a START condition from the controller. To avoid activating the timeout function, maintain a communication speed of at least 1 kHz for the SCL operating frequency. If another device on the bus is holding the SDA pin low, the TMP114 will not reset.

8.5.4.6 Coexist on I3C MixedBus

A bus with both I3C and I^2C interfaces is referred to as a mixed with clock speeds up to 12.5 MHz. The TMP114 is an I^2C device that can be on the same bus that has an I3C device attached as the TMP114 incorporates a spike suppression filter of 50 ns on the SDA and SCL pins to avoid any interference to the bus when communicating with I3C devices.

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8.5.4.7 Cyclic Redundancy Check Implementation

Table 8-3 defines the CRC calculation rule.

Table 8-3. CRC Rule Table

CRC Rule	Value
CRC Width	8 bits
Polynomial	$x^8 + x^2 + x + 1$ (07h)
Initial seed value	FFh
Input data reflected	No
Result data reflected	No
XOR value	00h

The CRC calculation is done on the command word and the data block. Figure 8-19 shows the block diagram. The module consists of an 8-bit shift register and 3 exclusive-OR gates. The register starts with the seed value FFh and the module performs an XOR function and shifts its content until the last bit of the register string is used. The final value of the shift register is the checksum that is checked by either the controller or the TMP114 to validate the transaction.

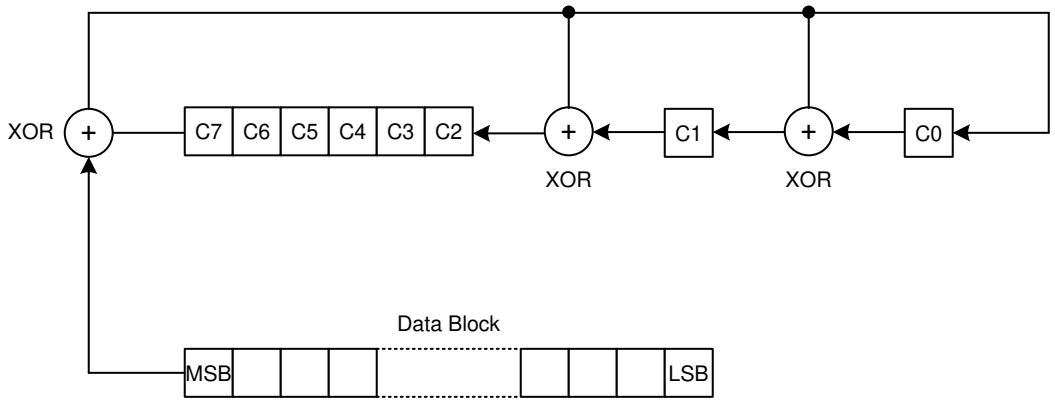

Figure 8-19. CRC Module

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8.6 Register Map

Table 8-4. TMP114 Registers

ADDRESS	TYPE	RESET	ACRONYM	REGISTER NAME	SECTION
00h	R	0000h	Temp_Result	Temperature result register	Go
01h	R	0000h	Slew_Result	Slew rate result register	Go
02h	R/RC	0000h	Alert_Status	Alert status register	Go
03h	R/W	0004h	Configuration	Configuration register	Go
04h	R/W	F380h	TLow_Limit	Temperature low limit register	Go
05h	R/W	2A80h	THigh_Limit	Temperature high limit register	Go
06h	R/W	0A0Ah	Hysteresis	Hysteresis register	Go
07h	R/W	0500h	Slew_Limit	Temperature slew rate limit register	Go
08h	R	xxxxh	Unique_ID1	Unique_ID1 register	Go
09h	R	xxxxh	Unique_ID2	Unique_ID2 register	Go
0Ah	R	xxxxh	Unique_ID3	Unique_ID3 register	Go
0Bh	R	1114h	Device_ID	Device ID register	Go
10h - 2Ah	R	xxxxh	Reserved	Reserved	

Table 8-5. TMP114 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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8.6.1 Temp_Result Register (Address = 00h) [reset = 0000h]

This register stores the latest temperature conversion result in a 16-bit two's complement format with a LSB (Least Significant Bit) equal to 0.0078125 °C.

Return to Register Map.

Figure 8-20. Temp_Result Register

15	14	13	12	11	10	9	8
Temp_Result[15:8]							
R-00h							
7	6	5	4	3	2	1	0
Temp_Result[7:0]							
R-00h							

Table 8-6. Temp_Result Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Temp_Result[15:0]	R	0000h	16-bit temperature conversion result Temperature data is represented by a 16-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.0078125 °C.

8.6.2 Slew_Result Register (Address = 01h) [reset = 0000h]

This register stores the latest temperature conversion result in a 14-bit two's complement format with a LSB (Least Significant Bit) equal to 0.03125 °C/s. The Slew Rate Warning currently does not support negative values.

Return to Register Map.

Figure 8-21. Slew_Result Register

15	14	13	12	11	10	9	8
Slew_Result[13:6]							
R-0h							
7	6	5	4	3	2	1	0
Slew_Result[5:0]						**Reserved**	
R-0h						R-0h	

Table 8-7. Slew_Result Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	Slew_Result[13:0]	R	0000h	Temperature slew rate result Temperature slew rate is represented by a 14-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.03125 °C/s.
1:0	Reserved	R	0h	These two bits will always read 0h

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8.6.3 Alert_Status Register (Address = 02h) [reset = 0000h]

This register shows the current alert status of the TMP114.

Return to Register Map.

Figure 8-22. Alert_Status Register

15	14	13	12	11	10	9	8
Reserved							
R-00h							
7	6	5	4	3	2	1	0
CRC_Flag	Slew_Status	Slew_Flag	THigh_Status	TLow_Status	THigh_Flag	TLow_Flag	Data_Ready_Flag
RC-0h	R-0h	RC-0h	R-0h	R-0h	RC-0h	RC-0h	RC-0h

Table 8-8. Alert_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	R	00h	Reserved
7	CRC_Flag	RC	0h	CRC checksum error flag indicator. This indicates that the write transaction CRC checksum failed and the register settings were discarded 0h = The most recent CRC enabled write transaction was successful 1h = The most recent CRC enabled write transaction failed
6	Slew_Status	R	0h	Slew status indicator. This bit is set if there is a positive slew rate exceeding the Slew_Rate_Limit. 0h = The most recent temperature conversion result is below the Slew_Rate_Limit 1h = The most recent temperature conversion result is above the Slew_Rate_Limit
5	Slew_Flag	RC	0h	Slew rate flag indicator. This indicates that the temperature slew rate crossed the slew rate limit threshold. Reading the Alert_Status register will clear this bit 0h = The most recent temperature conversion has not crossed the Slew_Rate_Limit threshold 1h = A temperature conversion has crossed the Slew_Rate_Limit threshold
4	THigh_Status	R	0h	High temperature status indicator. 0h: The most recent temperature conversion result is below the THigh_Limit 1h: The most recent temperature conversion is above the THigh_Limit. Once set, this bit will not clear until a temperature conversion is below THigh_Limit - THigh_Hyst
3	TLow_Status	R	0h	Low temperature status indicator. 0h: The most recent temperature conversion result is above the TLow_Limit 1h: The most recent temperature conversion is below the THigh_Limit. Once set, this bit will not clear until a temperature conversion is above TLow_Limit + TLow_Hyst

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Table 8-8. Alert_Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	THigh_Flag	RC	0h	High temperature flag indicator. This indicates that the latest temperature conversion has cross above the THigh_Limit register threshold or crossed below the THigh_Limit - THigh_Hyst threshold. Reading Alert_Status register will clear this bit. 0h = The most recent temperature conversion has not crossed the THigh_Limit or the hysteresis threshold. 1h: A temperature conversion crossed the THigh_Limit or crossed below the THigh_Limit - THigh_Hyst threshold. Once the THigh_Flag is set, THigh_Flag will not be set again until a temperature conversion is below THigh_Limit - THigh_Hyst
1	TLow_Flag	RC	0h	Low temperature flag indicator. This indicates that the latest temperature conversion has cross below the TLow_Limit register threshold or crossed above the Tlow_Limit + TLow_Hyst threshold. Reading Alert_Status register will clear this bit. 0h = The most recent temperature conversion has not crossed the TLow_Limit or the hysteresis threshold. 1h: A temperature conversion crossed below the TLow_Limit. Once the TLow_Flag is set, TLow_Flag will not be set again until temperature conversion is above TLow_Limit + TLow_Hyst
0	Data_Ready_Flag	RC	0h	Data Ready flag indicator. This indicates a new temperature conversion result is available. This bit is only cleared by reading the Alert_Status register . 0h = Data_Ready_Flag has been cleared since the last temperature conversion 1h = Data in Temp_Result is new

8.6.4 Configuration Register (Address = 03h) [reset = 0004h]

This register is used to configuration the operation of the TMP114.

Return to Register Map.

Figure 8-23. Configuration Register

15	14	13	12	11	10	9	8
Reserved					ADC_Conv_Time[1:0]		Reset
R-00h					RW-0h		R/W-0h
7	6	5	4	3	2	1	0
AVG	CRC_En	**Reserved**	OS	Mode	Conv_Period[2:0]		
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-4h		

Table 8-9. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	R	00h	Reserved
10:9	ADC_Conv_Time[1:0]	R/W	0h	ADC Conversion Time setting. This bit field changes the ADC conversion time and resolution of the TMP114. If the averaging time is longer than the conversion period setting the minimum cycle time will be the averaging time. 0h = 6.4 ms 1h = 3.5 ms 2h = 2.0 ms 3h = 1.2 ms

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Table 8-9. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Reset	R/W	0h	Software reset bit. When set to 1 it triggers software reset with a duration of 1 ms. This bit will always read back 0
7	AVG	R/W	0h	Averaging enable bit. Averaging will force every measurement including one-shot measurements to be averaged with eight conversions. 0h: Averaging is disabled 1h: Averaging is enabled
6	CRC_En	R/W	0h	CRC enable. Enables the CRC feature for the next transaction after a stop command is received. 0h = CRC is disabled 1h = CRC is enabled
5	Reserved	R	0h	Reserved
4	OS	R/W	0h	One-shot conversion trigger. After completing the one-shot conversion this bit is reset to 0h. Triggering a one-shot conversion will place the TMP114 into shutdown mode. 0h = Default 1h = Trigger a one-shot conversion
3	Mode	R/W	0h	Conversion mode selection bit. 0h = Continuous conversion mode 1h = Shutdown mode
2:0	Conv_Period[2:0]	R/W	4h	Conversion period setting. This bit field changes the conversion period of the TMP114. If the averaging time is longer than the conversion period setting the minimum conversion time will be the averaging time. 0h = 6.4 ms 1h = 31.25 ms / 32 Hz 2h = 62.5 ms / 16 Hz 3h = 125 ms / 8 Hz 4h = 250 ms / 4 Hz 5h = 500 ms / 2 Hz 6h = 1 s / 1 Hz 7h = 2 s / 0.5 Hz

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8.6.5 TLow_Limit Register (Address = 04h) [reset = F380h]

This register is used to configuration the low temperature limit of the TMP114. The limit is formatted in a 14-bit two's complement format with a LSB (Least Significant Bit) equal to 0.03125 °C. The range of the register is ±256 °C. The default value on start-up is F380h or -25 °C. If the THigh_Limit register is equal to or less than the TLow_Limit register the temperature limits will be ignored.

Return to Register Map.

Figure 8-24. TLow_Limit Register

15	14	13	12	11	10	9	8
TLow_Limit[13:6]							
R/W-F3h							
7	6	5	4	3	2	1	0
TLow_Limit[5:0]						**Reserved**	
R/W-20h						R-0h	

Table 8-10. TLow_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	TLow_Limit[13:0]	R/W	3CE0h	14-bit temperature low limit setting. Temperature low limit is represented by a 14-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.03125°C. The default setting for this is -25°C.
1:0	Reserved	R	0h	These two bits will always read 0h

8.6.6 THigh_Limit Register (Address = 05h) [reset = 2A80h]

This register is used to configuration the high temperature limit of the TMP114. The limit is formatted in a 14-bit two's complement format with a LSB (Least Significant Bit) equal to 0.03125 °C. The range of the register is ±256 °C. The default value on start-up is 2A80h or 85 °C. If the THigh_Limit register is equal to or less than the TLow_Limit register the temperature limits will be ignored.

Return to Register Map.

Figure 8-25. THigh_Limit Register

15	14	13	12	11	10	9	8
THigh_Limit[13:6]							
R/W-2Ah							
7	6	5	4	3	2	1	0
THigh_Limit[5:0]						**Reserved**	
R/W-20h						R-0h	

Table 8-11. THigh_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	THigh_Limit[13:0]	R/W	0AA0h	14-bit temperature high limit setting. Temperature high limit is represented by a 14-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.03125°C.
1:0	Reserved	R	0h	These two bits will always read 0h

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8.6.7 Hysteresis Register (Address = 06h) [reset = 0A0Ah]

This register sets the hysteresis for the THigh_Limit threshold and the TLow_Limit threshold. The default hysteresis value for both the high and low limits is equal to 5 °C.

The Hysteresis is in a 8-bit unsigned format with the LSB equal to 0.5 °C. This gives a maximum value of 127.5 °C of hysteresis.

Return to Register Map.

Figure 8-26. Hysteresis Register

15	14	13	12	11	10	9	8
THigh_Hyst[7:0]							
R/W-0Ah							
7	6	5	4	3	2	1	0
TLow_Hyst[7:0]							
R/W-0Ah							

Table 8-12. Hysteresis Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	THigh_Hyst[7:0]	R/W	0Ah	THigh_Limit Hysteresis setting. Hysteresis value is represented by a unsigned byte with the LSB equal to 0.5 °C. The High temperature limit hysteresis threshold is equal to (THigh_Limit - THigh_Hyst). The default hysteresis value is 5 °C.
7:0	TLow_Hyst[7:0]	R/W	0Ah	TLow_Limit Hysteresis setting. Hysteresis value is represented by a unsigned byte with the LSB equal to 0.5 °C. The Low temperature limit hysteresis threshold is equal to (TLow_Limit + TLow_Hyst). The default hysteresis value is 5 °C.

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8.6.8 Slew_Limit Register (Address = 07h) [reset = 0500h]

This register is used to configure the temperature slew rate limit of the TMP126. The limit is formatted in a 13-bit unsigned format with the LSB (Least Significant Bit) equal to 0.03125 °C/s. The range of the register is 0 °C/s to +256 °C/s. The default value of Slew_Limit[12:6] on start-up is 0140h or 10 °C/s. The slew rate limit will trigger a slew rate alert on positive slew rates that are greater than the limit.

Return to Register Map.

Figure 8-27. Slew_Limit Register

15	14	13	12	11	10	9	8
Reserved	Slew_Limit[12:6]						
R-0h	R/W-05h						
7	6	5	4	3	2	1	0
Slew_Limit[5:0]						**Reserved**	
R/W-00h						R-0h	

Table 8-13. Slew_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	This bits will always read 0h
14:2	Slew_Limit[13:0]	R/W	0140h	13-bit temperature slew rate limit setting. Temperature low limit is represented by a 13-bit unsigned word with a LSB (Least Significant Bit) equal to 0.03125°C/s. The default setting for this is 10 °C/s.
1:0	Reserved	R	0h	These two bits will always read 0h

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8.6.9 Unique_ID1 Register (Address = 08h) [reset = xxxxh]

This register contains bits 47:32 of the Unique ID for the device. The Unique ID of the device is used for NIST traceability purposes.

Return to Register Map.

Figure 8-28. Unique_ID1 Register

15	14	13	12	11	10	9	8
Unique_ID[47:40]							
R-xxh							
7	6	5	4	3	2	1	0
Unique_ID[39:32]							
R-xxh							

Table 8-14. Unique_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Unique_ID[47:32]	R	xxxxh	Bits 47:32 of the device Unique ID

8.6.10 Unique_ID2 Register (Address = 09h) [reset = xxxxh]

This register contains bits 31:16 of the Unique ID for the device.

Return to Register Map.

Figure 8-29. Unique_ID2 Register

15	14	13	12	11	10	9	8
Unique_ID[31:24]							
R-xxh							
7	6	5	4	3	2	1	0
Unique_ID[23:16]							
R-xxh							

Table 8-15. Unique_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Unique_ID[31:16]	R	xxxxh	Bits 31:16 of the device Unique ID

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8.6.11 Unique_ID3 Register (Address = 0Ah) [reset = xxxxh]

This register contains bits 15:0 of the Unique ID for the device.

Return to Register Map.

Figure 8-30. Unique_ID3 Register

15	14	13	12	11	10	9	8
Unique_ID[15:8]							
R-xxh							
7	6	5	4	3	2	1	0
Unique_ID[7:0]							
R-xxh							

Table 8-16. Unique_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Unique_ID[15:0]	R	xxxxh	Bits 15:0 of the device Unique ID.

8.6.12 Device_ID Register (Address = 0Bh) [reset = 1114h]

This register indicates the device ID.

Return to Register Map.

Figure 8-31. Device_ID Register

15	14	13	12	11	10	9	8
Rev[3:0]				ID[11:8]			
R-1h				R-1h			
7	6	5	4	3	2	1	0
ID[7:0]							
R-14h							

Table 8-17. Device_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	Rev[3:0]	R	1h	Device revision indicator.
11:0	ID[11:0]	R	114h	Device ID indicator.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMP114 can be operated with a two-wire I²C or SMBus compatible interface and features the ability to operate with a 1.2-V bus voltage regardless of the VDD voltage. The TMP114 features a uniquely small z-height of 0.15 mm designed for low clearance and space-constrained applications.

The device also features an integrated optional CRC checksum for ensuring data integrity during communication.

9.2 Separate I²C Pullup and Supply Application

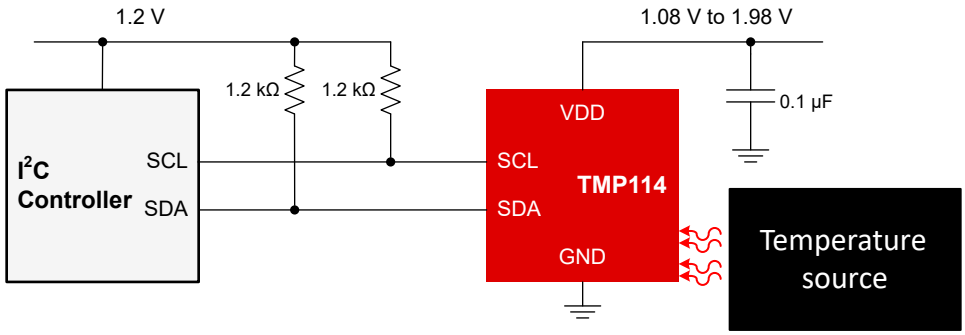

Figure 9-1. Separate I²C Pullup and Supply Voltage Application

9.2.1 Design Requirements

For this design example, use the parameters listed below.

Table 9-1. Design Parameters

Parameter	Value
Supply (V_{DD})	1.08 V to 1.98 V
SDA, SCL V_{PULLUP}	1.2 V
SDA, SCL R_{PULLUP}	1.2 kΩ

9.2.2 Detailed Design Procedure

The TMP114 will convert temperature at a default 250 ms interval with an adjustable conversion period between 6.4 ms and 2 s. The SDA and SCL pin voltage of the TMP114 can be at a higher voltage than the VDD pin voltage, removing the need for power sequencing when using the TMP114.

The TMP114 comes in an ultra-small body and z-height package the user can place as close to temperature sources as possible for better thermal coupling.

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9.2.3 Application Curves

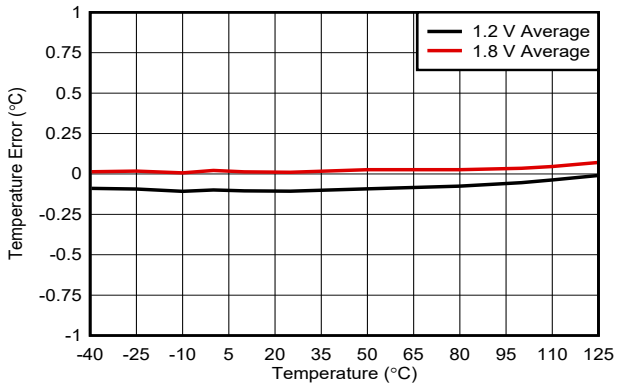

Figure 9-2. Average Temperature Accuracy

9.3 Equal I²C Pullup and Supply Voltage Application

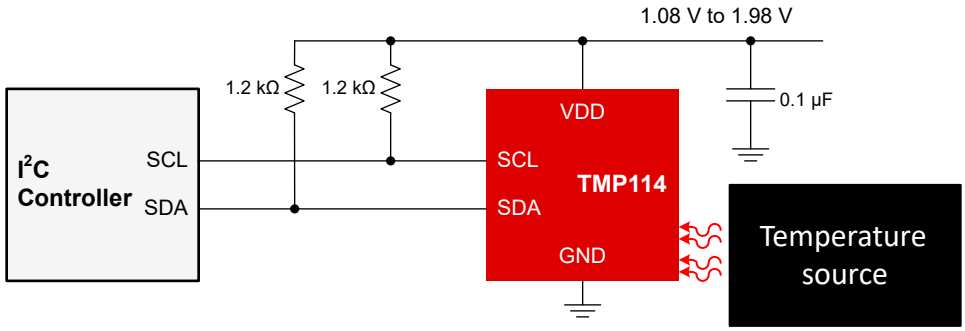

Figure 9-3. Equal I²C Pullup and Supply Voltage Application

9.3.1 Design Requirements

For this design example, use the parameters listed below.

Table 9-2. Design Parameters

Parameter	Value
Supply (V_{DD})	1.08 V to 1.98 V
SDA, SCL V_{PULLUP}	V_{DD}
SDA, SCL R_{PULLUP}	1.2 kΩ

9.3.2 Detailed Design Procedure

The SDA and SCL pin voltage of the TMP114 can be the same as the supply voltage V_{DD}. The accuracy of the TMP114 is not affected by the pullup voltage.

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10 Power Supply Recommendations

The TMP114 operates with power supply in the range of 1.08 V to 1.98 V. The device can measure temperature accurately in the full supply range. A power-supply bypass capacitor is required for proper operation. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

11 Layout

11.1 Layout Guidelines

The TMP114 is a simple device to layout. Place the power supply bypass capacitor as close to the device as possible, and connect the capacitor as shown in Figure 11-1. Pull up the open-drain output pin SDA and the I^2C clock SCL through R_{PULLUP} pullup resistors.

11.2 Layout Example

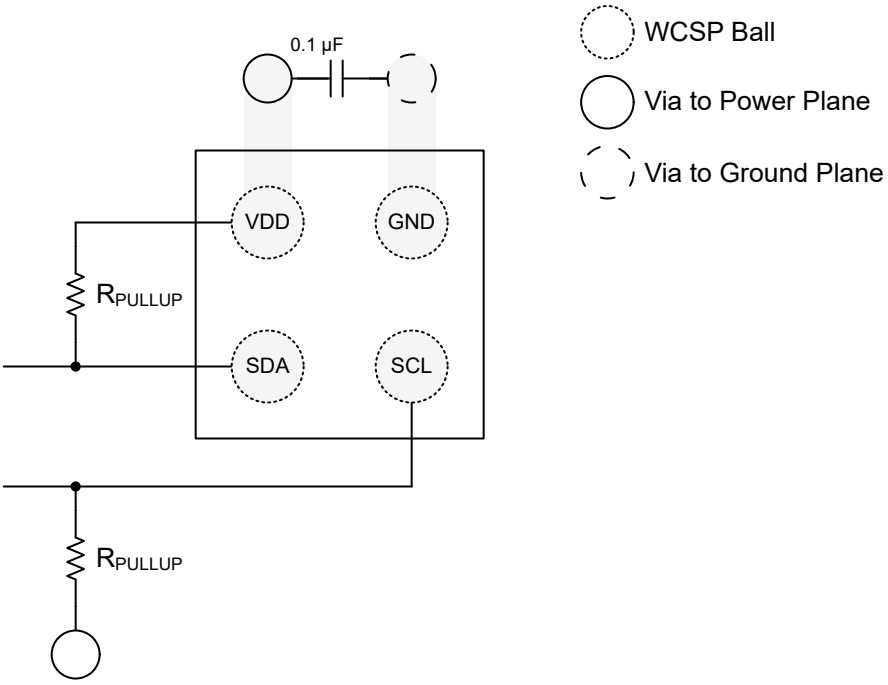

Figure 11-1. Layout Recommendation (Top View)

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Table 13-1. YMT Package D and E Dimensions

	MIN	NOM	MAX
D	0.750 mm	0.758 mm	0.766 mm
E	0.750 mm	0.758 mm	0.766 mm
C (Seating Plane)			20 µm

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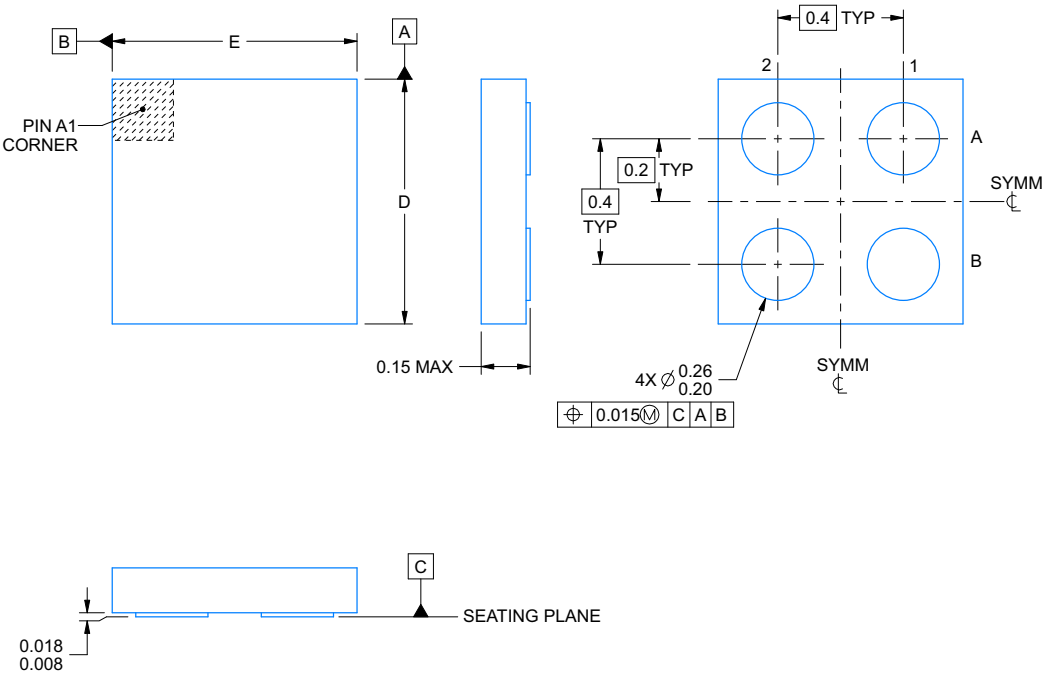
PACKAGE OUTLINE

YMT0004

PicoStar ™ - 0.15 mm max height

PicoStar



4225388/B 08/2020

PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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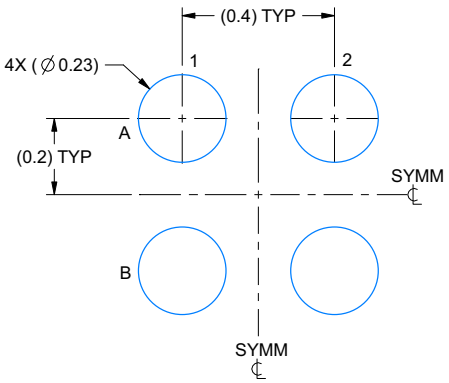
EXAMPLE BOARD LAYOUT

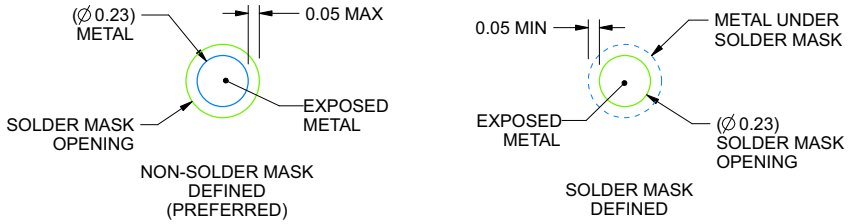
YMT0004

PicoStar ™ - 0.15 mm max height

PicoStar



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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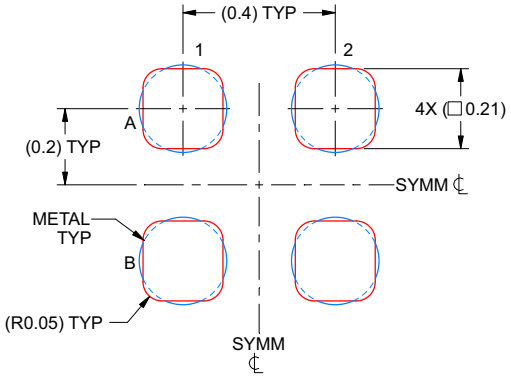
EXAMPLE STENCIL DESIGN

YMT0004

PicoStar ™ - 0.15 mm max height

PicoStar



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE:60X

4225388/B 08/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP114AIYMTR	ACTIVE	PICOSTAR	YMT	4	3000	RoHS & Green	CUNIPD	Level-1-260C-UNLIM	-40 to 125		Samples
TMP114AIYMTT	ACTIVE	PICOSTAR	YMT	4	250	RoHS & Green	CUNIPD	Level-1-260C-UNLIM	-40 to 125		Samples
TMP114BIYMTR	ACTIVE	PICOSTAR	YMT	4	3000	RoHS & Green	CUNIPD	Level-1-260C-UNLIM	-40 to 125	YS	Samples
TMP114CIYMTR	ACTIVE	PICOSTAR	YMT	4	3000	RoHS & Green	CUNIPD	Level-1-260C-UNLIM	-40 to 125	YS	Samples
TMP114DIYMTR	ACTIVE	PICOSTAR	YMT	4	3000	RoHS & Green	CUNIPD	Level-1-260C-UNLIM	-40 to 125	YS	Samples
TMP114NAIYMTR	ACTIVE	PICOSTAR	YMT	4	3000	RoHS & Green	CUNIPD	Level-1-260C-UNLIM	-40 to 125	YS	Samples
TMP114NAIYMTT	ACTIVE	PICOSTAR	YMT	4	250	RoHS & Green	CUNIPD	Level-1-260C-UNLIM	-40 to 125	YS	Samples
TMP114NBIYMTR	ACTIVE	PICOSTAR	YMT	4	3000	RoHS & Green	CUNIPD	Level-1-260C-UNLIM	-40 to 125	YS	Samples
TMP114NCIYMTR	ACTIVE	PICOSTAR	YMT	4	3000	RoHS & Green	CUNIPD	Level-1-260C-UNLIM	-40 to 125	YS	Samples
TMP114NDIYMTR	ACTIVE	PICOSTAR	YMT	4	3000	RoHS & Green	CUNIPD	Level-1-260C-UNLIM	-40 to 125	YS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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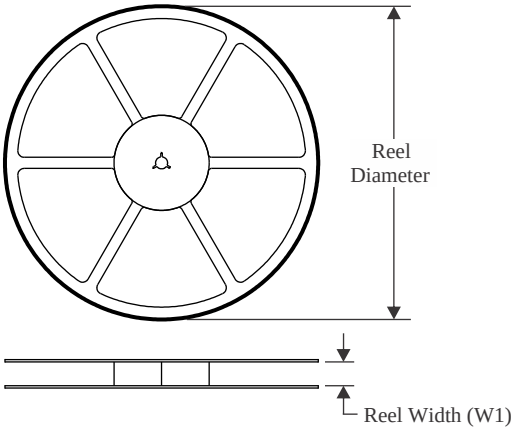
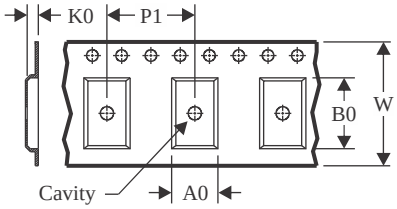
TAPE AND REEL INFORMATION

REEL DIMENSIONS

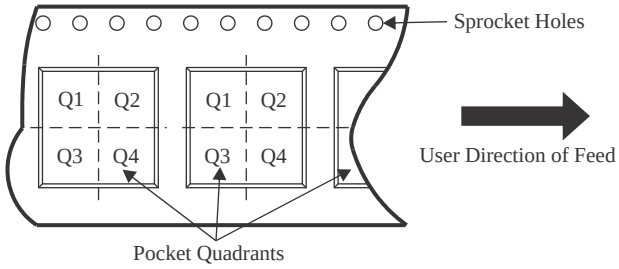


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

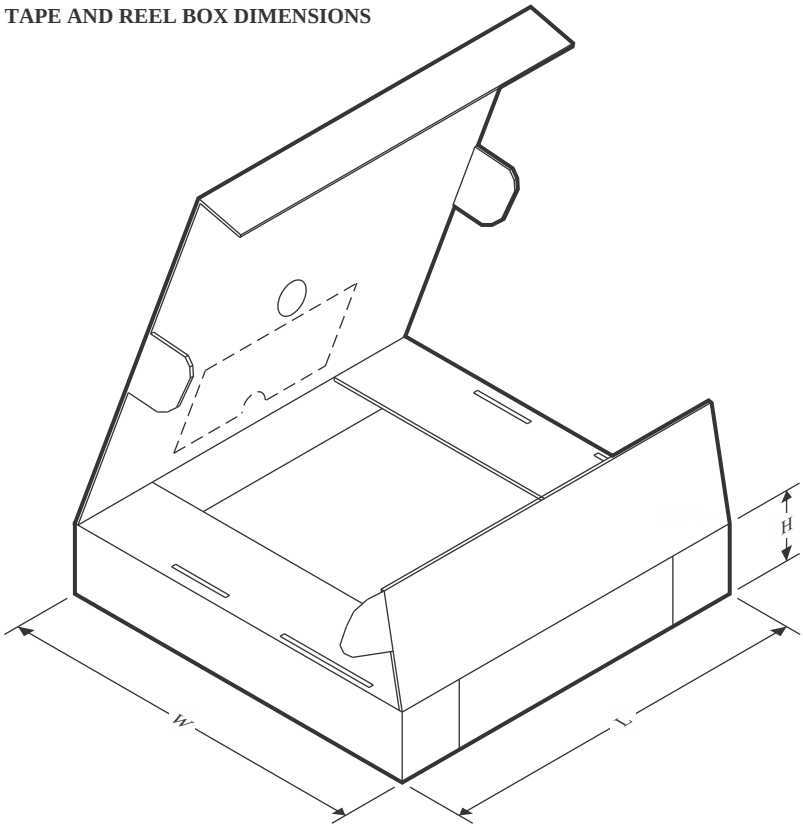
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP114AIYMTR	PICOSTAR	YMT	4	3000	180.0	8.4	0.85	0.85	0.23	2.0	8.0	Q1
TMP114AIYMTT	PICOSTAR	YMT	4	250	180.0	8.4	0.85	0.85	0.23	2.0	8.0	Q1
TMP114BIYMTR	PICOSTAR	YMT	4	3000	180.0	8.4	0.85	0.85	0.23	2.0	8.0	Q1
TMP114CIYMTR	PICOSTAR	YMT	4	3000	180.0	8.4	0.85	0.85	0.23	2.0	8.0	Q1
TMP114DIYMTR	PICOSTAR	YMT	4	3000	180.0	8.4	0.85	0.85	0.23	2.0	8.0	Q1
TMP114NAIYMTR	PICOSTAR	YMT	4	3000	180.0	8.4	0.85	0.85	0.23	2.0	8.0	Q1
TMP114NAIYMTT	PICOSTAR	YMT	4	250	180.0	8.4	0.85	0.85	0.23	2.0	8.0	Q1
TMP114NBIYMTR	PICOSTAR	YMT	4	3000	180.0	8.4	0.85	0.85	0.23	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP114AIYMTR	PICOSTAR	YMT	4	3000	182.0	182.0	20.0
TMP114AIYMTT	PICOSTAR	YMT	4	250	182.0	182.0	20.0
TMP114BIYMTR	PICOSTAR	YMT	4	3000	182.0	182.0	20.0
TMP114CIYMTR	PICOSTAR	YMT	4	3000	182.0	182.0	20.0
TMP114DIYMTR	PICOSTAR	YMT	4	3000	182.0	182.0	20.0
TMP114NAIYMTR	PICOSTAR	YMT	4	3000	182.0	182.0	20.0
TMP114NAIYMTT	PICOSTAR	YMT	4	250	182.0	182.0	20.0
TMP114NBIYMTR	PICOSTAR	YMT	4	3000	182.0	182.0	20.0

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