Product Change Notification - SYST-19YTNN552

Date: 20 Apr 2017

Product Category: 32-bit PIC Microcontrollers

Affected CPNs:

Notification subject: Data Sheet - SAM L22 Datasheet

Notification text: SYST-19YTNN552

Microchip has released a new DeviceDoc for the SAM L22 Datasheet of devices. If you are using one of these devices please read the document located at SAM L22 Datasheet.

Notification Status: Final

Description of Change:
1) Change of document style and New Microchip document number from previous version of Atmel document 42402 rev.E.)
2) Added package UFBGA100 and updated colors and legends in pinout diagrams and editorial updates.
3) Editorial updates on PAC - Peripheral Access Controller, FREQM – Frequency Meter, SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter, CCL – Configurable Custom Logic and PTC - Peripheral Touch Controller.
4) Register BOD12 is PAC Write-Protected and write-Synchronized on SUPC – Supply Controller and editorial updates.
5) Register CONFIG is not Enable-protected for WDT – Watchdog Timer
6) In RTC – Real-Time Counter, added Functional description of General Purpose registers, updated Bit field position updated: CTRLB.ACTF, CTRLB.DEBF, SYNCBUSY.GPn and editorial updates
7) STEPSIZE factor in SRAM register BTCTRL is based on beat size in bytes and Editorial updates for DMAC – Direct Memory Access Controller
8) NVMCTRL – Non-Volatile Memory Controller have 16 region locks available.
9) Notes added on PINCFG and PMUX registers are repeated per PORT group with offset 0x80 for PORT - I/O Pin Controller and bit PORT.CTRL.SAMPLING is write-only.
10) For TC – Timer/Counter, Register representation re-organized, CTRLA.SWRST is write-only, STATUS register is Read-Synchronized and Editorial updates.
11) Registers PER, PATT are Write-Synchronized, Bit fields in PATBYF register are 8 bit in size, Bit field TCC.DBGCTRL.FDDBD: Default '0' is OCD fault protection disabled For TCC – Timer/Counter for Control Applications.
12) TRNG – True Random Number Generator's Bit field DATA.DATA is R/W and AES – Advanced Encryption Standard Register DBGCTRL is not enable-protected also made editorial updates.
13) The USB – Universal Serial Bus Device STATUS register has reset value of 0x40 and made editorial updates.
14) For Electrical Characteristics FDPLL96M: Maximum FOUT 96MHz in PL2, and 48MHz in PL0.
15) On Schematic Checklist, Leave VLCD pin unconnected when the LCD controller is not used and made Editorial updates.
16) New errata for SERCOM: In USART autobaud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors. Errata reference 13852
17) New errata for EIC: Changing the NMI configuration (CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt. Errata reference 15279
18) New errata for ADC: Clock request not going low in standby mode. Errata reference 15463
19) New errata for PORT: PORT read/write attempts on nonimplemented registers, including addresses beyond the last implemented register group (PA, PB, …) do not generate a PAC protection error. Errata reference 15611
20) New errata for TCC: Using dithering mode with external retrigger events can lead to unexpected stretch of right aligned pulses, or shrink of left aligned pulses. Errata reference 15625
21) New errata for DMAC: When using more than one DMA channel and one of them is w/linked descriptor, a fetch error can appear on this channel. Errata reference 15670
22) New errata for DMAC: When at least one channel w/linked descriptors is already active, and the channel number of the channel being enabled is lower than the channel already active, enabling another DMA channel can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch. Errata reference 15683
23) New errata for FDPLL: When changing on-the-fly the FDPLL ratio in DPLLnRATIO register, STATUS.DPLLnLDRTO will not be set when the ratio update will be completed. Errata reference 15753

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 20 April 2017

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s): SAM L22 Datasheet

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

Affected Catalog Part Numbers (CPN)

ATSAML22G16A-MUT
ATSAML22G16A-AUT
ATSAML22J16A-MUT
ATSAML22J16A-AUT
ATSAML22J18A-MUT
ATSAML22J18A-AUT
ATSAML22N17A-CFUT
ATSAML22N17A-AUT
ATSAML22G17A-UUTA0
ATSAML22G17A-UUT
ATSAML22G17A-MUT
ATSAML22G17A-AUT
ATSAML22N18A-W-NG
ATSAML22N18A-W
ATSAML22N18A-CFUT
ATSAML22N18A-AUT
ATSAML22J17A-MUT
ATSAML22J17A-AUT
ATSAML22N16A-CFUT
ATSAML22N16A-AUT
ATSAML22G18A-UUT
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