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APPLICATION NOTE 3777

Using Software to Shape the Transmit Pulse of the DS325x LIUs

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Abstract: This application note describes how to adjust the transmit pulse settings, both amplitude and shape, of the DS3254, DS3253, DS3252, and DS3251 DS3, E3, STS-1 line interface units (LIUs) without having to modify external components.

Introduction

The default operation of the [DS3254](#), [DS3253](#), [DS3252](#), and [DS3251](#) DS3, E3, STS-1 line interface units (LIUs) will always produce a transmit pulse that is within specifications. Nonetheless, it may become necessary, or desirable, to alter the pulse output to conform to specific application needs. This application note explains which registers to change and the pulse adjustments that will result. The article also identifies the settings for both pulse amplitude and pulse shape which will help ensure satisfactory results.

Amplitude Adjustments

Using the register below, the user can control the amplitude of the transmit pulse.

Register Name: Test Register C

Register Address: 0Ah

Register Description: Bits 6 through 3 of Test Register C (TESTC.6 - TESTC.3) adjust transmitter amplitude. The effects of the bits settings are additive, except in the case of TESTC.6 = 1 and TESTC.5 = 1 which override all amplitude settings.

Bit 7: This bit must be set to zero for proper operation.

Bits 6, 5: These bits are decoded together according to the table below.

Bit 6	Bit 5	Amplitude Adjustment
0	0	No amplitude adjustment
0	1	Amplitude raised by 8%
1	0	Amplitude lowered by 8%

1	1	Amplitude raised to current limiter threshold (amplitude, max)
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Bit 4: Amplitude raised 4%.

Bit 3: Amplitude raised 2%.

Pulse Width and Shape Adjustments

Using the register below, the user can control the shape of the transmit pulse.

Register Name: Test Register C

Register Address: 0Ah

Register Description: Bits 2 through 0 of Test Register C (TESTC.2 through TESTC.0) are used to invoke various mutually exclusive adjustments to the transmitter pulse shape. These bits can be used to adjust pulse mask fitting.

Bits 2 through 0: These bits are decoded together according to the table below.

Bit 2	Bit 1	Bit 0	Pulse shape adjustment
0	0	0	No pulse adjustment
0	0	1	Make pulse ~0.8ns wider (DS3/STS-1, LBO = 0 Mode Only)
0	1	0	Make pulse ~0.8ns narrower (DS3/STS-1, LBO = 1 Mode Only) Make pulse ~1.1 ns narrower (E3 Mode Only)
0	1	1	Flattens top of pulse slightly
1	0	0	Not useful (Do not use.)
1	0	1	Force square pulses (Forces E3 mode in the wave shape circuit.)
1	1	0	Not useful (Do not use.)
1	1	1	Not useful (Do not use.)

Register Name: Test Register D

Register Address: 0Bh

Register Description: This register has different effects depending on the mode of operation. Because the transmit pulse is constructed in piecewise linear fashion, the wave shape can be altered by adjusting the relative durations of the various segments. Besides pulse construction in DS3 and STS-1 modes, lowpass filtering also occurs. In all modes, the pulse amplitude remains unaffected by these settings.

In DS3 and STS-1 modes, bits 7 and 3 through 0 of Test Register D (TESTD.7, TESTD.3 through TESTD.0) adjust the wave shape by varying the durations of the ramp period.

In E3 mode, bits 7 and 4 through 0 of Test Register D (TESTD.7, TESTD.4 through TESTD.0) adjust wave shape by varying the durations of the ramp period.

DS3 and STS-1 Mode Settings

In the DS3 and STS-1 modes, the lower four bits operate more or less independently, so any combination of settings can be used. For example, setting both bits 1 and 2 makes the pulse slightly wider with a flatter top. Setting bits 0 and 3 makes the pulse wider, but with a more sharply peaked top. Setting all four bits gives a wider pulse without much change to the shape.

Bit 7: Doubles the trailing undershoot effects of bits TESTD.3 and TESTD.0.

Bit 6 - 4: These bits must be set to zero for proper operation.

Bit 3: Increases the level of the trailing undershoot. This is achieved by increasing the duration that the wave-shape circuit drives the falling edge of the pulse.

Bit 2: Lengthens the second half of the top of the pulse (slightly increases undershoot).

Bit 1: Lengthens the first half of the top of the pulse (slightly decreases undershoot).

Bit 0: Decreases the level of the trailing undershoot. This is achieved by increasing the duration that the wave-shape circuit drives the rising edge of the pulse. This operation will not affect the pulse amplitude which is controlled independently.

E3 Mode Settings

In E3 mode, the bits mostly affect the pulse's duration because the ideal pulse is square. However, bit 4 does affect the leading edge shape. In addition, the pulse top can be flattened by increasing the amplitude (TESTC6:3) while decreasing the external load resistor (which lowers the amplitude).

Bit 7: Doubles the effect of bit TESTD.0.

Bit 6, 5: These bits must be set to zero for proper operation.

Bit 4: Sharpens the leading edge of the pulse.

Bit 3: Shortens the pulse by $\sim 0.25\text{ns}$ (This bit has no effect if TESTD.7 = 1).

Bit 2: Lengthens the pulse by $\sim 0.25\text{ns}$.

Bit 1: Lengthens the pulse by $\sim 0.25\text{ns}$.

Bit 0: Lengthens the pulse by $\sim 0.25\text{ns}$ ($\sim 0.5\text{ns}$ if TESTD.7 = 1)

References

If you have additional questions on LIU initialization and configuration, please contact the [Telecommunication Applications support team](#).

For more information about the DS3254, DS3253, DS3252, or DS3251 line interface units please consult the appropriate data sheet which is available on the Maxim website at: [T/E Carrier and Packetized Products](#).

Related Parts

DS3251	Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs	Free Samples
DS3252	Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs	Free Samples
DS3253	Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs	Free Samples
DS3254	Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs	Free Samples

More Information

For Technical Support: <http://www.maximintegrated.com/support>

For Samples: <http://www.maximintegrated.com/samples>

Other Questions and Comments: <http://www.maximintegrated.com/contact>

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