LH5164A/AH

CMOS 64K (8K × 8) Static RAM

FEATURES

- 8,192 × 8 bit organization
- Access times: 80/100 ns (MAX.)
- Low-power consumption:
  - Operating:
    - 303 mW (MAX.) LH5164A/D/N
      @ 80 ns
    - 248 mW (MAX.) LH5164A/D/N/T
      @ 100 ns
    - 275 mW (MAX.) LH5164AH/HD/HN/HT
      @ 100 ns
  - Standby:
    - LH5164A/D/N/T: 5.5 µW (MAX.)
    - LH5164AH/HD/HN/HT:
      - $T_A \leq 85°C$: 16.5 µW (MAX.)
      - $T_A \leq 70°C$: 5.5 µW (MAX.)
- Fully-static operation
- Three-state outputs
- Single +5 V power supply
- TTL compatible I/O
- Wide temperature range available
  - LH5164A: -10 to +70°C
  - LH5164AH: -40 to +85°C
- Packages:
  - 28-pin, 600-mil DIP
  - 28-pin, 300-mil SK-DIP
  - 28-pin, 450-mil SOP
  - 28-pin, 8 × 13 mm^2 TSOP (Type I)

DESCRIPTION

The LH5164A/AH are static RAMs organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5164AH is designed for wide temperature range from -40 to +85°C.

PIN CONNECTIONS

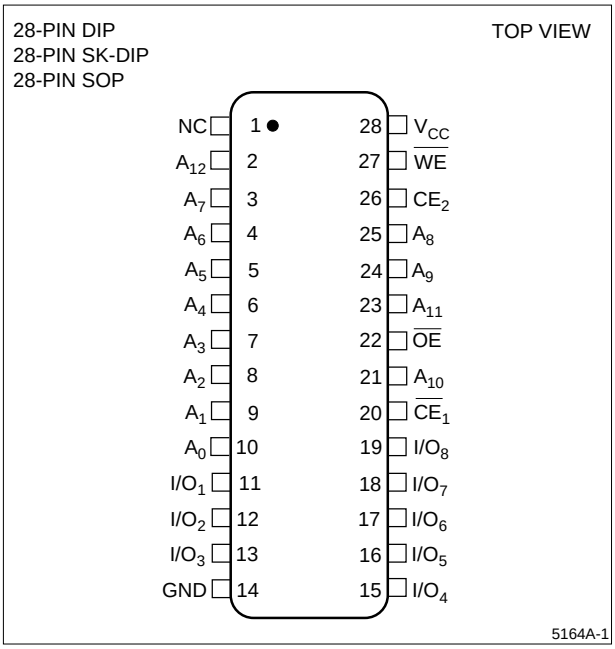


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

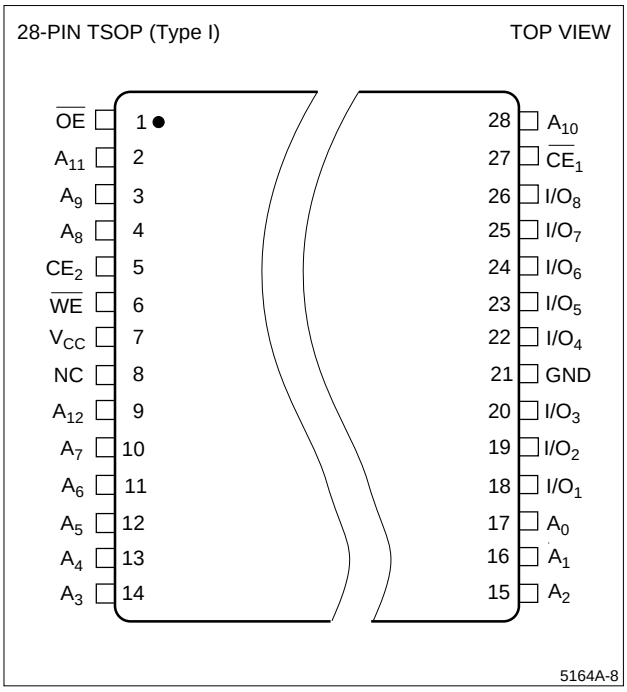


Figure 2. Pin Connections for TSOP Package

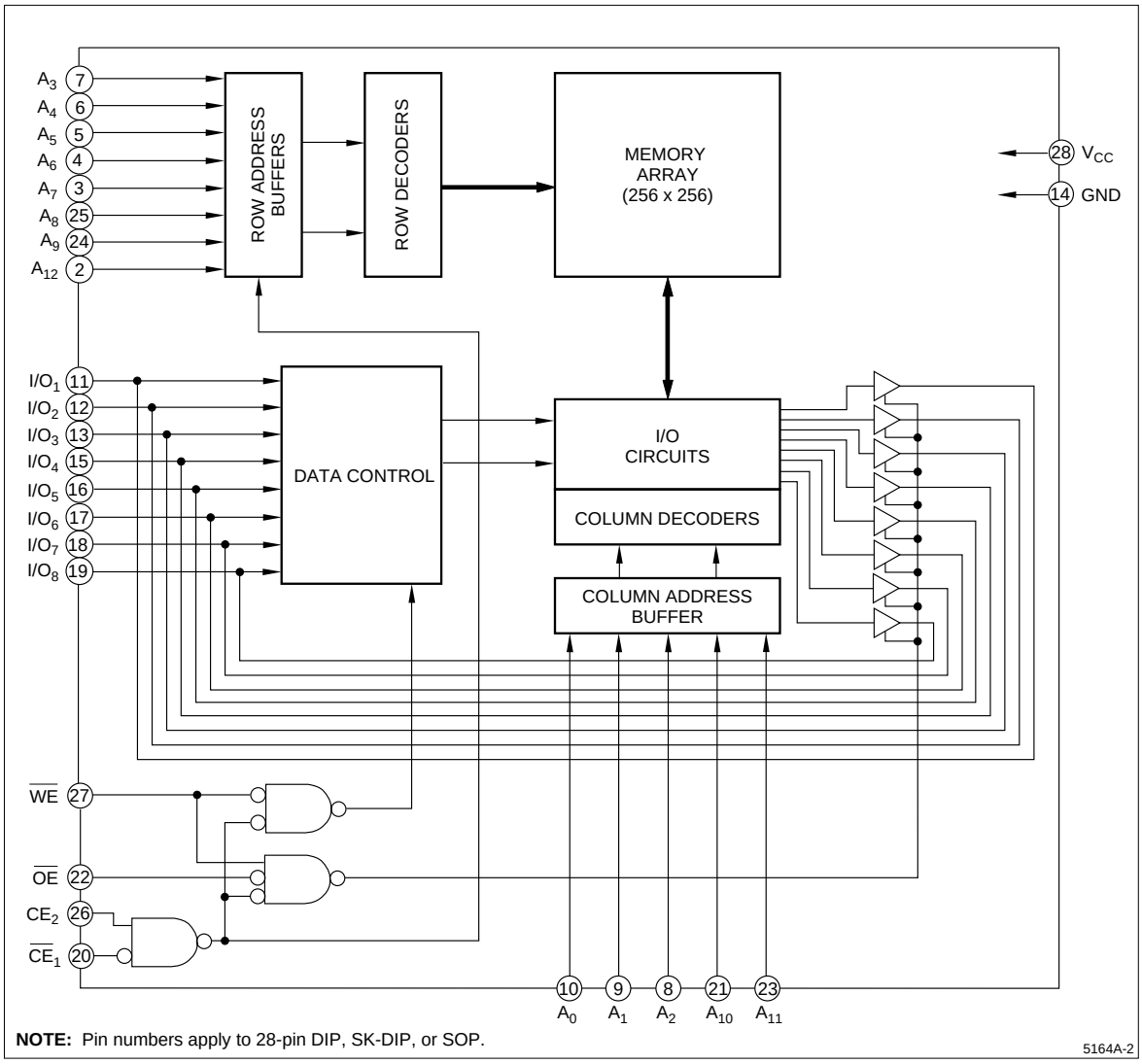


Figure 3. LH5164A/AH Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE_1}$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	No connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I_{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	80 ns RATING	100 ns RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	-0.3 to V_{CC} + 0.3	V	1, 2
Operating temperature	Topr	-10 to +70	-10 to +70	°C	3
			-40 to +85	°C	4
Storage temperature	Tstg	-55 to +150	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. V_{IN} (MIN.) = -3.0 V for pulse width ≤50 ns.
3. LH5164A/AD/AN/AT
4. LH5164AH/AHD/AHN/AHT

RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	80 ns MIN.	80 ns TYP.	80 ns MAX.	100 ns MIN.	100 ns TYP.	100 ns MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	V	
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	2.2		V_{CC} + 0.3	V	
	V_{IL}	-0.3		0.8	-0.3		0.8	V	2

NOTES:
1. T_A = -10 to +70°C (LH5164A/AD/AN/AT), T_A = -40 to +85°C (LH5164AH/AHD/AHN/AHT).
2. V_{IN} (MIN.) = -3.0 V for pulse width ≤50 ns.

DC CHARACTERISTICS [1] (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}		-1.0	1.0	µA	
Output leakage current	I_{LO}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}		-1.0	1.0	µA	
Operating current	I_{CC}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH} CE_2 = V_{IH}, Outputs open	t_{CYCLE} = 80 ns		55	mA	
		$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH} CE_2 = V_{IH}, Outputs open	t_{CYCLE} = 100 ns		45	mA	2
					50		3
		$\overline{CE_1}$ = V_{IL}, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{IH}, Outputs open	t_{CYCLE} = 1.0 µs		10		
Standby current	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			5	mA	
		CE_2 ≤ 0.2 V or $\overline{CE_1}$ ≥ V_{CC} - 0.2 V	T_A ≤ 70°C		1.0	µA	2, 3, 4
			T_A ≤ 85°C		3.0	µA	3, 4
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
	V_{OH}	I_{OH} = -1 mA		2.4		V	

NOTES:
1. T_A = -10 to 70°C (LH5164A/AD/AN/AT), T_A = -40 to +85°C (LH5164AH/AHD/AHN/AHT)
2. LH5164A/AD/AN/AT
3. LH5164AH/AHD/AHN/AHT
4. CE_2 should be ≥ V_{CC} – 0.2 V or ≤ 0.2 V when $\overline{CE_1}$ ≥ V_{CC} – 0.2 V

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ±10%)

PARAMETER		SYMBOL	80 ns		100 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
Read cycle time		t_{RC}	80		100		ns	
Address access time		t_{AA}		80		100	ns	
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		80		100	ns	
	(CE_2)	t_{ACE2}		80		100	ns	
Output enable access time		t_{OE}		40		40	ns	
Output hold time		t_{OH}	10		10		ns	
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	10		10		ns	1
	(CE_2)	t_{LZ2}	10		10		ns	1
Output enable to output in Low-Z		t_{OLZ}	5		5		ns	1
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	30	0	30	ns	1
	(CE_2)	t_{HZ2}	0	30	0	30	ns	1
Output disable to output in High-Z		t_{OHZ}	0	20	0	20	ns	1

(2) WRITE CYCLE (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	80 ns		100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	80		100		ns	
Chip enable to end of write	t_{CW}	70		80		ns	
Address valid to end of write	t_{AW}	70		80		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	60		60		ns	
Write recovery time	t_{WR}	0		0		ns	
Data valid to end of write	t_{DW}	40		40		ns	
Data hold time	t_{DH}	0		0		ns	
Output active from end of write	t_{OW}	10		10		ns	2
$\overline{WE}$ to output in High-Z	t_{WZ}	0	30	0	30	ns	2
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	20	0	20	ns	2

NOTES:

1. T_A = -10 to +70°C (LH5164A/AD/AN/AT), T_A = -40 to +85°C (LH5164AH/AHD/AHN/AHT)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

AC TEST CONDITIONS

PARAMETER	MODE	NOTE
Input voltage amplitude	0.6 to 2.4 V	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load conditions	1TTL + C_L (100 pF)	1

NOTE:

1. Includes scope and jig capacitance.

CAPACITANCE [1] (T_A = 25°C, f = 1 MHz)

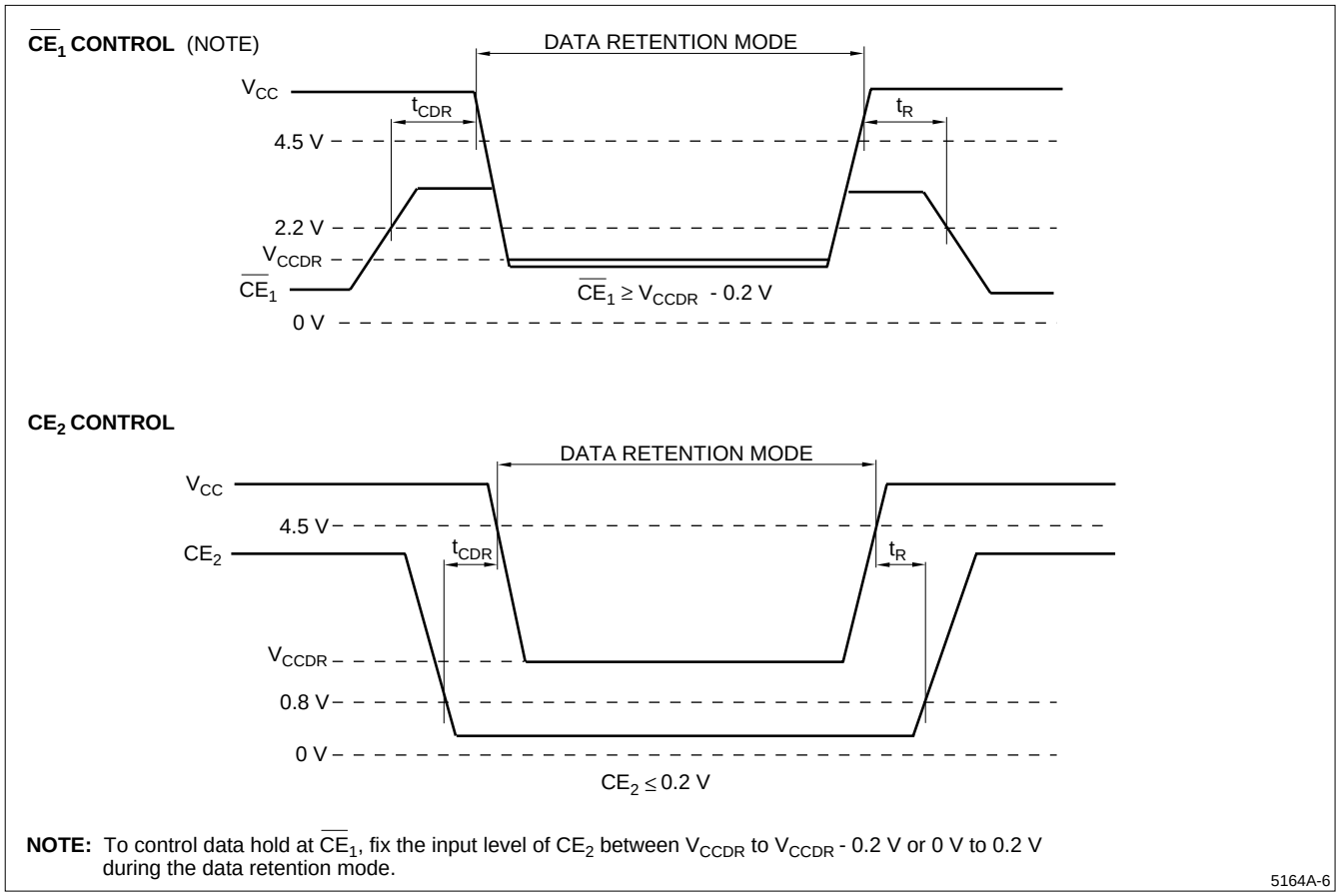
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE_2} \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR}$ - 0.2 V		2.0	5.5	V	2
Data retention current	I_{CCDR}	V_{CCDR} = 3 V, $\overline{CE_2} \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR}$ - 0.2 V	T_A = 25°C		0.2	µA	2, 3
			T_A = 40°C		0.4	µA	2, 3
					0.6	µA	2, 3
		V_{CCDR} = 3 V, $\overline{CE_2} \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR}$ - 0.2 V	T_A = 25°C		0.2	µA	2, 4
			T_A = 70°C		0.6	µA	2, 4
					1.5	µA	2, 4
Chip disable to data retention	t_{CDR}			0		ns	
Recovery time	t_R			t_{RC}		ns	5

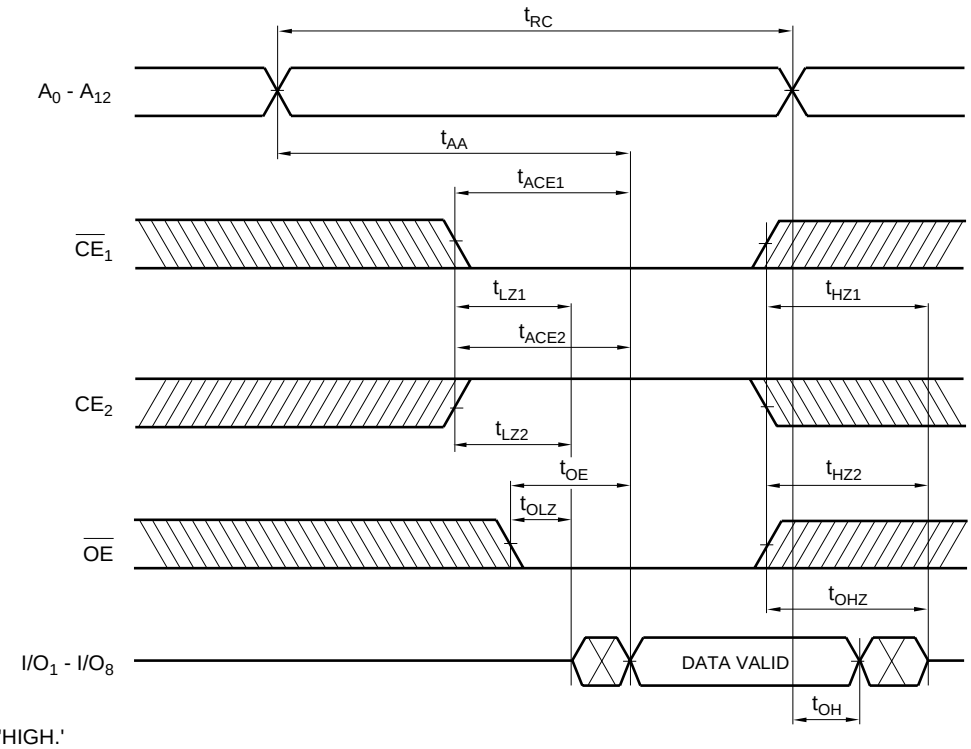
NOTES:
1. T_A = -10 to +70°C (LH5164A/AD/AN/AT), T_A = -40 to +85°C (LH5164AH/AHD/AHN/AHT)
2. $\overline{CE_2}$ should be ≥ V_{CCDR} - 0.2 V or ≤ 0.2 V when $\overline{CE_1} \ge V_{CCDR}$ – 0.2 V
3. LH5164A/AD/AN/AT
4. LH5164AH/AHD/AHN/AHT
5. t_{RC} = Read cycle time



NOTE: To control data hold at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} - 0.2 V or 0 V to 0.2 V during the data retention mode.

5164A-6

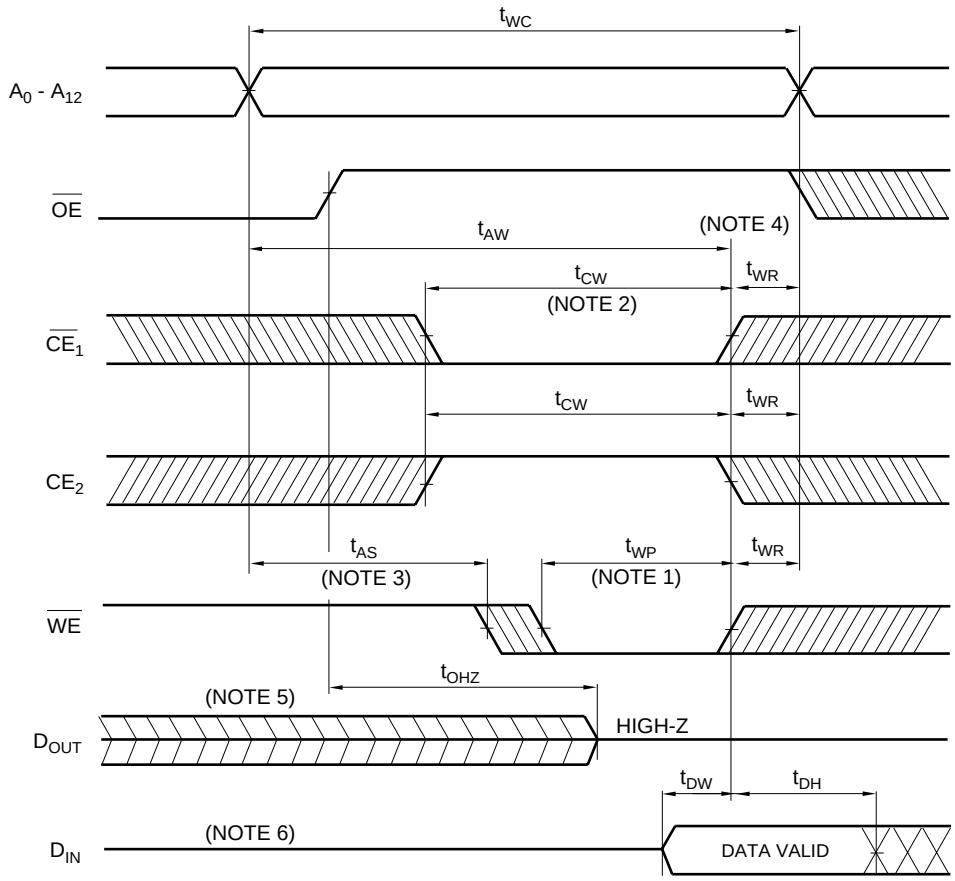
Figure 4. Low Voltage Data Retention



NOTE: $\overline{WE}$ = 'HIGH.'

5164A-3

Figure 5. Read Cycle

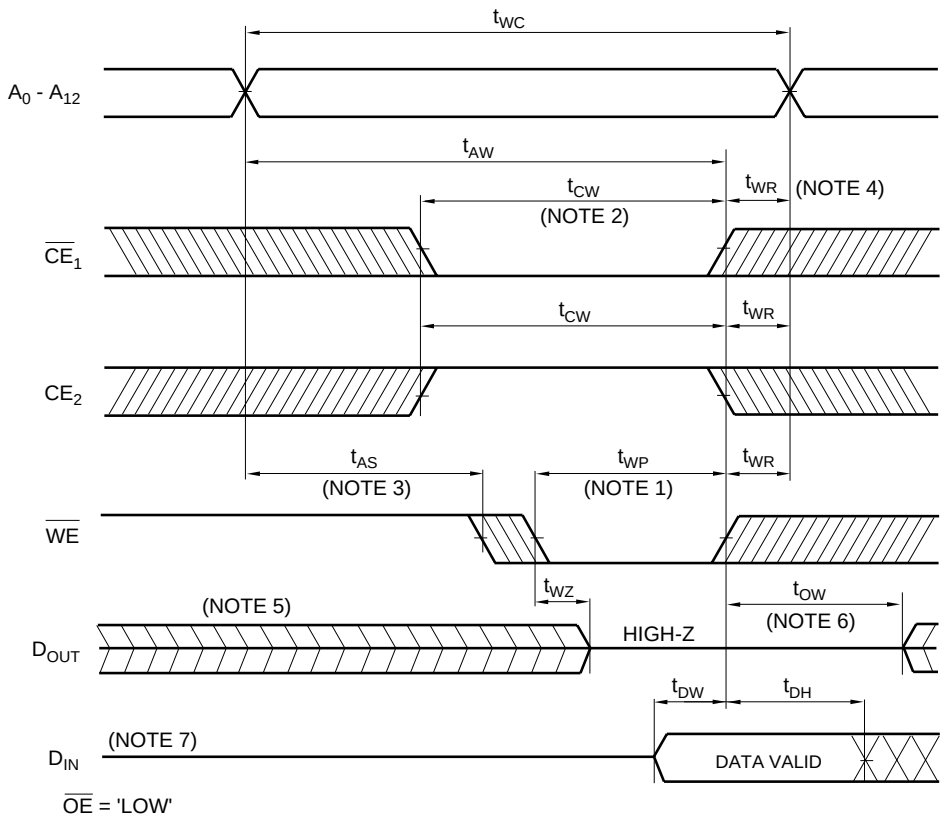


NOTES:

1. The writing occurs during an overlapping period of $\overline{CE_1}$ = 'LOW,' CE_2 = 'HIGH,' and $\overline{WE}$ = 'LOW' (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
6. While I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5164A-4

Figure 6. Write Cycle 1



NOTES:

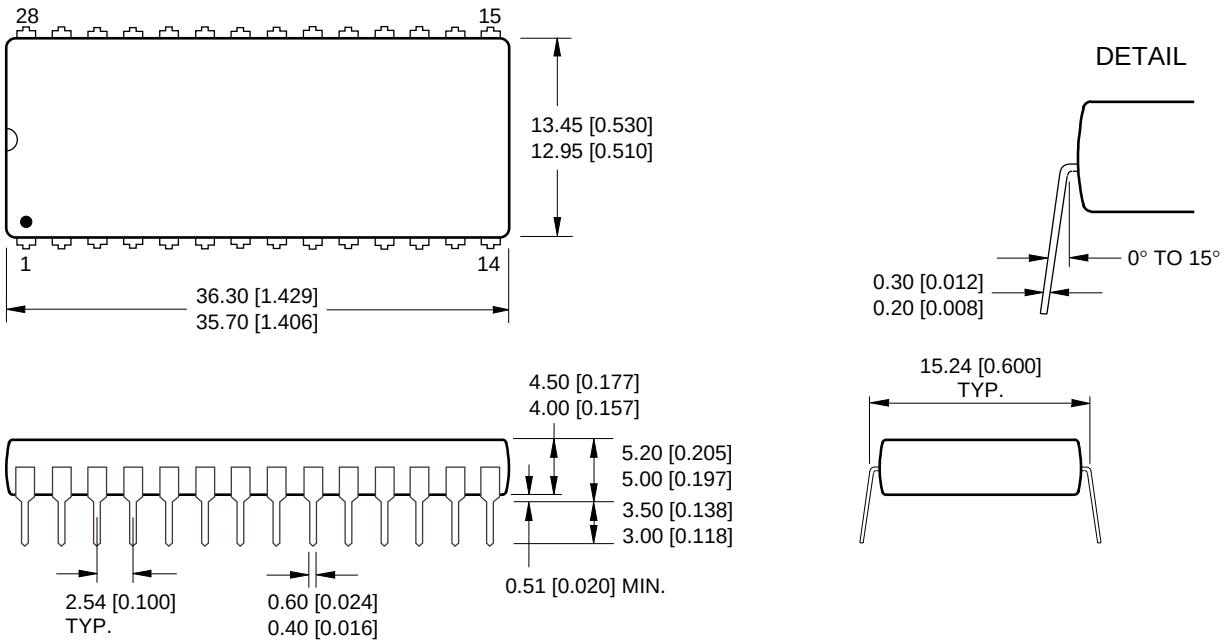
1. The writing occurs during an overlapping period of $\overline{CE_1}$ = 'LOW,' CE_2 = 'HIGH,' and $\overline{WE}$ = 'LOW' (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the outputs will remain high-impedance.
7. While I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5164A-5

Figure 7. Write Cycle 2

PACKAGE DIAGRAMS

28DIP (DIP028-P-0600)

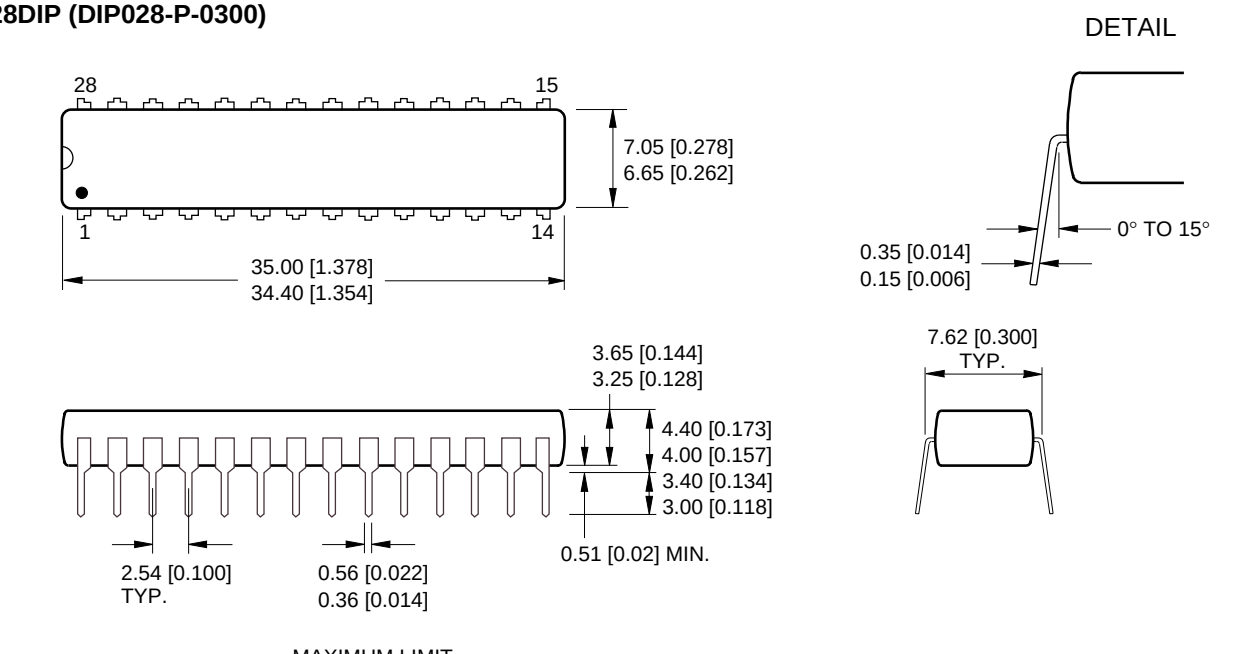


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-2

28-pin, 600-mil DIP

28DIP (DIP028-P-0300)

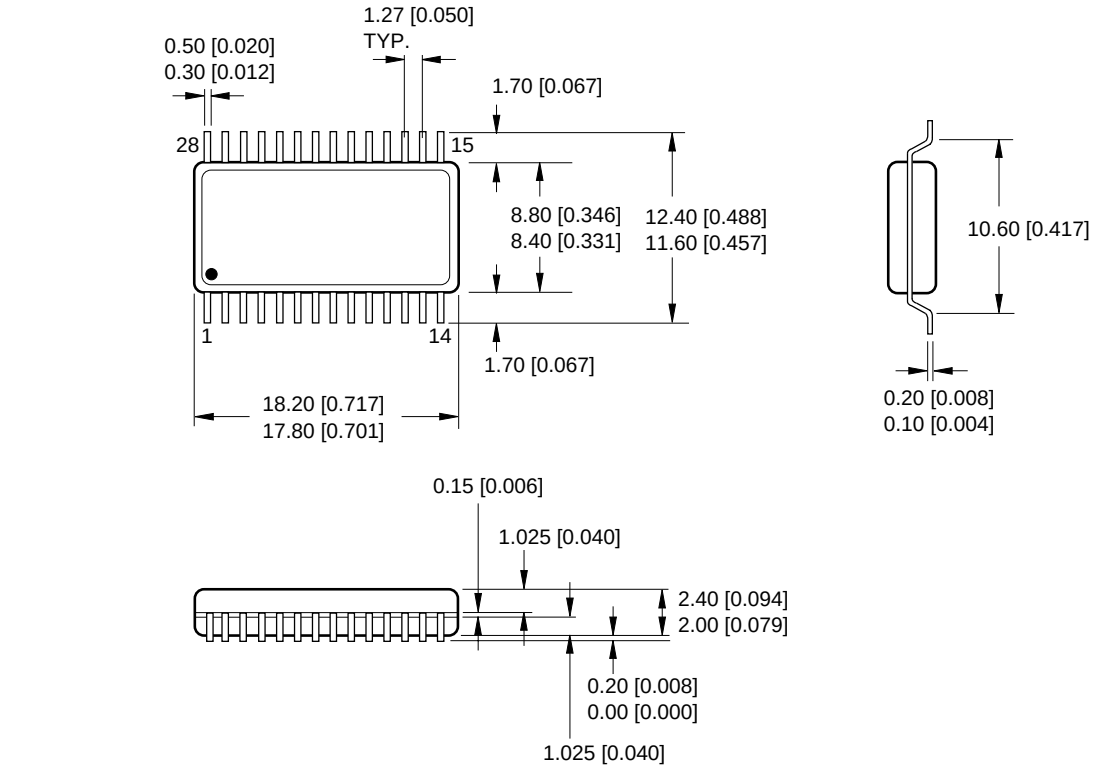


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-6

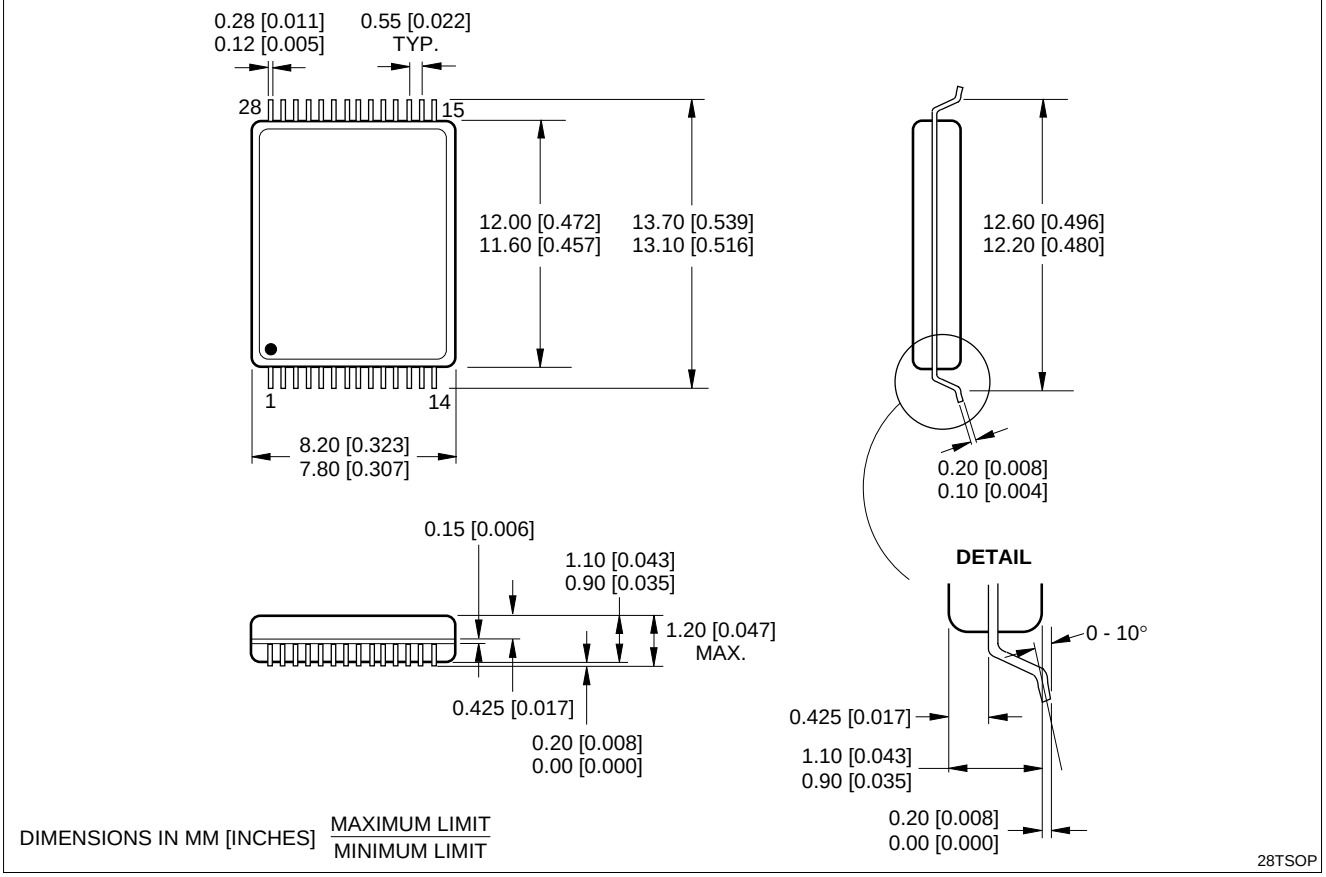
28-pin, 300-mil SK-DIP

28SOP (SOP028-P-0450)



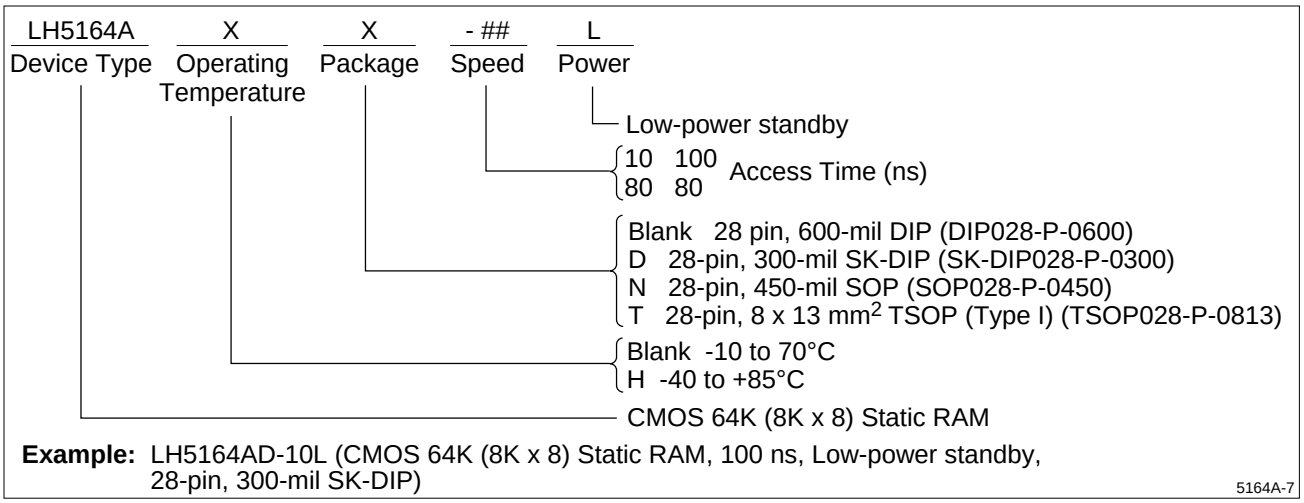
28-pin, 450-mil SOP

28TSOP (TSOP028-P-0813)



28-pin, 8 × 13 mm^2 TSOP (Type I)

ORDERING INFORMATION



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